2

Transconductor

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1. Introduction

The transconductor is a versatile building block employed in many analog and mixed-signal circuit applications, such as continuous-time filters, delta-sigma modulators, variable gain-amplifier or data converter. The transconductor is to perform voltage-to-current conversion. Linearity is one of most critical requirements in designing transconductor. Especially in designing delta-sigma modulators for high resolution Analog/Digital converters, it needs high linearity transconductors to accomplish the required signal-to-(noise+distortions) ratio. The tuning ability of transconductor is also mandated to adjust center frequency and quality factor in filter applications.

The portable electronic equipments are the trend in comsumer markets. Therefore, the low power consumption and low supply voltage becomes the major challenge in designing CMOS VLSI circuitry. However, designing for low-voltage and highly linear transconductor, it requires to consider many factors. The first factor is the linear input range. The range of linear input is justified by the constant transconductance, G_m. Since the distortion of transconductor is determined by the ratio of output currents versus input voltage. The second factor is the control voltage of transconductor. This voltage can greatly impact the value of transconductance, linear range, and power consumption. For example, when the control voltage increases, the transconductance also increase but the linear input range of transconductor is reduced and power consumption is increased. Hence it is critical in designing transconducotr operated at low supply voltage. The third factor is the symmetry of the two differential outputs. If the transconductance of the positive and negative output is $G_{m+}=I_{O+}/V_i$ and $G_{m-}=I_{O-}/V_i$, then how close G_{m+} and G_{m-} should be is a critical issue, where I_{O+} is the positive output current, I_{O-} is the negative output current, and V_i is the input differential voltage. This factor is the major cause of common-mode distortion of transconductor which occurs at outputs.

In general, the design of differential transconductor can be classified into triode-mode and saturation-mode methods depending on operation regions of input transistors. Triode-mode transconductor has a better linearity as well as single-ended performance. On the other hand, saturation-mode transconductor has better speed performance. However, it only exhibits moderate linearity performance. Furthermore, the single-ended transconductor of saturation-mode suffers from significant degradation of linearity. Several circuit design techniques for improving the linearity of transconductors have been reported in literatures. The linearization methods include: source degeneration using resistors or MOS transistors

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[Krummenacher & Joeh, 1988; Leuciuc & Zhang, 2002; Leuciuc, 2003; Furth & Andreou, 1995], crossing-coupling of multiple differential pairs [Nedungadi & Viswanathan, 1984; Seevinck & Wassenaar, 1987] class-AB configuration [Laguna et al., 2004; Elwan et al., 2000; Galan et al., 2002], adaptive biasing [Degrauwe et al., 1982; Ismail & Soliman, 2000; Sengupta, 2005], constant drain-source voltages [Kim et al., 2004; Fayed & Ismail, 2005; Mahattanakul & Toumazou, 1998; Zeki, 1999; Torralba et al., 2002; Lee et al., 1994; Likittanapong et al., 1998], pseudo differential stages [Gharbiya & Syrzycki, 2002], and shift level biasing [Wang & Guggenbuhl, 1990].

Source degeneration using resistors or MOS transistors is the simplest method to linearize transconductor. However, it requires a large resistor to achieve a wide linear input range. In addition, MOS used as resistor exhibits considerable varitions affected by process and temperture and results in the linearity degradation. Crossing-coupling with multiple differential pairs is designed only for the balanced input signals. The Class-AB configuration can achieve low power consumption. On the other hand, the linearity is the worst due to the inherited Class-AB structure. The adaptive biasing method generates a tail current which is proportional to the square of input differential voltage to compensate the distortion caused by input devices. However, the complication of square circuitry makes this technique hard to implement. The constant drain-source voltage of input devices is a simple structure. It can achieve a better linearity with tuning ability. However, it needs to maintain V_{DS} of input devices in low voltage and triode region. Therefore, this technique is difficult to implement in low supply voltage. Hence, a new transconductor using constant drain-source voltage in low voltage application is proposed to achieve low-voltage, highly linear, and large tuning range abilities.

In section 2, basic operatrion and disadvantage of the linerization techniques are described. The proposed new transconductor is presented in section 3. The simulation results and conclusion are given in section 4 and 5.

2. Linearization techniques

In this section, reviews of common linearization techniques reported in literatures are presented. The first one is the transconductor using constant drain-source voltage. The second one is using regulated cascode to replace the auxiliary amplifier. The third one is transconductor with source degeneration by using resistors and MOS transistors. The last one is the linear MOS transconductor with a adaptive biasing scheme. Besides introducing their theories and analyses, the advantages and disadvantages of these linearization techniques are also discussed.

2.1 Transconductor using constant drain-source voltage

The idea of transconductors using constant drain-source voltages is to keep the input devices in triode region such that the output current is linearized. The schematic of this method is shown in Fig. 1. Considering that transistors M_1, M_2 operate at triode region, M_3, M_4 are biased at saturation region, channel length modulation, body effect, and other second-order effects are ignored, the drain current of M_1 and M_2 is given by

$$I_D = \beta\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{1}$$

where $\beta=\mu_n C_{OX}(W/L)$, V_{GS} is the gate-to-source voltage, V_T is the threshold voltage, and V_{DS} is the drain-to-source voltage. If the two amplifiers in Fig. 1 are ideal amplifiers, then

$$V_{DS1} = V_{DS2} = V_C \tag{2}$$

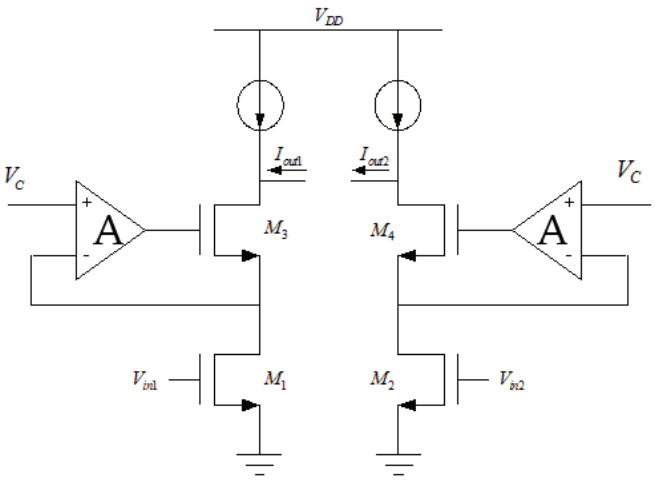


Fig. 1. Transconductor using constant drain-source voltage

The transfer characteristic of this transconductor is given by

$$I_{out1} = \beta\left[(V_{GS1}-V_T)V_{DS1} - \frac{V_{DS1}^2}{2}\right] = \beta\left[(V_{GS1}-V_T)V_C - \frac{V_C^2}{2}\right]$$

$$I_{out2} = \beta\left[(V_{GS2}-V_T)V_{DS2} - \frac{V_{DS2}^2}{2}\right] = \beta\left[(V_{GS2}-V_T)V_C - \frac{V_C^2}{2}\right]$$

$$I_{out} = I_{out1} - I_{out2} = \beta V_C(V_{in1} - V_{in2}) \tag{3}$$

The transconductance value is

$$G_m = \beta V_C \tag{4}$$

In fact, it is difficult to design an ideal amplifier implemented in this circuits. However, it can force $V_{DS1}=V_{DS2}=V_{DS}$ by using two auxiliary amplifiers controlled with the same V_C to keep V_{DS} at the constant value. Therefore, the transfer characteristic of this transconductor is changed as follows:

$$I_{out1} = \beta\left[(V_{GS1}-V_T)V_{DS1} - \frac{V_{DS1}^2}{2}\right] = \beta\left[(V_{GS1}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_{out2} = \beta\left[(V_{GS2}-V_T)V_{DS2} - \frac{V_{DS2}^2}{2}\right] = \beta\left[(V_{GS2}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_{out} = I_{out1} - I_{out2} = \beta V_{DS}\left(V_{in1} - V_{in2}\right) \tag{5}$$

, where $V_{GS1} = V_{in1}$ and $V_{GS2} = V_{in2}$.
Therefore, the new transconductance value is

$$G_m = \beta V_{DS} \tag{6}$$

The linearity of this transconductor is moderated. It is also easy to implement in circuit. However, V_{DS} of the input devices must be small enough to keep transistors in triode region. The following condition has to be satisfied:

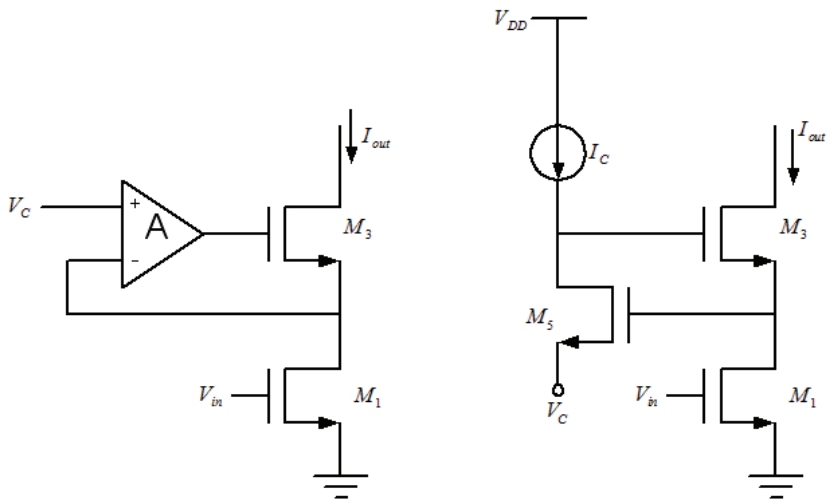
$$V_{DS} < V_{GS} - V_T \tag{7}$$

On the other hand, the auxiliary amplifiers need to design carefully to reduce the overhead of extra area and power.

2.2 Transconductor using regulated cascode to replace auxiliary amplifier

In Fig. 2(a) regulating amplifier keeps V_{DS} of M_1 at a constant value determined by V_C. It is less than the overdrive voltage of M_1. The voltage can be controlled from V_C so as to place M_3 in current-voltage feedback, thereby increasing output impedance. The concept is to drive the gate of M_3 by an amplifier that forces V_{DS1} to be equal to V_C. Therefore, the voltage variations at the drain of M_3 affect V_{DS1} to a lesser extent because amplifiers "regulate" this voltage. With the smaller variations at V_{DS1}, the current through M_1 and hence output current remains more constant, yielding a higher output impedance [Razavi, 2001]

$$R_{out} \approx A g_{m3} r_{O3} r_{O1} \tag{8}$$



(a) (b)

Fig. 2. (a)Basic triode transconductor structure (b) Simple RGC triode transconductor

It is one of solutions using regulated cascode to replace the auxiliary amplifier in order to overcome restrictions on Fig. 1. The circuit in Fig. 2(b) proposed in [Mahattanakul & Toumazou, 1998] uses a single transistor, M_5, to replace the amplifier in Fig. 2(a). This circuit called regulated cascode which is abbreviated to RGC. The RGC uses M_5 to achieve the gain boosting by increasing the output impedance without adding more cascode devices. V_{DS1} is calculated by follows: Assuming M_5 is in saturation region in Fig. 2(b). It can be shown that

$$I_C = \frac{1}{2}\beta_5 (V_{GS5} - V_T)^2$$

$$\Rightarrow V_{GS5} = V_{DS1} - V_C = \sqrt{\frac{2I_C}{\beta_5}} + V_{T5}$$

$$\Rightarrow V_{DS1} = V_C + \sqrt{\frac{2I_C}{\beta_5}} + V_{T5} \tag{9}$$

From (6) $G_m = \beta_1 V_{DS1} = \beta_1 \left(V_C + \sqrt{\frac{2I_C}{\beta_5}} + V_{T5} \right)$. Thus, G_m can be tuned by using a controllable voltage source V_C or current source I_C. However, it is preferable in practice to use a controllable voltage source V_C for lowering power consumption since V_{DS1} only varies as a square root function of I_C.

Simple RGC transconductor using a single transistor to achieve gain boosting can reduce area and power wasted by the auxiliary amplifiers. However, it still has some disadvantages. First, it will cause an excessively high supply-voltage requirement and also produce an additional parasitic pole at the source of transistors. Therefore, it can not apply to the low-supply voltage design. Second, the tuning range of V_{DS1} is restricted. The smallest value of V_{DS1} is $\sqrt{\frac{2I_C}{\beta_5}} + V_T$ when $V_C = 0$. In other words, V_{DS1} can not be set to zero. Owing to the restriction of (7), V_{DS} is as low as possible and the best value is zero. Third, V_T dependent G_m may be a disadvantage due to the substrate noise and V_T mismatch problems [Lee et al., 1994].

In Fig. 3, another RGC transconductor that can apply to the low-voltages applications is proposed in [Likittanapong et al., 1998]. The circuit overcomes the disadvantages mentioned above is to utilize PMOS transistor that can operate in saturation region as gain boosting. The use of this PMOS gain boosting in the feedback path can result in a circuit with a wide transconductance tuning range even at the low supply voltage. In [Likittanapong et al., 1998], it mentions that at the maximum input voltage, M_3 may be forced to enter triode region, especially if the dimension of M_2 is not properly selected, resulting in a lower dynamic range. Besides, β_2 may be chosen to be larger for a very low distortion transconductor. It means that the tradeoff between linearity and bandwidth of transconductor is controlled by β_2. Therefore, β_2 should be selected to compromise these two characteristics for a given application.

V_{DS1} is calculated by follows. Assuming M_3 is in saturation region in Fig. 3.

$$I_C = \frac{1}{2}\beta_3 (V_{GS3} - V_{T3})^2$$

$$=> V_{GS3} = V_C - V_{DS1} = \sqrt{\frac{2I_C}{\beta_3}} + V_{T3}$$

$$=> V_{DS1} = V_C - \left(\sqrt{\frac{2I_C}{\beta_3}} + V_{T3} \right) \quad (10)$$

From (6) $G_m = \beta_1 V_{DS1} = \beta_1 \left[V_C - \left(\sqrt{\frac{2I_C}{\beta_3}} + V_{T3} \right) \right]$. It shows that V_{DS1} can be set to zero when $V_C = \sqrt{\frac{2I_C}{\beta_3}} + V_{T3}$. Therefore, this transconductor has a wider tuning range compared to that of RGC transconductor and is capable of working in low-supply voltage (3V). However, this transconductor still has some drawbacks. The major drawback is the tuning ability. For example, it is difficult to control $V_C = \sqrt{\frac{2I_C}{\beta_3}} + V_{T3}$ if V_{DS1} is set to zero. The minor drawback is that V_T depends on the G_m. It also may cause substrate noise and V_T mismatch problems [Lee et al., 1994].

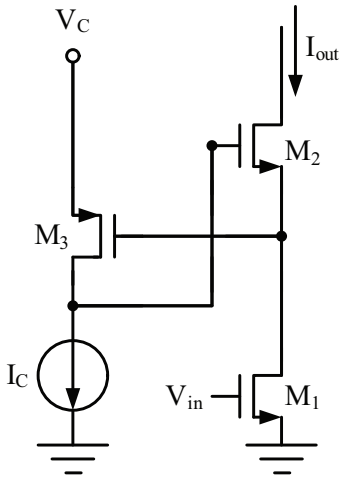


Fig. 3. RGC transconductor with PMOS gain stage

2.3 Transconductor using source degeneration

A simple differential transconductor is shown in Fig. 4(a). Assuming that M_1 and M_2 are in saturation and perfectly matched, the drain current is given by

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \quad (11)$$

The transfer characteristic using (5) is given by

$$I_{out} = I_{out1} - I_{out2} = \sqrt{2\beta I_{SS}}V_i\sqrt{1-\frac{\beta V_i^2}{8I_{SS}}} = \sqrt{2\beta I_{SS}}V_i\sqrt{1-\frac{V_i^2}{4(V_{GS}-V_T)}} \tag{12}$$

, where $V_i = (V_{in1} - V_{in2})$
If V_{GS} is large enough, the higher linearity can be achieved. Unfortunately, it can not be used in the low-voltage application and the linear input range is limited. Simplest techniques to linearize the transfer characteristic of MOS transconductor is the one with source degeneration using resistors as shows in Fig. 4(b). The circuit is described by

$$V_i - RI_{out} = V_{GS1} - V_{GS2} \tag{13}$$

A transfer characteristic derived from (13) is given by

$$I_{out} = \sqrt{2\beta I_{SS}}\left(V_i - RI_{out}\right)\sqrt{1-\frac{\beta\left(V_i - RI_{out}\right)^2}{8I_{SS}}} \tag{14}$$

The transconductance G_m is

$$G_m \approx \frac{g_m}{1+g_m R} \tag{15}$$

where g_m is the transconductance of transistor M_1 and M_2.
We should notice that in (14), the nonlinear term depends on $V_i - RI_{out}$ rather than V_i. Higher linearity can be achieved when $R >> 1/g_m$. The disadvantage of this transconductor is that large resistor value is needed in order to maintain a wider linear input range. Owing to $G_m \approx 1/R$, the higher transconductance is limited by the smaller resistor. Hence, there is a tradeoff between wide linear input range and higher transconductance which is mainly determined by a resistor.

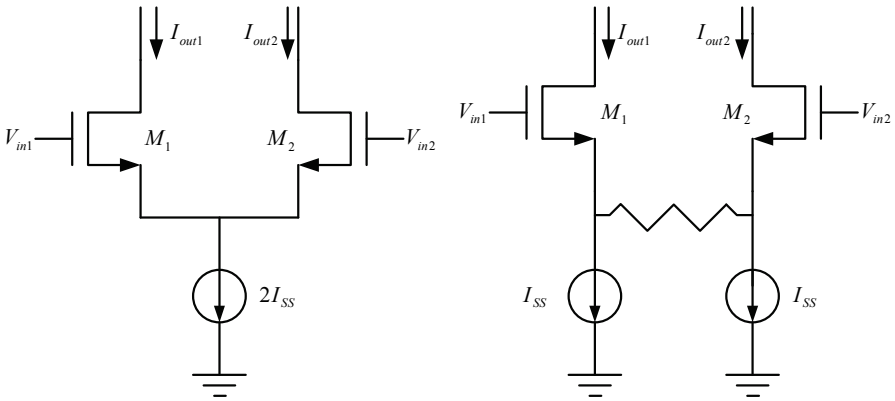


Fig. 4. (a) Simple differential MOS transconductor (b) MOS transconductor with resistive source degeneration

Another method to linearize the transfer characteristic of MOS transconductor is using source degeneration to replace the degeneration resistor with two MOS transistors operating in triode region. The circuit is shown in Fig. 5. Notice that the gates of transistor M_3 and M_4 connect to the differential input voltage rather than to a bias voltage. To see that M_3 and M_4 are generally in triode region, we look at the case of the equal input signals (V_{in1}=V_{in2}), resulting in

$$V_x = V_y = V_{in1} - V_{GS1} \tag{16}$$

Therefore, the drain-source voltages of M_3 and M_4 are zero. However, V_{DS} of M_3 and M_4 equal those of M_1 and M_2. Owing to (7), M_3 and M_4 are indeed in triode region. Assuming M_3, M_4 are operating in triode region, the small-signal drain-source resistance of M_3, M_4 is given by

$$r_{ds3} = r_{ds4} = \frac{1}{\beta_3 (V_{GS1} - V_T)} \tag{17}$$

It must be noted that in this circuit the effect of varying V_{DS} of M_1 and M_2 can not be ignored since the drain currents are not fixed to a constant value. The small-signal source resistance of M_1, M_2 is given by

$$r_{s1} = r_{s2} = \frac{1}{g_{m1}} = \frac{1}{\beta_1 (V_{GS1} - V_{T1})} \tag{18}$$

Using small-signal T model, the small-signal output current, i_{o1}, is equal to

$$\begin{aligned} i_{o1} &= \frac{V_{in1} - V_{in2}}{r_{s1} + r_{s2} + (r_{ds3} \,||\, r_{ds4})} \\ \Rightarrow i_{o1} &= \frac{2\beta_1\beta_3}{\beta_1 + 4\beta_3}(V_{GS1} - V_{T1})(V_{in1} - V_{in2}) \end{aligned} \tag{19}$$

Assuming M_1 is in saturation region, the drain current of M_1 is given by

$$\begin{aligned} I_{SS} &= \frac{1}{2}\beta_1 (V_{GS1} - V_{T1})^2 \\ \Rightarrow (V_{GS1} - V_{T1}) &= \sqrt{\frac{2I_{SS}}{\beta_1}} \end{aligned} \tag{20}$$

Using (20) substitutes for (19), that leads to

$$i_{o1} = \frac{2\beta_1\beta_3}{\beta_1 + 4\beta_3}\sqrt{\frac{2I_{SS}}{\beta_1}}(V_{in1} - V_{in2}) \tag{21}$$

The transconductance G_m is

$$G_m = \frac{2\beta_1\beta_3}{\beta_1 + 4\beta_3}\sqrt{\frac{2I_{SS}}{\beta_1}} \tag{22}$$

Linearity can be enhanced (assuming $r_{ds3} >> r_{s1}$) compared to that of a simple differential pair because transistors operated in triode region exhibits higher linearity than the source resistances of transistors operated in saturation region. When the input signal is increased, the small-signal resistance in one of two triode transistors in parallel, M_3 or M_4, is reduced. Meanwhile, the reduced resistance results in the lower linearity and the larger transconductance. As discussed in [Krummenacher & Joeh, 1988], if the proper size ratio of β_1/β_3 is chosen, the balance between higher linearity and stable transconductance can be achieved. How to choose the optimum size ratio of β_1/β_3 for the best linearity performance becomes slightly dependent on the quiescent overdrive voltage, $V_{GS}-V_T$. The size ratio of β_1/β_3=6.7 is used to achieve the best linearity performance.
According to (22), the transconductance can be tuned by changing I_{SS} and size ratio of β_1/β_3. Nevertheless, the nonlinearity error is up to 1% for I_{out}/I_{SS} < 80%. It is required to have a better linearity so as to achieve a THD of -60 dB or less in some filtering applications [Kuo & Leuciuc, 2001].

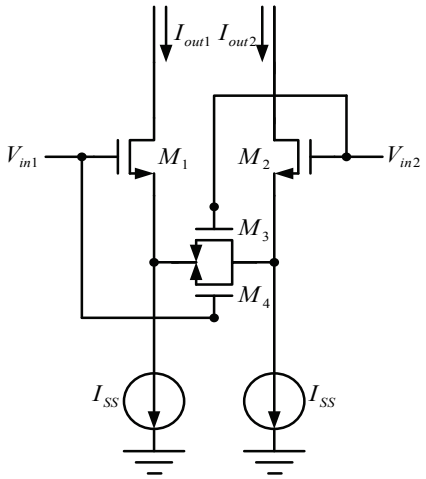


Fig. 5. Transconductor with source degeneration using MOS transistors

2.4 Transconductor using adaptive biasing

The transconductor using adaptive biasing is shown in Fig. 6. All transistors are assumed to be operated in saturation region, neglecting channel lengh modulation effect. First, transistor M_3 is absent, and output current as a function of two input voltages V_{in1} and V_{in2} is obtained as

$$I_1 = \frac{\beta}{2}\left(V_{GS1} - V_T\right)^2$$

$$I_2 = \frac{\beta}{2}\left(V_{GS2} - V_T\right)^2 \tag{23}$$

$$\Rightarrow I_{out} = I_1 - I_2 = \sqrt{\beta I_{SS}}\left(V_{in1} - V_{in2}\right)\sqrt{1 - \frac{\beta\left(V_{in1} - V_{in2}\right)^2}{4I_{SS}}}$$

, where I_{SS} is a tail current and equals I_B.
An adaptive biasing technique is using a tail current containing an input dependent quadratic component to cancel the nonlinear term in (23). Consequently, the circuit in Fig. 6 changes the tail current by adding transistor M_3. The tail current will be changed by

$$I_{SS} = I_B + I_C \tag{24}$$

$$I_C = \frac{\beta}{4}\left(V_{in1} - V_{in2}\right)^2 \tag{25}$$

, where I_B is tail current of differential pair and I_C is the compensating tail current that cancel nonlinear term.
Therefore, the transfer characteristic is changed by

$$I_{out} = \sqrt{\beta I_{SS}}\left(V_{in1} - V_{in2}\right) \tag{26}$$

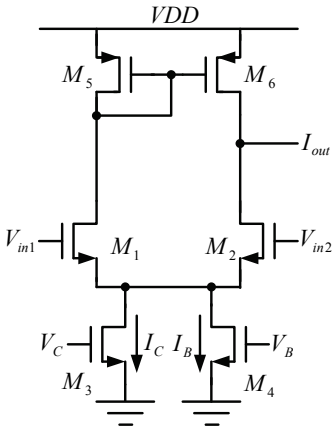


Fig. 6. Transconductor with adaptive biasing

3. New transconductor

The conventional structure which uses the constant drain source-voltage such as RGC with NMOS or PMOS can not operate at 1.8V or below. The main reason is that auxiliary amplifier under the low supply voltage can't provide enough gain to keep the constant drain-source voltage. Therefore, we propose a triode transconductor which uses new structure to replace the auxiliary amplifier. Fig. 7 shows the proposed triode transconductor structure.
MOS M_5, M_7, M_9 and M_{11} are made up a two-stage amplifier to replace the auxiliary amplifier. The two-stage amplifier is implemented using M_9 with the active loads M_{11} formed the first stage and M_5 with the active load M_7 formed the second stage. The first and second stages exhibit gains equal to

$$A_1 = gm_9\left(g_{m9}^{-1} \,||\, r_{O11}\right) \tag{27}$$

$$A_2 = gm_5\left(r_{O5} \,||\, r_{O7}\right) \tag{28}$$

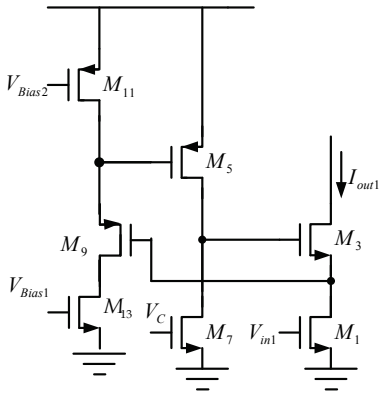


Fig. 7. Proposed triode transconductor

Therefore, the overall gain is

$$A_v = A_1 * A_2 = gm_9\left(g_{m9}^{-1} \,||\, r_{O11}\right) gm_5\left(r_{O5} \,||\, r_{O7}\right) \tag{29}$$

The proposed transconductor is shown in Fig. 8.

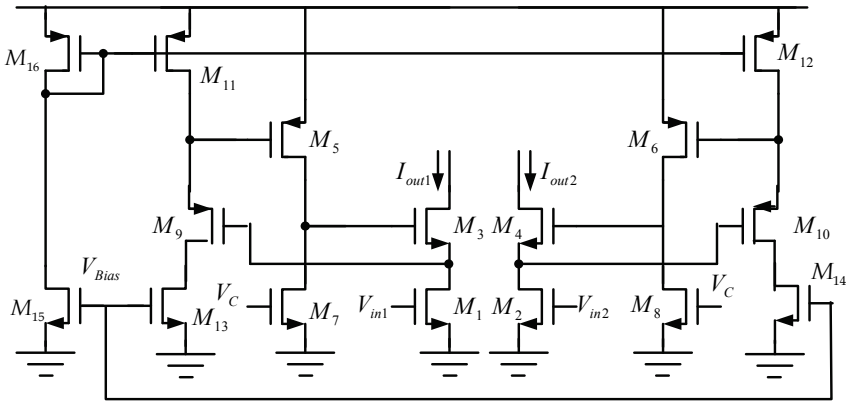


Fig. 8. The proposed transconductor

Considering that the large gain is achieved and is able to keep transistors M_1 and M_2 in triode region, the drain current of M_1 and M_2 is given by

$$I_{out1} = \beta_1\left[\left(V_{GS1} - V_{T1}\right)V_{DS1} - \frac{V_{DS1}^2}{2}\right] \tag{30}$$

$$I_{out2} = \beta_2\left[\left(V_{GS2} - V_{T2}\right)V_{DS2} - \frac{V_{DS2}^2}{2}\right] \tag{31}$$

The transfer characteristic is given by

$$I_{out} = I_{out1} - I_{out2} = \beta_1 V_{DS1}\left(V_{in1} - V_{in2}\right) \tag{32}$$

, where $\beta_1 = \beta_2$, $V_{T1} = V_{T2}$, and $V_{DS1} = V_{DS2}$. Assuming that current I_9 flows from M_{11} through M_9 and MOS M_9 is in saturation region, V_{DS1} can be found in (33)

$$V_{GS3} + V_{DS1} = V_{DS7}$$

$$V_C - V_{T7} = V_{DS7}$$

$$\Rightarrow V_{GS3} + V_{DS1} = V_C - V_{T7}$$

$$V_{DS1} = V_C - V_{T7} - V_{GS3} \tag{33}$$

According to (32)

$$I_{out} = \beta_1 V_{DS1}\left(V_{in1} - V_{in2}\right) = \beta_1\left(V_C - V_{T7} - V_{GS3}\right)\left(V_{in1} - V_{in2}\right) \tag{34}$$

The transconductance G_m is

$$G_m = \beta_1\left(V_C - V_{T7} - V_{GS3}\right) \tag{35}$$

From (35), the transconductance can be tuned by control voltage V_C To keep M_1 and M_2 in triode region, the relation (36) needs to be satisfied.

$$V_{DS1} < V_{GS1} - V_{T1} \tag{36}$$

Using (33) to substitute (36)

$$V_C - V_{T7} - V_{GS3} \le V_{GS1} - V_{T1} \Rightarrow V_C \le V_{GS1} + V_{GS3} - \left(V_{T1} - V_{T7}\right) \tag{37}$$

The proposed transconductor is suitable for low supply voltage and we choose 1.8V to achieve a wide linear range. Moreover, M_9 is needed to obtain a negative feedback to keep the drain-source voltage of M_1, V_{DS1}, constant. This new structure can provide enough gain to keep V_{DS1} constant at 1.8V supply voltage. It has a low control voltage V_C between 0.69V~0.72V and the large transconductance tuning range depending on applications. Besides, it has a simple structure so as to save area.

4. Simulation results

The circuits in Fig. 8 have been designed by using TSMC CMOS 0.18μm process with a single 1.8V supply voltage and simulated by Hspice. Fig. 9. shows the curve of input voltage transferring to the output current at V_C = 0.7V. The slope of the curve is linear when the input voltage varies from −1V to 1V. The slope in Fig. 9. is equal to the transconductance in Fig. 10. In order to verify the performance of the proposed transconductor, we define transconductance error (equation 39) as the linearity of the transconductance's output current. The transconductance error is less than 1% among ±0.9V input voltage, so the input linear range is up to 1.8V.

$$TE(\%) = \frac{G_m\left(V_{id}\right) - G_m(0)}{G_m(0)} * 100 \tag{39}$$

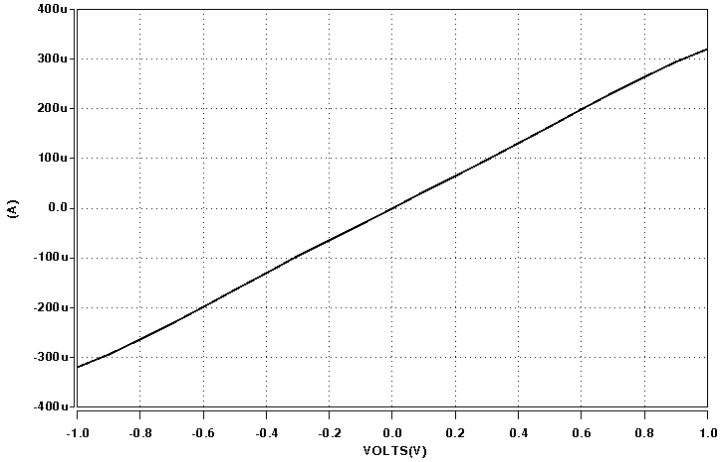


Fig. 9. V-I transfer characteristic

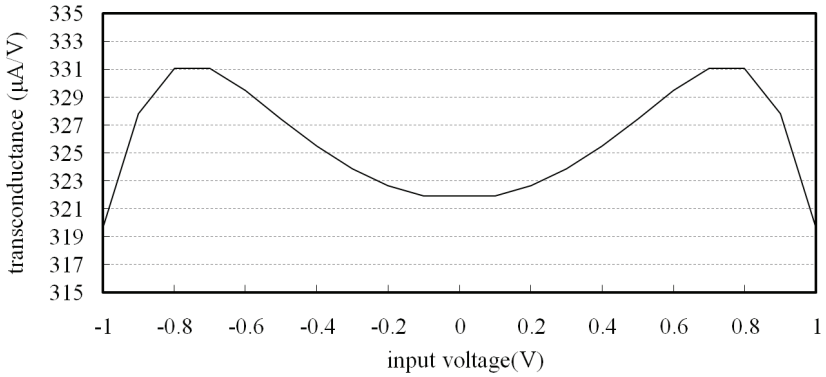


Fig. 10. The simulated transconductance at V_C=0.7V

In Fig. 11. it shows the drain-source voltage of the input transistors M_1 and M_2, V_{DS1} and V_{DS2}, changes with the input voltage. Within ±1V input voltage, V_{DS1} and V_{DS2} are very small. According to equation (40), V_{DS1} and V_{DS2} are too small such that transistors M_1 and M_2 can be set in triode region. Once the input voltage exceeds ±1V, V_{DS1} and V_{DS2} will increase rapidly. It results in that transistors M_1 and M_2 enter in saturation region. In other words, when M_1 and M_2 entering saturation region the proposed transconductor can not maintain the high linearity.

$$V_{DS} < V_{GS} - V_T \tag{40}$$

When V_C is set between 0.69V and 0.72V, the linear input range is up to 2.6V and the transconductance error is less than 1%. The smallest transconductance is 3.4μs and linear input range is 1.2V when V_C is 0.720V. The highest transconductance is 542μs and linear input range is 1.4V when V_C is 0.690V. Table 1 shows the linear input range and the transconductance tuned by different V_C. Therefore, the proposed transconductor achieve a large tuning range.

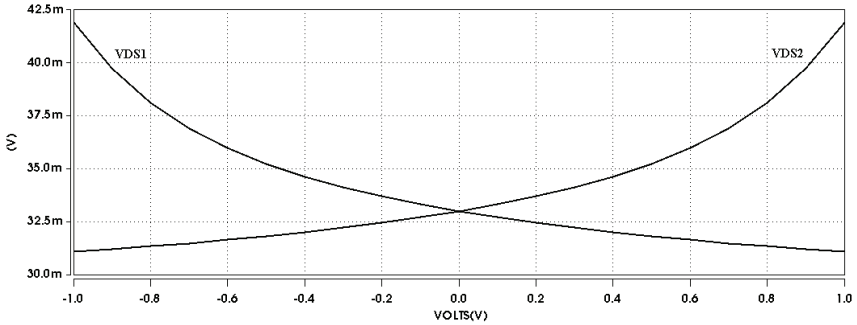


Fig. 11. The drain-source voltage of input transistor M_1 and M_2

V_C (V)	Linear input range (V)	Transconductance (μS)
0.690	1.4	542
0.695	1.8	434
0.700	1.8	326
0.705	2.2	219
0.710	2.4	122
0.715	2.6	42
0.720	1.2	3.4

Table 1. V_C versus Linear input range

In Fig. 12., the simulated THD as a function of the input frequency and input signal amplitude is plotted. The best THD is achieved at the low input voltage and the low frequency. When V_C is 0.7V, the linearity of the proposed transconductor is less than −60dB for 0.7Vpp at 100KHz.

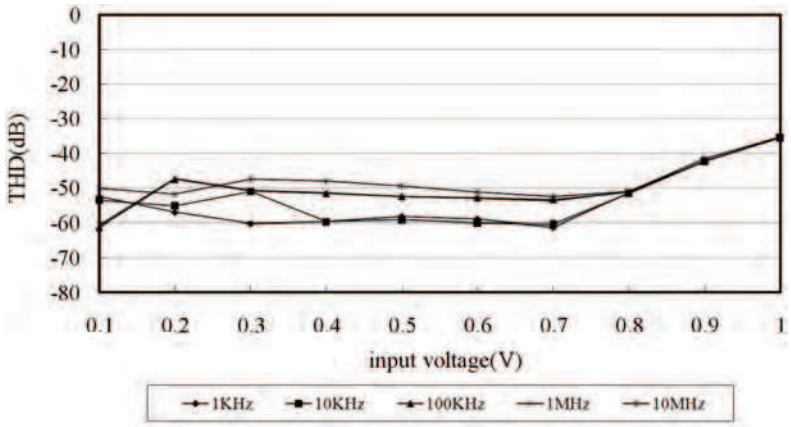


Fig. 12. Simulated THD for different input frequencies

Fig. 13. shows the linearity of transconductor in three linearization techniques. The transconductor using source degeneration with resistor is shown in Fig. 4(b), and the transconductance in Fig. 13(a) is tuned by different resistors. The transconductor using

source degeneration with MOS transistors is shown in Fig. 5, and the transconductance in Fig. 13(b) is tuned by the different size ratio of β_1/β_3. The transconductor using adaptive biasing is shown in Fig. 6, and the transconductance in Fig. 13(c) is tuned by the different compensating tail current, I_C. Fig. 14. Shows the simulation result of the proposed technique and other techniques. Fig. 14(a) is the full plot of the different linearization techniques. From Fig. 14(b) it can be easily seen that the linearity achieved by the newly proposed technique is better than all other implementations.

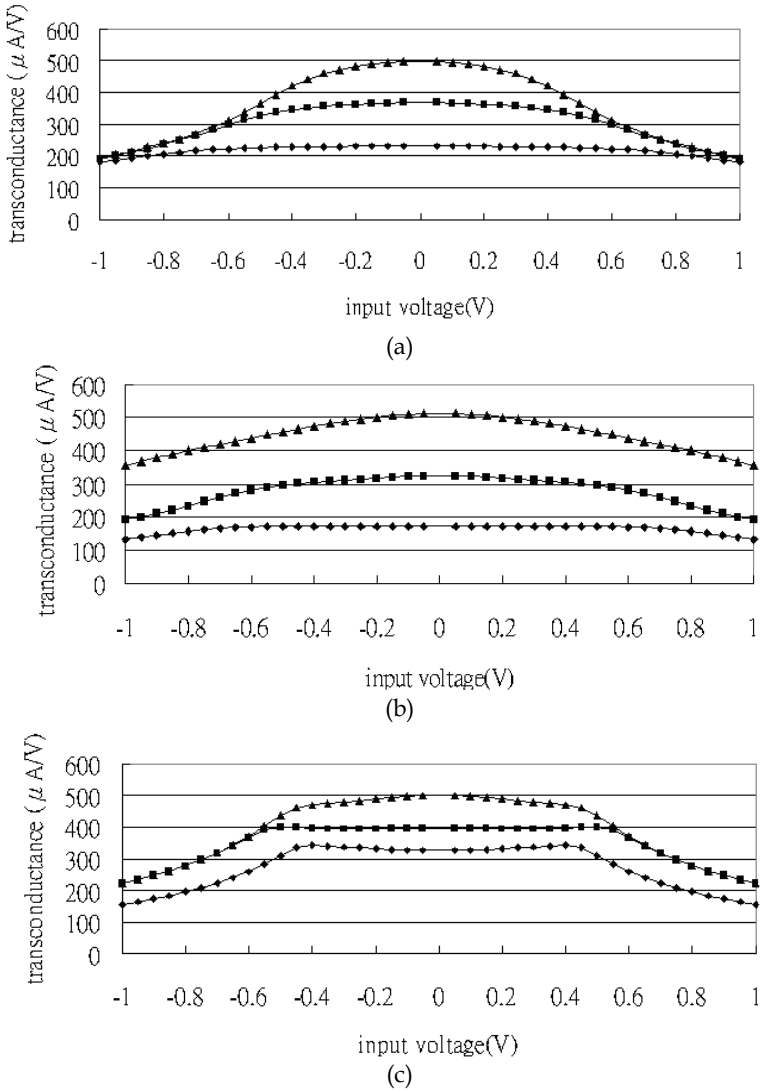
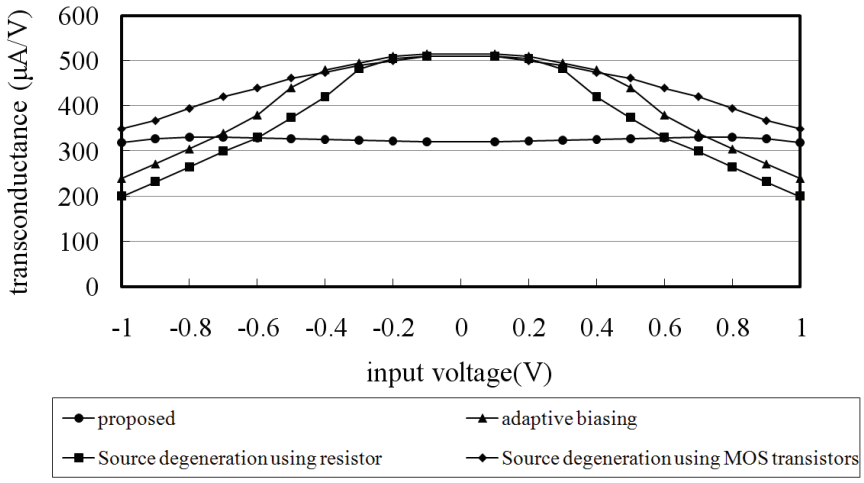
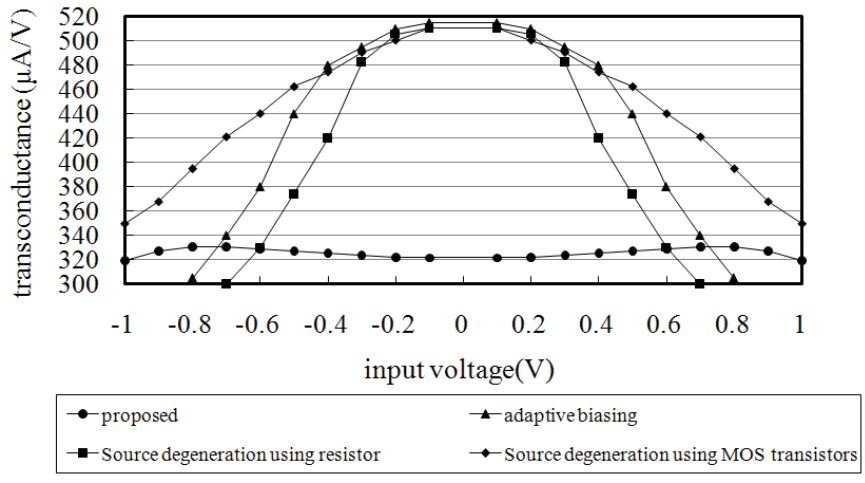


Fig. 13. Simulated transconductance of three linear transconductors (a) Source degeneration using resistor (b)Source degeneration using MOS transistors (c)Adaptive biasing



(a)



(b)

Fig. 14. Simulated transconductance for four linearization techniques (a) Full plot (b) Detail

The simulated THD of the output differential current versus the input signal amplitude for the four linearized transconductors is plotted in Fig. 15. The proposed transconductor achieves THD less than −61dB for the 0.7Vpp input voltage, 11dB better than the one using source degeneration using resistor, 24dB better than the one using source degeneration using MOS, and 31dB better than the one using adaptive biasing, at the same input range.

Table 2. shows the power consumption of the four linearized transconductors at the same transconductance. Power consumption changes with the different transconductances. Therefore, the same transconductance is chosen to be compared in each configuration. Table 3. shows different power consumption at the different transconductance of the proposed transconductor.

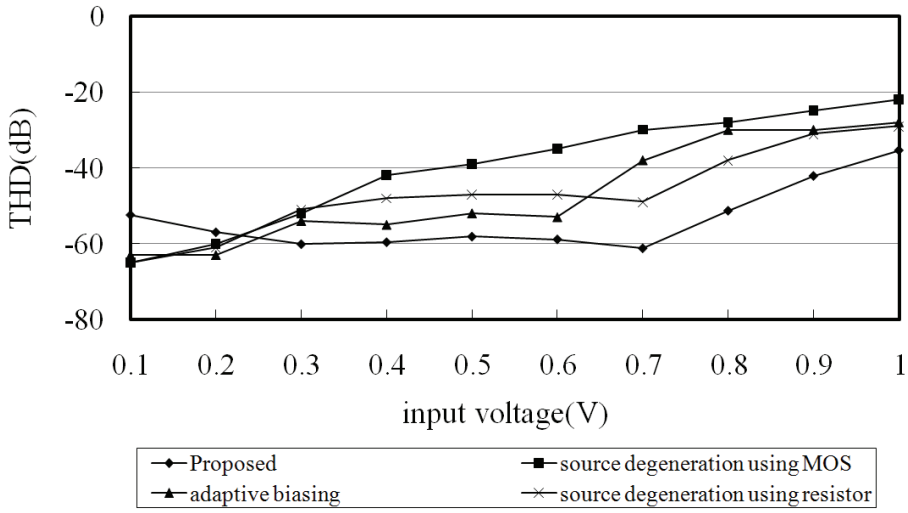


Fig. 15. Simulated THD at 1MHz for the four linearized transconductors

	Source degeneration using MOS	Source degeneration using resistor	Adaptive biasing	Proposed
Power (mW)	1.31	1.19	1.38	1.58

Table 2. The power consumption of four linearized transconductors

V_C (V)	Power (mW)	G_m (μA/V)
0.690	1.759	542
0.695	1.714	434
0.700	1.586	326
0.705	1.442	219
0.710	1.263	122
0.715	0.954	42
0.720	0.733	3.4

Table 3. The power consumption at different transconductances

Table 4. shows the comparison of performance with other transconductors at the low supply voltage (under 2V). The transconductor in [Fayed & Ismail 2005] also uses constant drain-source voltage. It modifies the basic structure of constant drain source voltage and uses the moderate amplifier. The proposed transconductor modifies the auxiliary amplifiers to obtain high gain under low supply voltage.

The layout including proposed transconductor, Common Mode Feedback, and bandgap is shown in Fig. 16. The proposed transconductor uses STC pure 1.8V linear I/O library in 0.18μm CMOS process. The chip area is 0.516mm^2.

	[Galan et. al 2002]	[Leuciuc & Chang 2002]	[Laguna et. al 2004]	[Sengupta 2005]	[Fayed & Ismail 2005]	Proposed
Process	0.8μm	0.25μm	0.8μm	0.18μm	0.18μm	0.18μm
Power supply	2V	1.8V	1.5V	1.8V	1.8V±10%	1.8V
THD	-40dB @10MHz	-80dB, 0.8Vpp, @2.5MHz	-33dB, 0.2Vpp, @5MHz	-65dB, 1Vpp, @1MHz	-50dB, 0.9Vpp, @50KHz	-60dB, 0.7Vpp, @100KHz
G_m (μA/V)	0.6~207	200~600	67~155	770	5~110	3.4~542
Linear input range	0.6Vpp	1.4Vpp	0.6Vpp	1Vpp	1.8Vpp	2.4Vpp
Year	2002	2002	2004	2005	2005	2009

Table 4. Comparison table

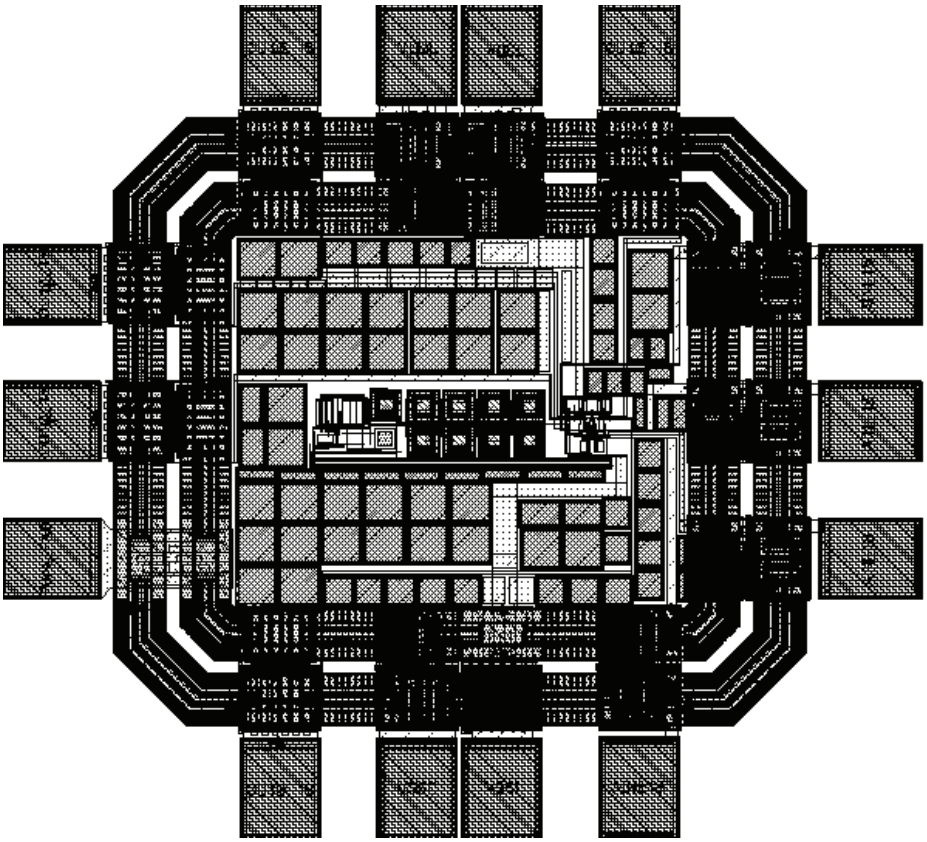


Fig. 16. The layout of proposed transconductor

5. Conclusion

The proposed low-voltage, highly linear, and tunable triode transconductor achieves the wide linear input range up to 2.4V. The total harmonic distortion is −60dB with a $0.7V_{pp}$ input voltage. The design uses TSMC 0.18μm CMOS technology and supply voltage is 1.8V. Moreover, it exhibits a large G_m tuning range from 3.4μS to 542μS and also keeps a wide linear input range. Finally, the performance comparison with other linear techniques shows that the proposed technique achieves better linearity, wider tuning range, and wider linear input range.

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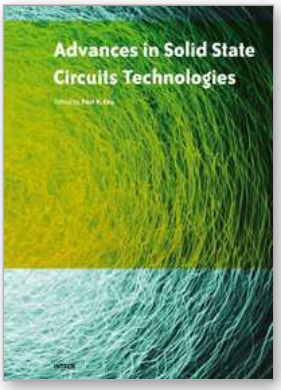

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This book brings together contributions from experts in the fields to describe the current status of important topics in solid-state circuit technologies. It consists of 20 chapters which are grouped under the following categories: general information, circuits and devices, materials, and characterization techniques. These chapters have been written by renowned experts in the respective fields making this book valuable to the integrated circuits and materials science communities. It is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions. Readers will be able to familiarize themselves with the latest technologies in the various fields.

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