UHF Power Transmission for Passive Sensor Transponders

Tobias Feldengut, Stephan Kolnsberg and Rainer Kokozinski
Fraunhofer Institute for Microelectronic Circuits and Systems (IMS)
Germany

1. Introduction

The importance of wireless sensors in medical systems, automotive applications, and environmental monitoring is growing continuously. A sensor node converts physical values such as pressure, temperature, or mechanical stress to digital values. The wireless interface connects it to a base station or a network for further data processing. Most of these products are required to be light, cheap, long lived, and maintenance free. Remote powering of transponder tags is a key technology to meet these demands, because it obviates the need for a battery. Near field systems usually operate in the low frequency range, typically between the 133 kHz (LF) and the 13.56 MHz (HF) ISM bands. While LF and HF systems operate in the magnetic near field via inductive coupling between two coils, UHF systems use electromagnetic waves in the far field of the base station. The range of the available inductive systems is typically limited to less than one meter, which motivates the use of far field energy transmission at ultra high frequencies. This chapter presents the design of a passive long range transponder with temperature sensor. The system is shown in figure 1.

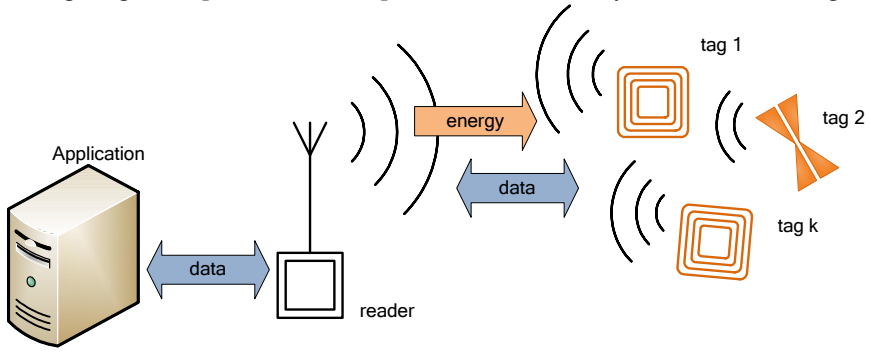


Fig. 1.passive far-field transponder system

A base station transmits an 868 MHz carrier wave that is modulated with the forward link data. In the transponder chip, the antenna voltage is rectified and multiplied to serve as the supply voltage for the integrated circuits including the sensor and a digital part. When the tag is transmitting data to the reader (backward link), it switches its input impedance

between two different states to modulate its own radar cross section. The transponder is shown in figure 2. It consists of an integrated circuit and an antenna. The ASIC comprises an analog front-end as an air interface, a digital part for protocol handling, as well as non-volatile memory. The temperature sensor and the readout circuit are integrated on the same chip.

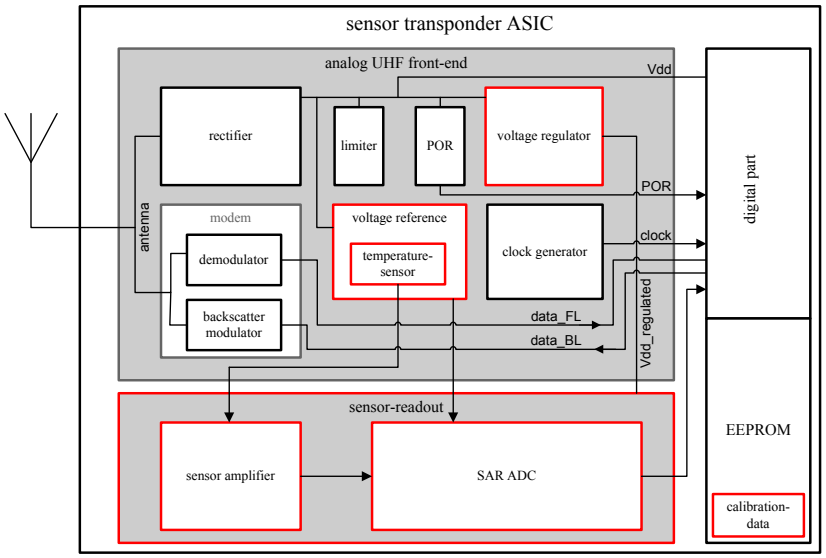


Fig. 2. sensor transponder architecture

The power supply block generates a stable 1.5 V voltage for the other circuit blocks by rectifying and regulating the incoming RF signal. The modem contains a simple low-power ASK demodulation circuit and a modulation switch. The carrier frequency from the reader is far too high to serve as a clock for the digital part, so that a local oscillator circuit is required. A bandgap circuit generates supply independent reference voltages and bias currents. It also generates a temperature-dependent voltage that is amplified to serve as the temperature sensor. This chapter is focused on the design of the analog front-end

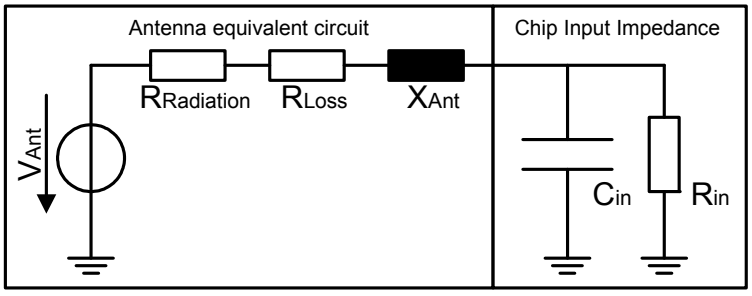


Fig. 3. simple equivalent circuit of transponder input

According to the well known Friis relation

$$P = P_{EIRP} G \frac{\lambda_{RF}^2}{(4\pi d)^2} \tag{1}$$

the power P that is available at the location of the transponder tag is related to the antenna gain G, the distance from the base station d and the wavelength λ_{RF}. The available power is sufficient to power the integrated circuits even in a far distance, but the high frequency antenna voltage is critically low. Figure 3 shows a simplified equivalent circuit of the tag input and the antenna. The antenna can be modelled as a radiation resistance $R_{Radiation}$, a loss resistance R_{Loss} and a reactive part X_{Ant}. The input of the transponder is modelled as a resistor and a capacitor as a linear approximation of the actual rectifier input impedance [Curty et. al, 2005]. Antenna matching is used to achieve high input voltage amplitude as well as power matching. The amplitude of the incoming signal is often as low as the threshold voltage of the rectifying devices, and sufficient rectifier efficiency is therefore difficult to achieve. Chapter 2.1 is focused on the rectifier optimisation.

2. Front-End Design

The analog front-end is mainly used for supply voltage generation, modulation and demodulation of data, clock synthesis, and reference voltage generation. In order to achieve a long range operation, all circuit blocks need to be optimised for ultra low power consumption. The main circuit blocks, namely the rectifier, the bandgap reference, the modem and the clock generator will be presented.

2.1 Rectifier

The rectifier is the most critical circuit for efficient energy transmission. The input from the antenna is a high frequency (868 MHz) signal with amplitude of less than 500 mV at large distance from the base station. Rectifying diodes are required to operate at (or slightly below) the threshold voltage. Recent research efforts have focused on the modelling and the optimisation of the typically used multi-stage Dickson charge pump [Curty et. al., 2005]; [Karthaus & Fischer, 2003]. This circuit is shown in figure 4.

Ideally, diode D1 and capacitor C1 lift the AC input voltage up by its peak value. Diode D2 and capacitor C2 create a peak detector, so that the output voltage of the first stage is set to twice the input amplitude. Several stages are cascaded to reach an output voltage that is high enough for the reliable operation of all circuits. At high frequencies and at low input voltage levels, the behavior of actual implementations differs significantly from the predictions of this simplified explanation [Karthaus & Fischer, 2003]. This fact results from the parasitics of real world devices, especially in cheap standard CMOS solutions. The following effects are detrimental to the rectifier performance. The diodes exhibit

- forward voltage drop,
- significant substrate and junction capacitances,
- reverse leakage current, and substrate leakage.

These values depend not only on the diode area, but also on the output current of the rectifier, on the temperature, and on random process variations. In addition to the diode parasitics, integrated capacitors exhibit parasitic substrate capacitances, series resistance, limited capacitance values, and leakage current. Finally, package parasitics, pad capacitance,

and metal line parasitics can not be neglected. All of the above mentioned effects need to be considered and make the rectifier design a challenging task.

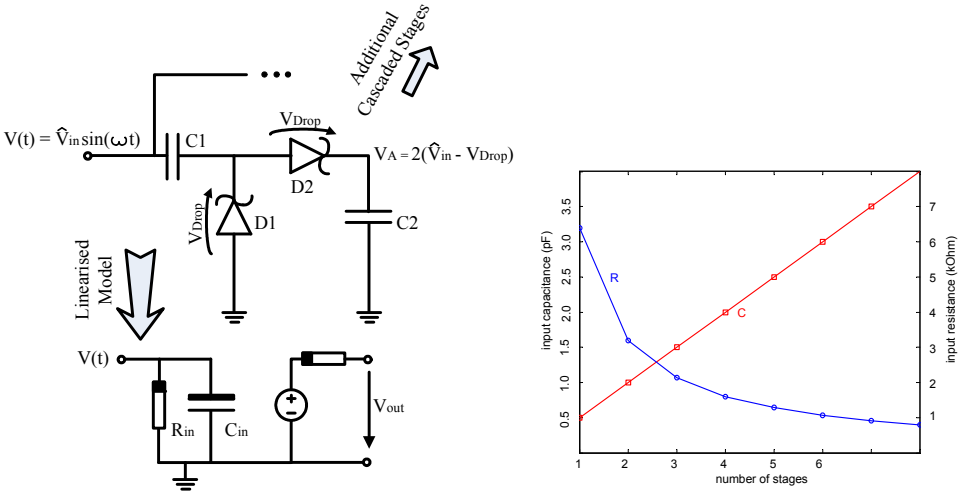


Fig. 4. basic rectifier stage, linearised model, and input impedance [Curty et. al., 1005]

Figure 4 also shows a linear model of the rectifier circuit [1]. It consists of an input resistance and an input capacitance, as well as an output voltage source and an output resistance. The antenna should be inductively matched to this input impedance of the rectifier. The tag also exhibits an input capacitance due to the above mentioned parasitic capacitances.

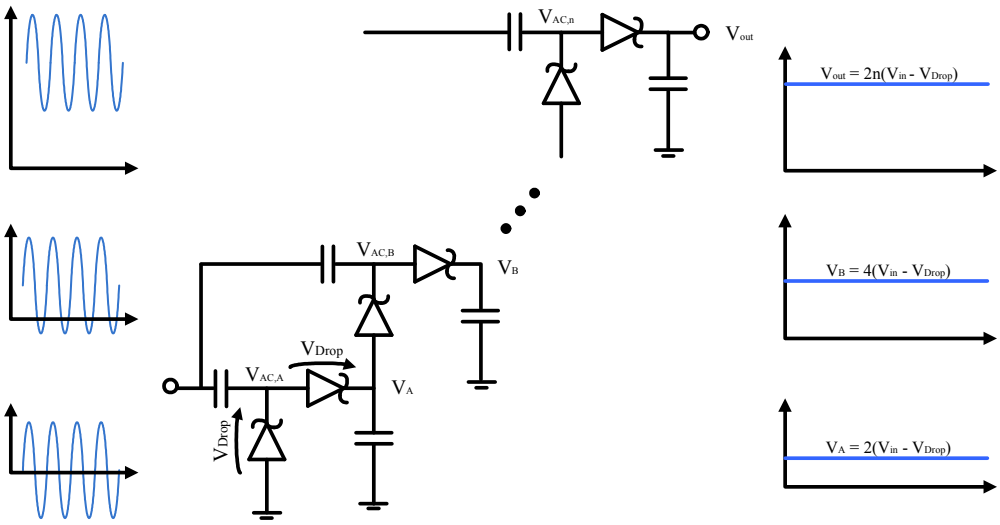


Fig. 5. multi stage voltage multiplier

At high quality factors, the bandwidth of the system is reduced, and inductive antenna matching is more difficult to achieve, so the input capacitance should be minimised. In summary, the goal of the rectifier design is to minimise the required input voltage and to achieve a large input impedance and low input capacitance for a given output current consumption. The major design concerns are therefore minimising the capacitance between AC and DC nodes as well as reducing the voltage drop

Figure 5 shows a multiplier stack with several stages, as well as the resulting waveforms at the AC terminal and the DC nodes. Each diode reduces the achievable output voltage by one threshold voltage drop. This voltage drop is a significant issue, as 12 diodes create a voltage drop of more than 2 V. One way to reduce this voltage drop is to use transistor diodes with threshold voltage compensation. This approach is depicted in figure 6 [Nakamoto et. al, 2007]. The gate of the transistor diode is forward biased by one threshold voltage, so that the device effectively acts as a diode with zero threshold voltage. The threshold voltage of transistors varies with temperature and process fluctuations, and the compensation voltage needs to track this variation. A compensation voltage that is too large would significantly increase reverse leakage currents, because the transistor could not close properly (see figure 7).

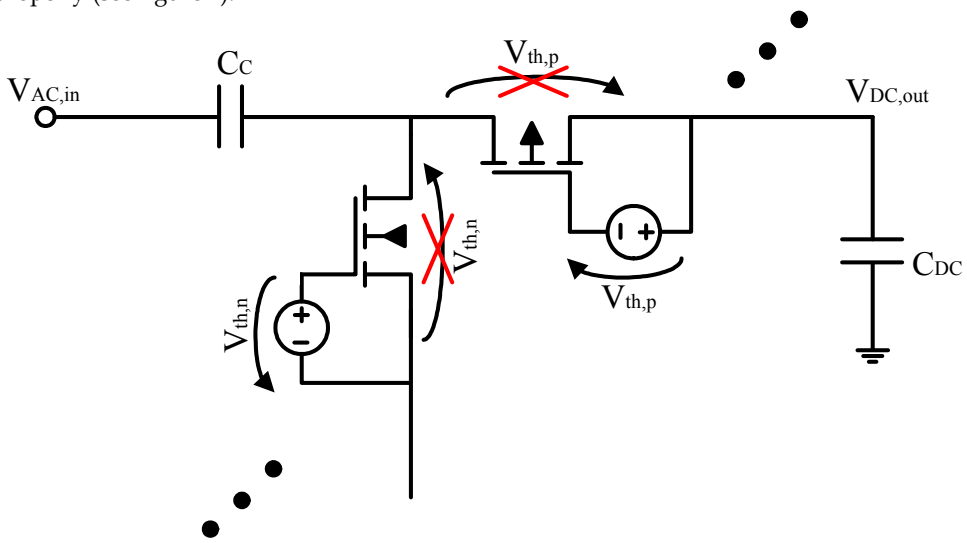


Fig. 6. rectifier stage with threshold voltage cancellation

Figure 8 shows the compensation voltage generator for NMOS transistors. It consists of a large resistor and a transistor diode M1 that is matched to the rectifying diode M2. Both diodes are designed to produce the same threshold voltage drop Vth.

The DC voltage at the anode of M2 is V_S. When the voltage at terminal V_B is larger than V_S+Vth, the compensation voltage at the gate of the rectifying diode equals one threshold voltage in a first order approximation, independent of V_B. When the diodes are matched, the compensation works independent of the temperature, the bulk-source voltage and process variations. The compensation of PMOS transistors works in an analog fashion.

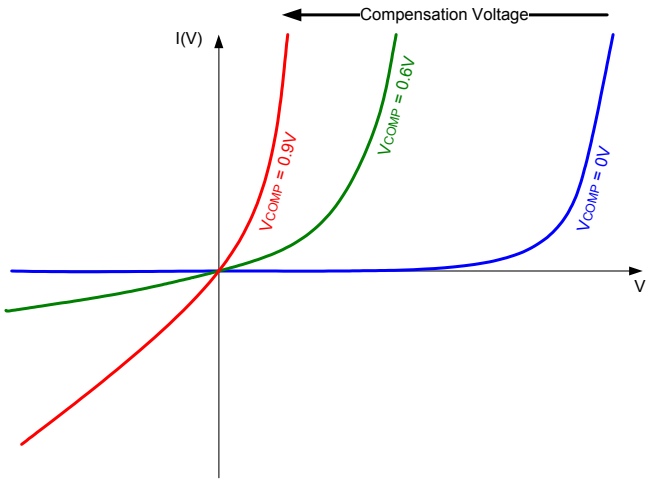


Fig. 7. I(V) characteristic of transistor diode with Vth compensation voltage

Figure 9 shows the complete rectifier circuit [Feldengut et. al., 2008]. It consists of two separate charge pumps, the first of which serves only as a compensation voltage generator (B) for the NMOS transistors in the main rectifier (A). The second rectifier (B) consists of eight stages with minimum area standard CMOS Schottky diodes. It can generate a large output voltage because it is almost unloaded. The output of this second rectifier is applied to the VB terminal of the compensation circuit in figure 8.

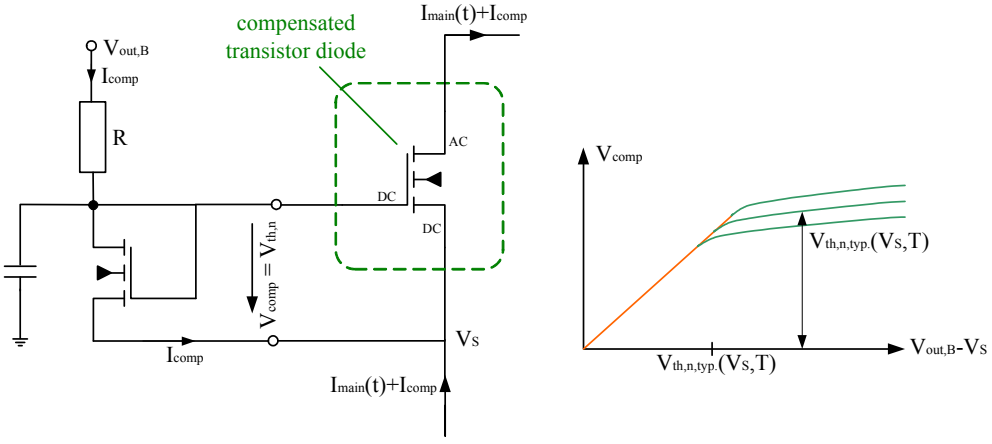


Fig. 8. compensation voltage generator

The total current consumption of the voltage dividers for the threshold voltage generation is less than 150 nA, while the output current of the six-stage main rectifier is typically several micro Amperes.

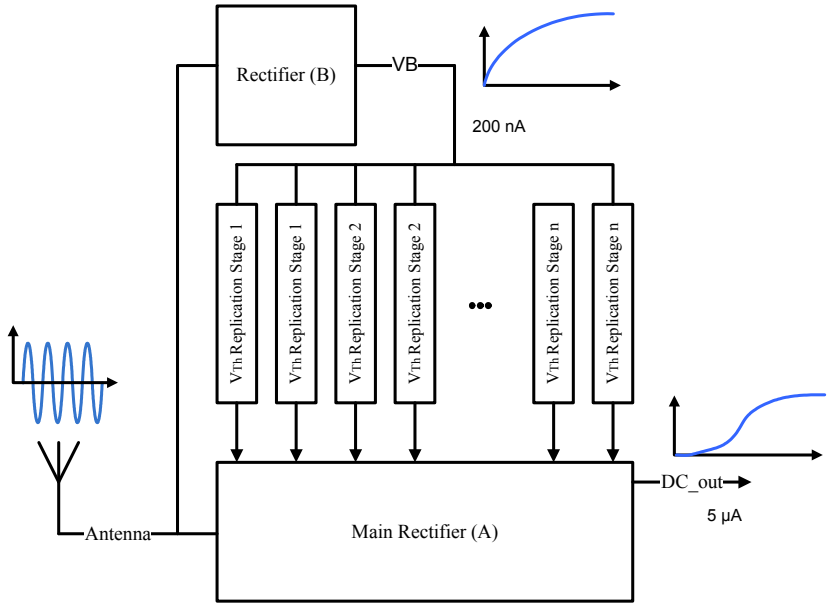


Fig. 9. proposed rectifier approach

The second rectifier (B) presents an additional load to the antenna. Its input capacitance and resistance appear in parallel to the main rectifier's input. The negative impact of this additional load is limited, because the input resistance is very large and the input capacitance is very small due to the minimum diode area and the low output current of rectifier (B). The circuit was implemented in a standard 0.35 µm CMOS process with Schottky diodes, double poly layers and high res poly resistors. The complete topology is shown in figure 10. Not all the voltage dividers for the threshold voltage reproduction are connected to the output of rectifier (B).

To reduce the current load and the required resistor size, the voltage dividers that compensate the lower stages of rectifier (A) are connected to intermediate output stages of rectifier (B). The voltage across the resistors is therefore very small. The compensation transistors have a much smaller aspect ratio, so that the voltage drop equals the threshold voltage across the rectification transistors, even when the current through the voltage dividers is several times smaller than the current flowing through the main rectifier stack (A).

Figure 11 shows the results for the conventional Schottky diode rectifier as well as for the proposed circuit. The load resistance is 300 kOhm and the output capacitor is 100 pF in both cases. The antenna resistance is 300 Ohm. At a distance of 4.5 m between the base station and the transponder, the input power is -11.3 dBm at a transmitted power of 2 W and a carrier frequency of 868 MHz. At this distance, the proposed rectifier (fig. 10) can power a transponder chip with 1.5 V supply voltage and 5 µA DC current, while the output voltage of the conventional circuit (fig. 5) is close to zero in the chosen process technology.

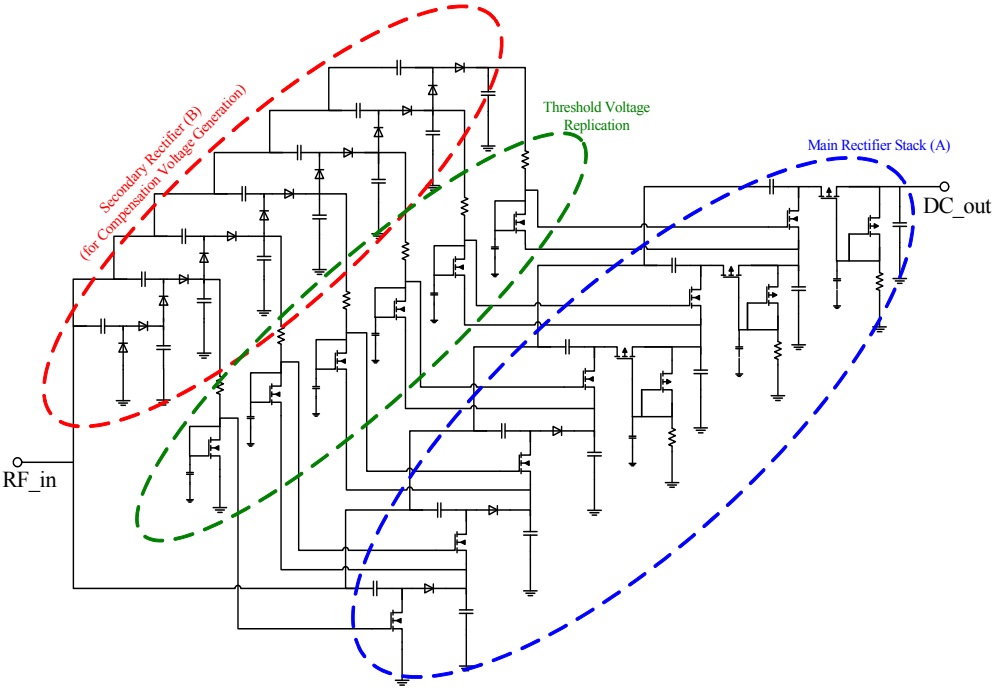


Fig. 10. complete circuit implementation

The transient start-up behaviour of the circuit is shown for different input voltages in figure 12. The output capacitor was reduced to only 20 pF in order to reduce the simulation time. The start-up waveform differs significantly from the typical capacitor loading waveform of a conventional diode multiplier. Once the compensation voltage has been build up, the rectifying transistors' efficiency is significantly increased, which changes the conversion efficiency. For very high output voltages of more than 2.5 V, some transistors are over compensated and begin to exhibit reverse leakage current. This leads to an abrupt stop of the output voltage increase.

Depending on the process technology, the number of stages may have to be reduced by one or two in each of the two rectifier stacks in order to reduce the input capacitance. The input capacitance has two negative effects: the first is that the bandwidth of the system is significantly reduced when the quality factor Q is high. The second issue with a large input capacitance is that it may also reduce the real part of the input impedance. When a large parasitic resistor lies in series to a large parasitic capacitance (this is often the case for substrate parasitics of diodes and capacitors in bulk CMOS), the equivalent parallel RC tank has a reduced resistance at the frequency of interest.

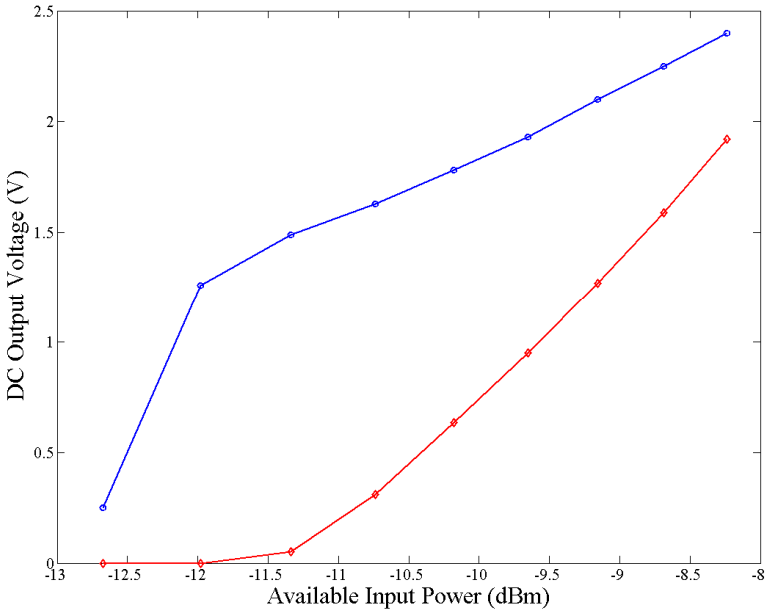


Fig. 11. Simulated output voltage as a function of input power under ideal matching conditions

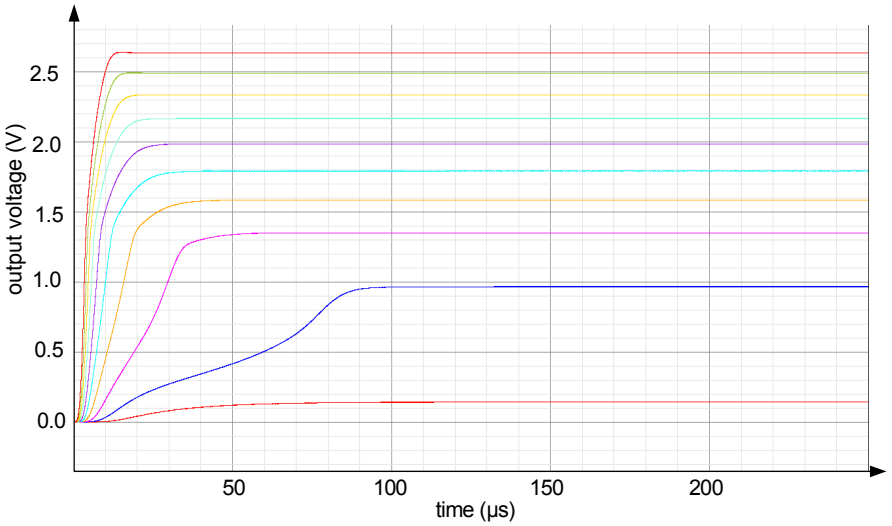


Fig. 12. simulation of transient start-up for different input voltages (reduced output capacitance to limit simulation time)

2.2 Reference and Temperature Sensor

The ADC and several other analog circuit blocks of a sensor transponder require precise reference voltages and currents that are insensitive to variations in the supply voltage, the temperature, and process variations. A low voltage bandgap reference circuit with low current consumption is implemented for this purpose [Razavi, 2001]; [Lee, 1998]. The topology is depicted in figure 13. The bandgap voltage reference core (middle) uses large high resistance poly resistors to limit the current in both branches to less than 1µA. These resistors have a negative temperature coefficient, so that the branch currents have a positive temperature coefficient (PTAT- Proportional To Absolute Temperature). A separate current reference circuit is required in order to obtain a temperature independent current. The V_{BE} of one of the PNP transistors is buffered and applied across another resistor with negative temperature coefficient, resulting in a nearly temperature-independent current.

The implementation of this circuit on a passive UHF transponder can be an issue, because the unregulated supply voltage from the rectifier (the input voltage for the reference) has a large dynamic range. The unregulated voltage is also very unstable due to the large output resistance and limited output capacitance of the rectifier. Furthermore, the required DC voltage level and the current consumption have to be reduced as far as possible in order to achieve long operating range. However, large resistor values and currents of less than 1µA lead to more mismatch, increased noise, and possibly stability issues. The operational transconductance amplifier provides limited gain and speed.

The reference circuit also serves as the temperature sensor because the voltage across the bipolar transistor is temperature dependant. The output signal is amplified and then converted by the ADC according to figure 2. Figure 14 shows the ADC input signal as a function of the temperature.

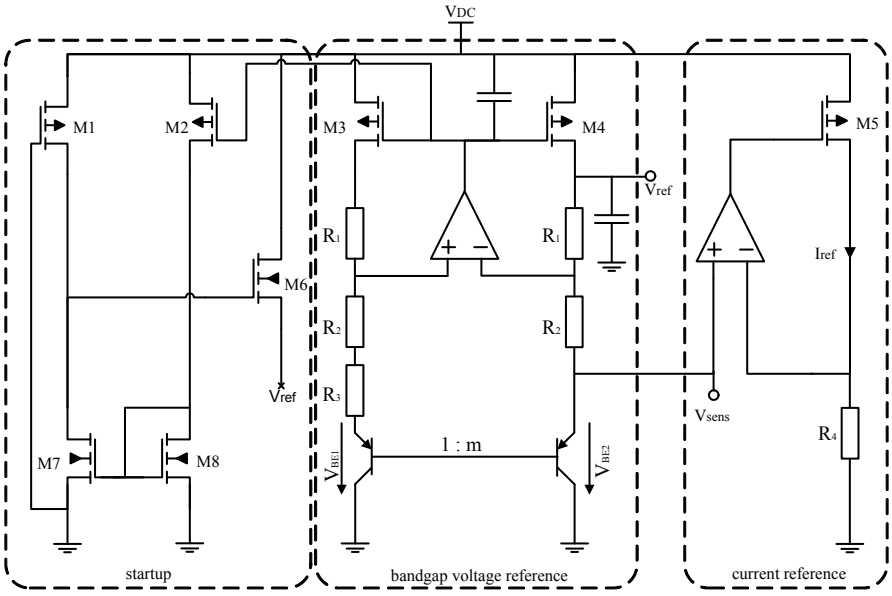


Fig. 13. Bandgap voltage and current reference

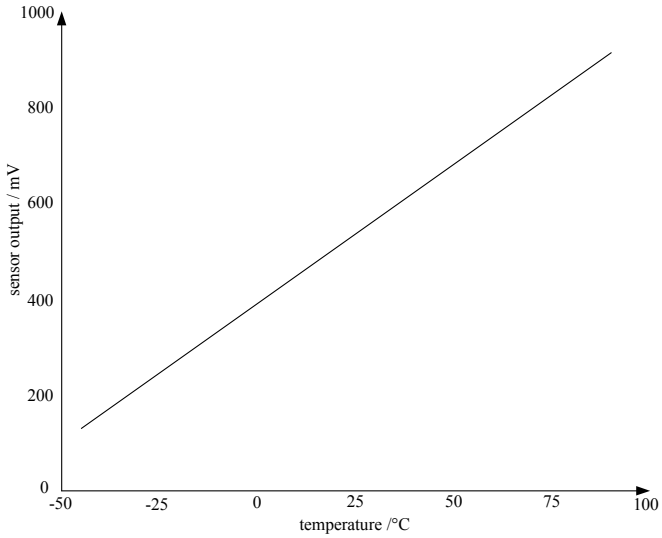


Fig. 14. output voltage of the temperature sensor after amplification

A low power successive approximation ADC is used to convert the sensor output to digital data. The operation principle is shown in figure 15. A digital value from the SAR register is converted to an analog value to be compared to the sampled input signal $V_{S/H}$. depending on which value is larger, the digital value in the register is either increased or reduced. After several cycles, the value of the SAR register is a digital representation of the analog input [Bechen, 2008].

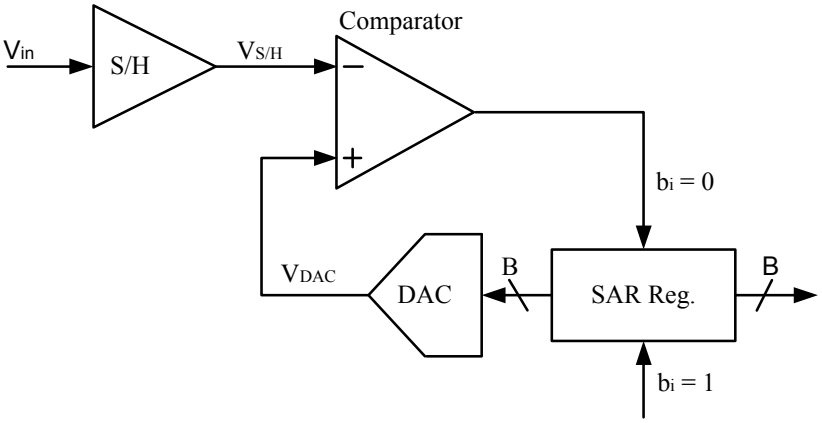


Fig. 15. SAR ADC architecture

Figure 16 shows the circuit implementation. The comparator is implemented using CMOS inverters. The first inverter is shortened from input to output to generate the middle voltage that determines the toggle threshold of the inverter. During the comparison phase, this

voltage is either increased or reduced, depending on the input voltage level. The DAC is implemented with a capacitive array to reduce the static current consumption compared to a resistive voltage divider. A scaling capacitor is connected between the MSB and the LSB to limit the total capacitor area [Bechen, 2008].

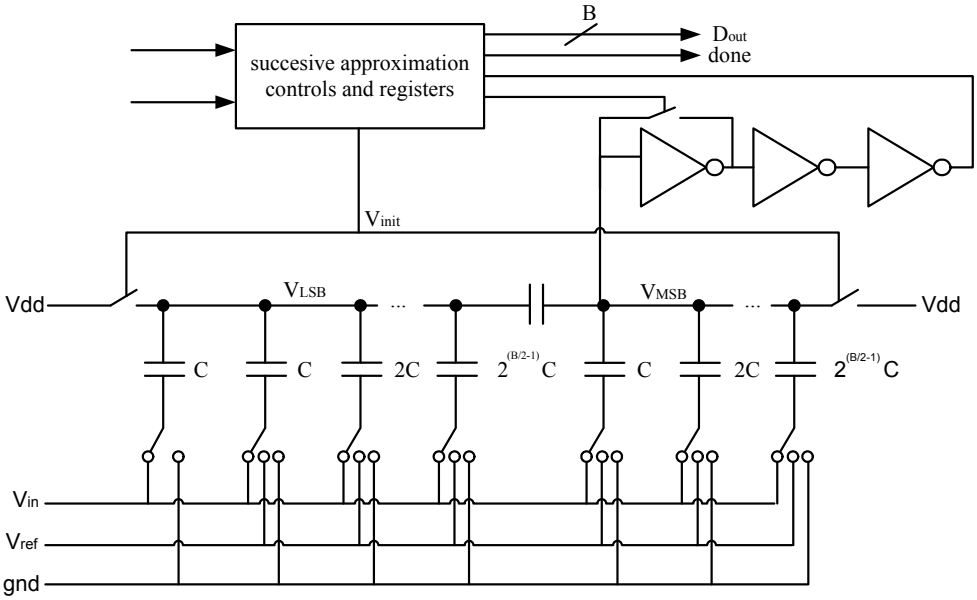


Fig. 16. SAR ADC circuit implementation for low power consumption

2.3 Demodulator and Clock Generator

Data transmission from the base station to the transponder is implemented using amplitude shift keying (ASK modulation). The shape of the antenna signal during communication is depicted in figure 17 ($V_{UHF,in}$). The amplitude of this signal varies with the distance between the transponder and the reader. A simple demodulator circuit (see figure 17) is used to extract the envelope and the average (or the delayed envelope) signal and to decide between the two logic states.

A small two stage multiplier that is loaded with a resistor extracts the envelope signal for the data frequency of 40 kHz. The circuit is similar to the main rectifier, but the diodes are very small so that the additional capacitive load that is presented to the antenna is not significantly raised. The envelope signal is fed into an additional low pass filter to extract the average value, which is different for each operating distance. The hysteretic comparator filters out noise and generates the logic signal for the digital part of the chip. The signals at the output of the envelope detector and the second low-pass filter are also shown in figure 17. Figure 18 shows the comparator circuit [7]. The unregulated supply voltage (VDC) is applied to the input stage to increase the common mode input range in close distance to the base station.

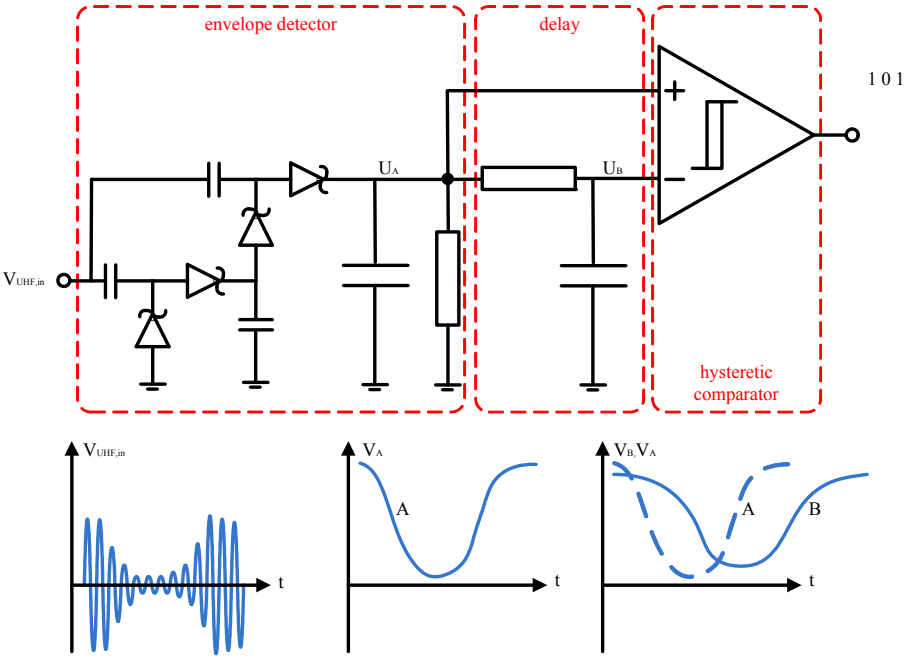


Fig. 17. Demodulator circuit

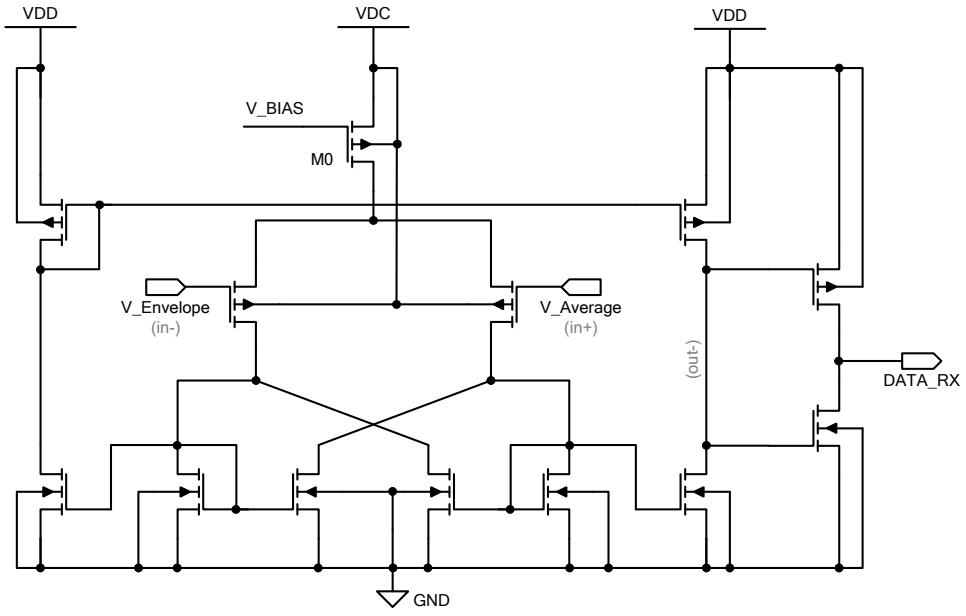


Fig. 18. hysteretic comparator circuit

In order to decode the data, the digital part also requires a clock signal that is several times faster than the data rate, but still at least two orders of magnitude smaller than the carrier frequency. This signal is generated by a local oscillator circuit. The relaxation type oscillator is shown in figure 19.

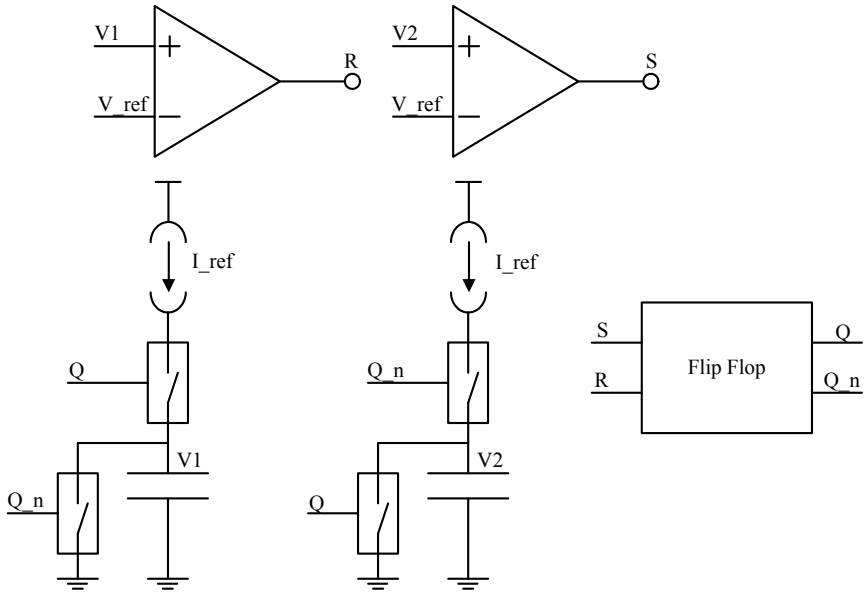


Fig. 19. low power relaxation type clock oscillator

Whenever the flip-flop is set, capacitor C2 is charged by a constant current while capacitor C1 is quickly discharged through transistor M1. The voltage at the input of comparator 2 rises linearly until it reaches V_ref. The flip-flop is reset, capacitor C2 is discharged through transistor M2 and capacitor C1 is charged. The advantage of this structure compared to a single capacitor design is that no hysteresis comparator is required in the oscillator and that the discharge time has no influence on the output frequency. The total current consumption of the oscillator is 400 nA at a frequency of 1 MHz. The frequency variation is mainly determined by the accuracy of the reference current, the capacitor accuracy, and the comparator delay. The comparator delay causes the capacitor voltage to peak above the reference voltage according to figure 20. This delay depends on process and temperature variation and is not controlled very well. When high frequencies are required the comparator current needs to be increased to reduce the delay in relation to the total oscillation period time. For high data rates above 100 kHz an oscillator frequency of 1.6 MHz is usually required. A ring oscillator circuit has the advantage of less current consumption at high frequencies. However, for the required data rate of 40 kHz, the relaxation design offers improved accuracy at lower oscillation frequency.

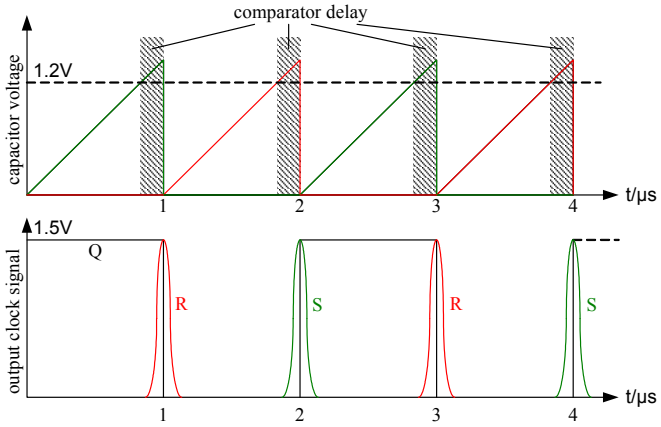


Fig. 20. internal oscillator waveforms

3. Conclusion

Wireless power transmission for sensor transponders in the electromagnetic far field is feasible. The architecture of the transponder circuits is more complex and requires more supply voltage and power than simple RFID transponders. The requirements for the air interface and the analog front-end are therefore more stringent. The voltage multiplier is the most critical circuit block concerning the power conversion efficiency and the maximum operating range.

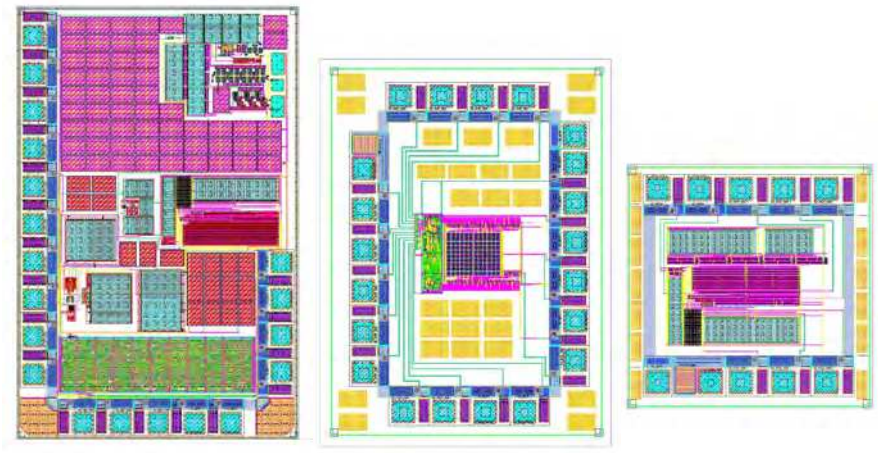


Fig. 21. layout of the analog front end, the ADC, and the sensor (left to right)

A rectifier has been presented that reduces the threshold voltage drop across rectifying devices. It uses a secondary unloaded voltage multiplier to generate a high DC voltage at low input amplitude. This voltage is used to generate the bias voltage for the rectifying

transistors in the main power rectifier stack. The minimum required input voltage and the efficiency of the main rectifier is therefore reduced compared to the conventional Schottky diode rectifier. Three transponder test chips have been developed that contain all required analog circuits including the front-end, the sensor and a low power ADC.

4. References

Bechen, B. (2008). "Systematischer Entwurf analoger Low-Power Schaltugnen in CMOS anhand einer kapazitiven Sensorauslese" (German), Fraunhofer IRB Verlag, Germany, 2008

Curty, J.-P. ; Declercq, M. ; Dehollain, C. & Joehl, N. (2006). "Design and Optimization of Passive UHF RFID Systems", Springer 2006, Germany

Feldengut, T.; Wang, J. ; Kolnsberg, S. & Kokozinski, R. (2008). "An Analog Front End for a Passive UHF Transponder With Temperature Sensor" Proceedings of the Microwave Conference, EuMC, 38th European

Finkenzeller, K. (2003) RFID Handbook, Radio Frequency Identification Fundamentals and Applications. 2nd ed. New York: Wiley, 2003

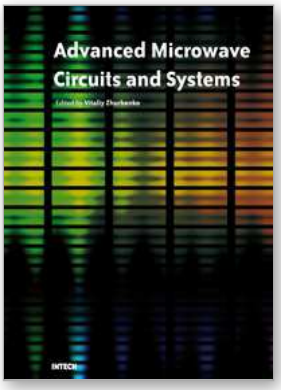
Karthaus, U. & M. Fischer (2003). "Fully Integrated Passive UHF RFID Transponder With 16.7 μW Minimum RF Input Power" IEEE J. Solid State Circuits, vol. 38, no. 10, pp. 1602-1608, Oct 2003.

Lee, T. H. (1998) "The Design of CMOS Radion Frequency Integrated Circuits" , Cambridge University Press, Cambridge, UK

Nakamoto, H. ; Yamazaki, D. ; Yamamoto, T. ; Kurata, H. ; Yamada, S. ; Mukaida, K. ; Ninomiya, T. ; Ohkawa, T. ; Masui, S. & Gotoh, K. (2006). "A Passive UHF RFID Tag LSI with 36,6% Efficiency CMOS Only Rectifier and Current Mode Demodulator in 0,35 μm FeRAM Technology" Proceedings of the International Solid State Circuits Conference, ISSCC, Session 17, 2006

Razavi, B. (2001) "Design of Analog CMOS Integrated Circuits", McGraw-Hill, New York, NY

Umeda, T. ; Yoshida, H. ; Sekine, S. ; Fujita, Y. ; Suzuki, T. & Otaka, S. (2005). "A 950 MHz Rectifier Circuit for Sensor Networks with 10 m Distance Proceedings of the International Solid State Circuits Conference, ISSCC, Session 14, 2005.



Advanced Microwave Circuits and Systems

Edited by Vitaliy Zhurbenko

ISBN 978-953-307-087-2
Hard cover, 490 pages
Publisher InTech
Published online 01, April, 2010
Published in print edition April, 2010

This book is based on recent research work conducted by the authors dealing with the design and development of active and passive microwave components, integrated circuits and systems. It is divided into seven parts. In the first part comprising the first two chapters, alternative concepts and equations for multiport network analysis and characterization are provided. A thru-only de-embedding technique for accurate on-wafer characterization is introduced. The second part of the book corresponds to the analysis and design of ultra-wideband low- noise amplifiers (LNA).

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821