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Current reuse topology in UWB CMOS LNA

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1. Introduction

In February 2002, the Federal Communications Commission (FCC) gave the permission for the marketing and operation of a new class of products incorporating Ultra Wide Band (UWB) technology. The early applications of UWB technology were primarily radar related, driven by the promise of fine-range resolution that comes with large bandwidth. But the recent 3.1-10.6GHz allocation extends the UWB use to a larger application area for which the specific frequency ranges are reported in the table 1.

Class/Applications	Frequency band for operation at part 1 limit
Communications and measurement systems	3.1 to 10.6GHz (different out-of-band emission limits for indoor and outdoor devices)
Imaging: ground penetrating radar, wall, medical imaging	< 960MHz or 3.1 to 10.6GHz
Imaging: through wall	< 960MHz or 1.99 to 10.6GHz
Imaging: surveillance	1.99 to 10.6GHz

Table I. FCC allocations for each UWB category [1]

In this work we will focus on communication applications for which maximum emissions in the prescribed bands are at an effective isotropic radiated power (EIRP) of −41.3 dBm/MHz or a maximum peak power level of 0dBm/50MHz, and the −10 dB level of the emissions must fall within the prescribed band. Hence UWB signal transmissions must respect the spectrum mask presented in the figure 1 for the 7.5GHz here considered bandwidth.
Unlike narrow band standards located within the 0.9 to 6 GHz range, UWB technology can meet the growing demand for high data rate communications in short range distance with relatively low power consumption. Several Gigabits per second (Gbps) are expected within a 5 meter range [2][3]. However targeting mass market applications its deployment success is first driven by a low cost implementation. To meet this requirement CMOS technology is a promising candidate. From technical point of view the digital part obviously benefits from Moore's law, but scaling of the CMOS devices with increasing f_T and f_{max} also facilitates the processing of large bandwidth analog signals with low power.

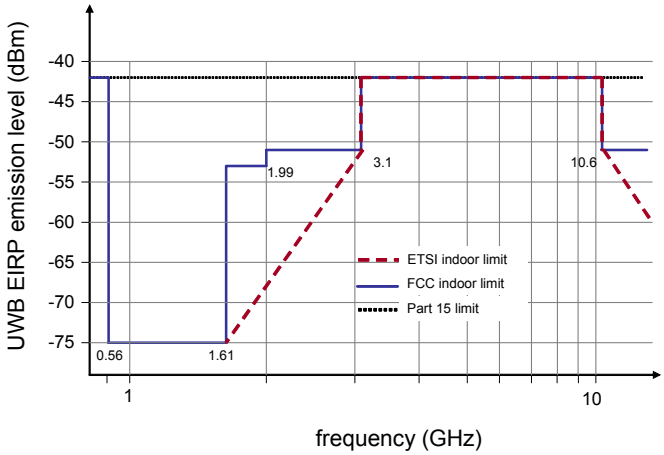


Fig. 1. UWB spectral mask for indoor communication systems [1]

Furthermore full CMOS wireless transceivers are often limited by output power capability of active device. The UWB spectral mask presented in the figure 1 relaxes such constrain enabling the use of CMOS PA. Hence the single chip solution becomes feasible with UWB technology.

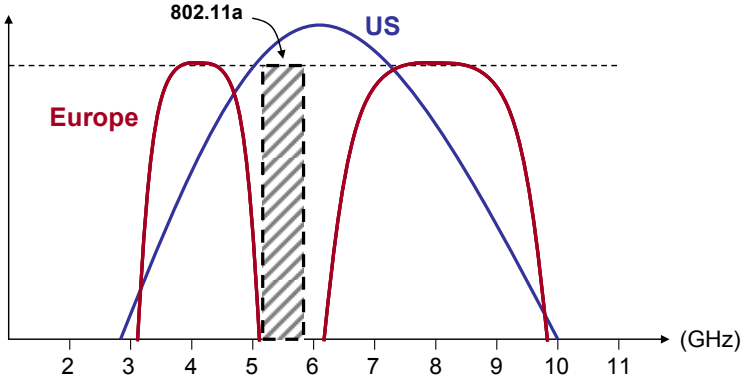
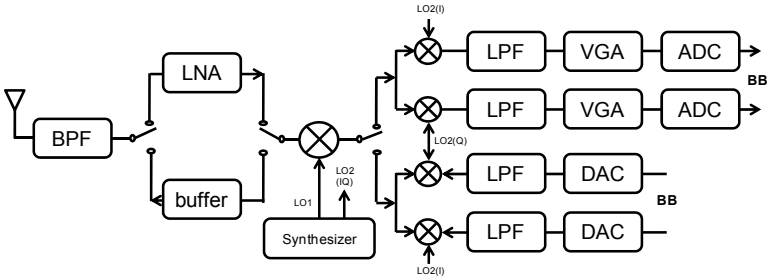


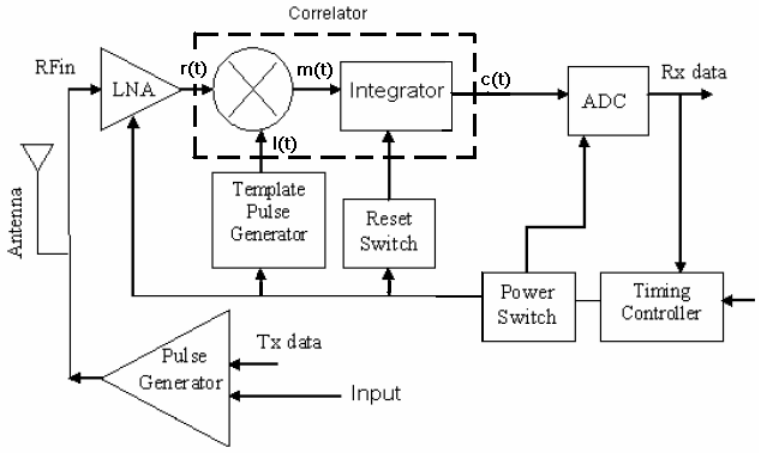
Fig. 2. UWB spectrum redrawing for US (blue) and Europe (red)

UWB allocation shares frequency spectrum with other wireless applications. As well the redrawing of the 3.1-10.6GHz band depends on the local regulation. For example, the entire 7.5GHz bandwidth, red line in the fig. 2, is used in US. In Europe, it is split in two bands, blue lines in the fig. 2: the lower from 3.1 to 5.1 GHz and the upper band from 6.4 to 10.6 GHz because of the 802.11a application which is located within the 5.15 to 5.725 GHz range. Currently, there are two major IEEE UWB radio schemes, i.e., multi-band (MB) OFDM [4]and direct sequence (DS), both dividing the 7.5GHz UWB bandwidth into multiple sub-bands, and use carrier in radio transmission. An alternative UWB radio solution, fig. 3(b),[5], is a fully pulse-based, non-carrier, single-band (7.5GHz), most-digital, all-CMOS UWB

transceiver that can take the full advantages of the original impulse UWB radio technology to achieve the required multi-Gbps throughput.



(a)



(b)

Fig. 3. MB-OFDM receiver [4] *(a)* pulse-based UWB transceiver [5] *(b)*

Whatever the radio scheme that is selected, both kinds of receiver architectures require a Low Noise Amplifier (LNA) after the antenna. This critical building block must exhibit a low return loss, a low noise figure, and a high gain across the entire frequency band of interest. These characteristics are mainly supported by the input matching skills of the circuit. As well the fig. 4 proposes some simplified schematics for the most common UWB LNA topologies. The two first, LC filter cascode [6], fig. 3(a), and transformer feedback [7][8], fig. 4(b), involve the transistor gate to source capacitance (C_{gs}) in the synthesis of a pass-band filter. Both architectures, sensitive to technology modeling, remain the best suited to achieve broadband operation, in term of gain, input matching, and low noise figure under low power consumption. Considering the implementation, the large number of inductor required to set up these techniques induces a huge, and so expensive, silicon area. The two last configurations resistive feedback (FB) [9][10] and common gate (CG) [11], fig. 4(c) and (d) respectively, offer a very compact silicon alternative. However resistive FB amplifier is

known for large current consumption and stringent gain-bandwidth trade-off inducing limited optimization. Basic CG topology can perform wideband response at the expense of increased noise figure (NF). The input impedance is so dominated by the trans-conductance once the input gate to source capacitor is cancelled out within the considered bandwidth [12].

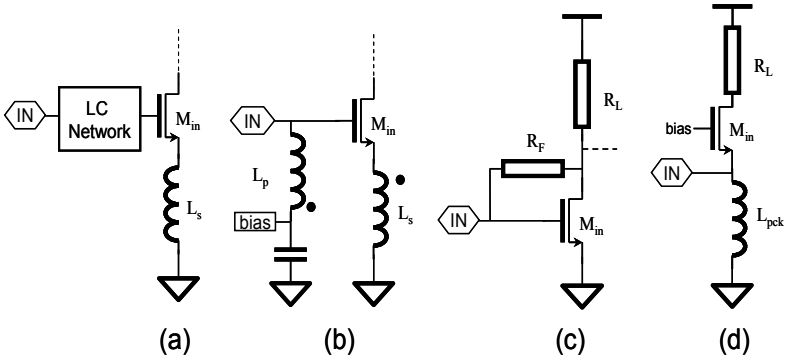
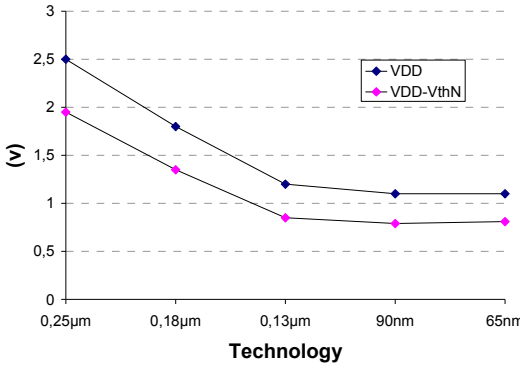


Fig. 4. Four basic topologies of UWB LNA input matching

For a couple of decade CMOS technologies scaling has induced a drastic reduction of the supply voltage reported in the fig. 5. From analog point of view, a meaningful figure of scaling impact is the threshold to supply margin (VDD-VthN). Indeed, it determines the number of devices that can be stacked between the two supply rails thus steering the design methodology and constrains.



TECHNOLOGY	SUPPLY (VDD)	V_{THN}	VDD-V_{THN}
0.25µm	2.5V	550mV	1.95V
0.18µm	1.8V	450mV	1.35V
0.13µm	1.2V	350mV	0.85V
90nm	1.1V	310mV	0.79V
65nm	1.1V	290mV	0.81V

Fig. 5. CMOS scaling impact on VDD and V_{th}

In RF designs it defines the maximum allowed headroom voltage which is directly connected to the linearity, the gain, and the signal to noise ratio (SNR) of the building blocks. As a matter of consequence UWB LNA performances greatly suffer from voltage scaling in deep sub-micron CMOS technologies. Considering such context this work proposes a new circuit technique making the aforementioned UWB topologies low voltage compatible.

2. Resistive feedback input matching

2.1 Resistive feedback theory

The single stage wide band amplifier, proposed in fig. 4(c), can be studied according to the simplified small signal model depicted in fig. 6. Where g_{mMin}, C_{gsMin} and C_{gdMin} are the transconductance, gate to source and drain to source capacitors of M_{in} respectively. R_L and R_F are load and feedback resistances. We assume that the circuit is connected to a source generator whose the R_s impedance is typically 50 Ω.

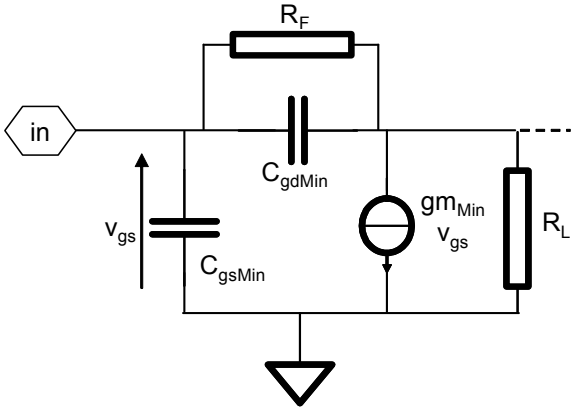


Fig. 6. Simplified model of a resistive feedback input stage

In first approximation, we can derive the analytic expressions of the voltage gain (A_v), noise figure (NF) and input impedance (Z_{in}) as:

$$\left|A_v\right| \approx g_{m_{M_{in}}}.(R_L \,//\, R_F) \tag{1}$$

$$NF \approx 1+\frac{2}{3}\frac{1}{g_{m_{M_{in}}}R_S}.\left(\frac{1}{R_S}+\frac{R_S}{R_F{}^2}\right)+\left(\frac{f}{f_{T_{Min}}}\right)^2.\frac{2}{3}g_{m_{Min}}R_S+\frac{R_S}{R_F} \tag{2}$$

$$Z_{in} \approx \frac{R_F + R_L}{1+\left|A_v\right|} \tag{3}$$

In a -3dB bandwidth (BW_{-3dB}) defined as it follows:

$$BW_{-3dB} \approx \frac{1+|A_v|}{R_F C_{gs_{M_{in}}}} \tag{4}$$

With f_{TMin} the cutoff frequency of M_{in}.
From (1) it comes a high voltage gain requires a large g_m and, or, a large load resistor R_L. But the square law of current drain in CMOS transistors implies an expensive DC current to significantly increase the transconductance thus limiting the gain improvement through g_m in wireless applications. Concerning R_L it is limited by biasing conditions since it must keep M_{in} in saturation region. Hence moderate gains are performed with this kind of topology. In expression (2) the larger the R_F is the lower the NF is. But R_F is limited in (3) for a fixed input impedance, typically 50Ω, and contributes to the bandwidth tuning in (4), a roughly 10GHz in UWB applications. So to estimate the capability of such amplifier configuration to address UWB requirements, the expressions (1) to (4) have been drawn, fig. 7, based on 0.13µm CMOS skills.

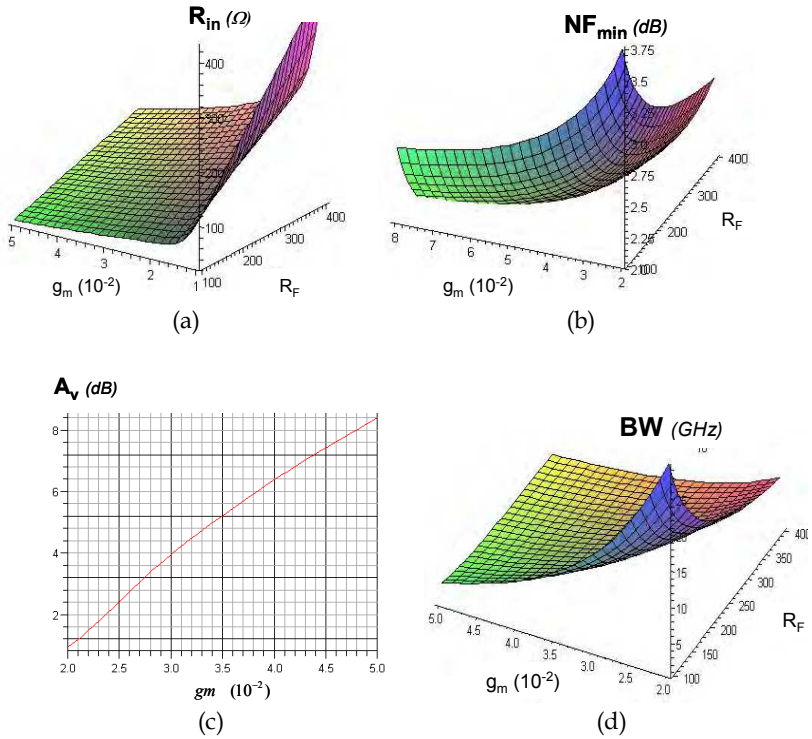


Fig. 7. Re(Zin) (a) NFmin (b) Av (c) and Bandwidth (d) of single stage resistive feedback amplifier with typical 0.13µm CMOS technology skills. VDD=1.6V

Considering a 50Ω input impedance in fig. 7(a), the transconductance, g_m, and the feedback resistance, R_F, must be tuned to 30 mS and 130 Ω respectively. Under such conditions a roughly 3 dB NF_{min}, fig. 7(b), and 4 dB voltage gain, fig. 7(c), are performed. According to

Friis formula [10], this available gain cannot ensures a low NF_{min} to the front end. To overcome this drawback we can either implement a multi-stage LNA either design a mixer performing both a low noise figure and a high gain. The first solution is power hungry and so unexpected for wearable applications. The second puts on the mixer some hard design constrains. Hence these preliminary investigations emphasize that a conventional resistive feedback topology is unsuited for UWB LNA design in a 0.13µm CMOS implementation.

2.2 Current reuse improvement

It has been demonstrated in the previous part that the lack of gain is the bottleneck of resistive feedback amplifier optimization. The current reuse topology relying on active load configuration can complete this missing. Indeed both improving the voltage gain and lowering the design trade-off, this technique makes resistive feedback topology more attractive for ultra wide band purpose.

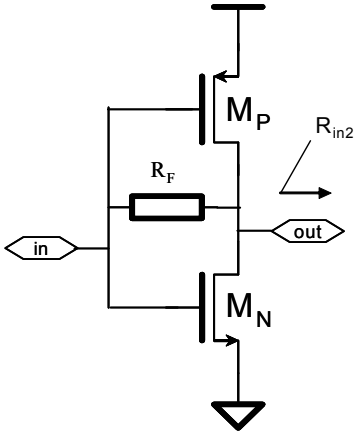


Fig. 8. resistive feedback current reuse configuration [12]

Considering the topology depicted in fig. 8, the overall trans-conductance is now ($g_{mN}+g_{mP}$) that is twice larger the basic resistive feedback one for the same biasing current. Loading the NMOS transistor with the PMOS allows the circuit to operate under lower supply voltage than resistive load configuration. As well the expressions *(1)*, *(2)*, *(3)* and *(4)* remain the same according to the equivalences reported in the Table II:

RESISTIVE FEEDBACK	REUSE FEEDBACK
C_{gsMin}	$C_{gsN}+C_{gsP}$
C_{gdMin}	$C_{gdN}+C_{gdP}$
R_L	$R_F//r_{dsN}//r_{dsP}//R_{in2}$
$\mathbf{g_{mMin}}$	$\mathbf{g_{mN}+g_{mP}}$

Table II. resistive to reuse feedback equivalence table

With R_{in2} the input impedance of the following stage. In reuse approach, R_F remains large to lower NF in *(2)* where as g_m boosting achieves a high A_v for a reasonable current consumption in *(1)*. Hence the growth of A_v mitigates the increase of parasitic capacitor value to keep a wide -3dB bandwidth in *(4)*.

Measurement results

The schematic of the LNA is depicted in fig. 9. A 0.7nH input inductor is added to compensate for the parasitic capacitors of M_N and M_P at high frequencies. A resistive feedback buffer with peaking inductor load is coupled with the reuse UWB stage to drive the 50Ω output load.

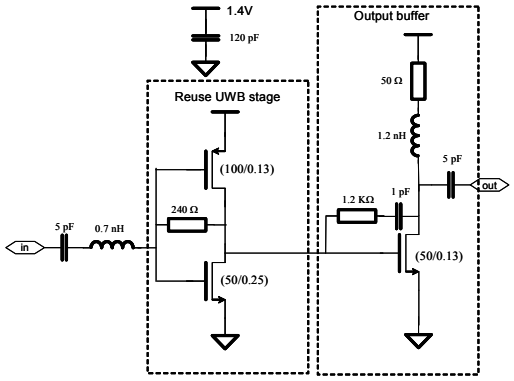


Fig. 9. UWB resistive feedback current reuse LNA [11]

This circuit is implemented in a 6 metal levels 130nm CMOS technology from STM. The measurement results have been performed with a GSG probe bench combined with a HP 8510B network analyzer and a HP 8970 NF-meter.

The reuse input stage, in charge of NF and input matching, depicts, in fig. 10, its ability to achieve a wide band input matching. Indeed S_{11}, in good agreement with simulations, is kept lower than -12dB from 1 to 14.8 GHz.

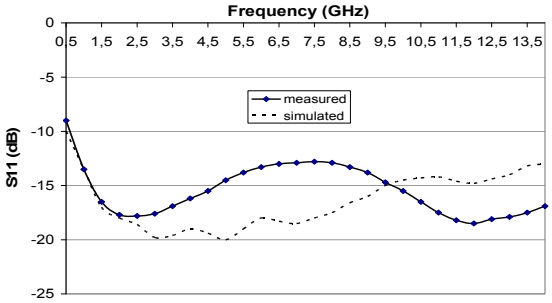


Fig. 10. Measured x Simulated S_{11} parameter

As far as noise is concerned, both NMOS and PMOS of the current reuse stage are sized to provide the lowest NF at 3.6GHz -i.e. a good tradeoff regarding to the 3 to 11 GHz frequency band of interest-. However resistive amplifier is not well suited to synthesize the imaginary part required by the noise matching of MOS transistor, especially over a wide bandwidth. For this reason, such kind of topology remains noisier than its LC ladder counterpart [9]. According to the expression *(2)*, the high f_T of the 130nm MOS technology combined with a large R_F feedback resistor keeps the NF lower than 9dB up to 10 GHz thus addressing UWB requirement. It reaches a 4.45dB minimum at 3.74GHz, as showed in the fig. 11.

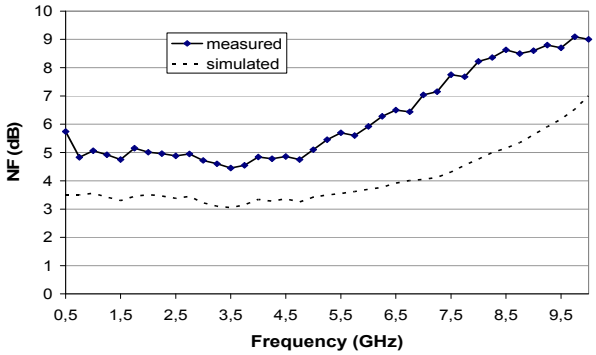


Fig. 11. Measured x Simulated Noise Figure

In fig. 12, an 11.5dB quasi flat band gain is provided from 2 to 9 GHz. This gain is entirely performed by the current reuse stage which consumes a 17mW under 1.4 supply voltage. The buffer does not provide additional gain it both compensates for the roll-off induced by C_{gsMin} in the previous stage, with the 1.2 nH peaking inductor, and delivers the signal to the 50Ω load.

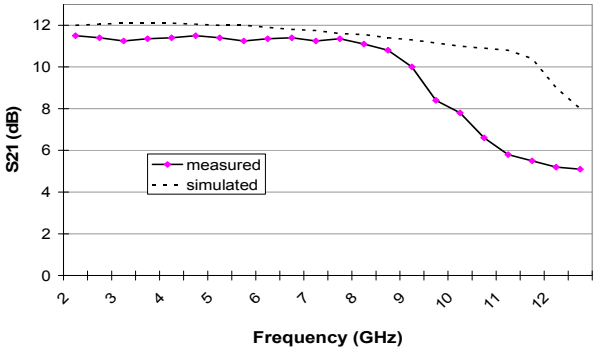


Fig. 12. Measured x Simulated S_{21} parameters

Fig. 13, depicting S_{21} and NF_{min} variations versus supply voltage emphasizes the ability of the current reuse topology to operate under low supply voltage. The sweep range is lower

limited to 0.9V since the input matching is not completed below. A roughly 6dB gain 5.5 dB NF_{min} are achieved under 1V. Whereas the gain is voltage dependent, the minimum noise figure is almost constant, close to 4.5dB, until 1.1V supply. For lower supply voltages the gain drop-off mainly contributes to the noise figure growth. According to expression (4) it has been also observed that the bandwidth slightly shrinks with the voltage decreasing, it covers a 2 to 8GHz range under 1V.

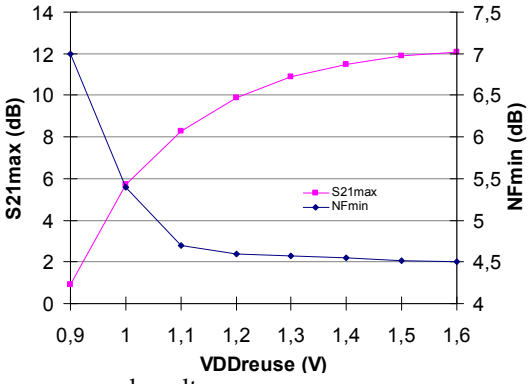


Fig. 13. S_{21} and NF_{min} versus supply voltage

The -1dB input compression point is reported in fig. 14. The supply reduction first limits the allowed voltage swing at the output of the current reuse stage thus degrading the ICP1. For sub-1V operation the serious lack of gain permits larger power processing.

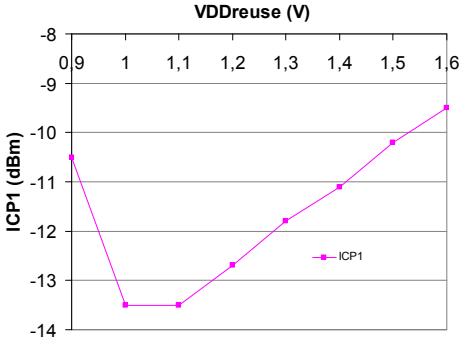


Fig. 14. ICP1 versus supply voltage

3. LC ladder input matching

Another useful technique to perform wide band input matching in UWB LNA is the filter synthesis. This solution is interesting since it achieves a pass band filtering instead of a wide band response like resistive amplifiers do. Out-band blockers are so attenuated thus relaxing the linearity and power consumption constrains of the LNA. The synthesis is based on LC elements, the larger the number of cascaded cells is the wider and better the filtering

is. But inductors are silicon expensive, so designers have to deal with input matching level and bulk management. Fourth and sixth order topologies are good trade-off in UWB applications.

3.1 LC ladder theory

The LC network presented in fig. 15(a) is a 6th order pass-band filter whose the impedance response, Zin, is depicted in fig. 15(b). Hence Zin is purely resistive within a frequency range defined as it follows:

$$f_L \sim \frac{1}{2\pi RC_2} \sim \frac{R}{2\pi L_1} \tag{5}$$

$$f_U \sim \frac{1}{2\pi RC_1} \tag{6}$$

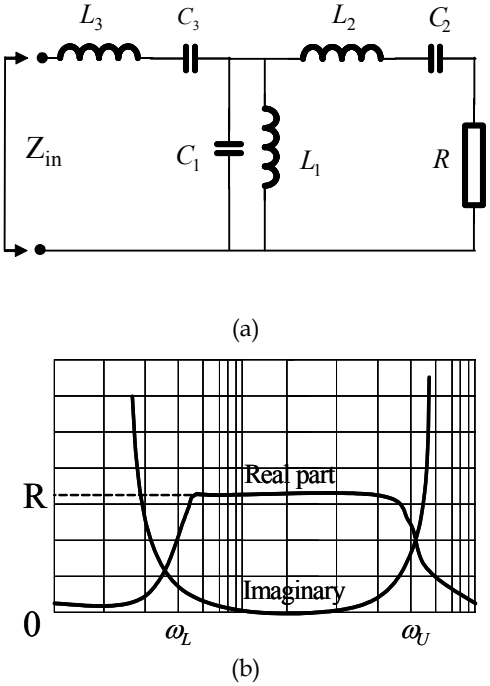


Fig. 15. 6th order pass-band filter form [8] (a) Z_{in} response (b)

This input matching configuration is often implemented in UWB LNA in accordance with the schematic reported in fig. 16. The circuit proposed in fig. 16 has been implemented in a 0.25µm SiGe BiCMOS technology [10].

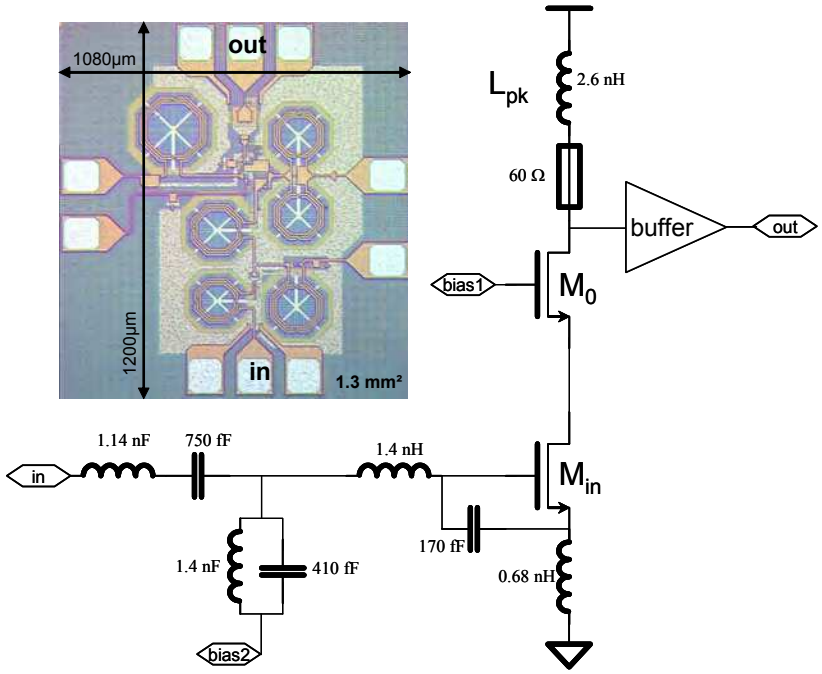


Fig. 16. UWB LC ladder cascode LNA [13]

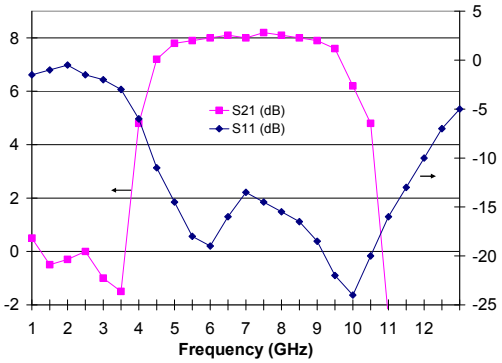
The roll off induced over the gate to source capacitor of M_{in} is compensated by L_{pk} peaking load inductor to perform a quasi flat band voltage gain, G_v, expressed as:

$$G_v = \frac{g_{m M_{in}}[r_{pk} + jL_{pk}\omega]}{2R_S.jC_{GS\,tot}\omega} \tag{7}$$

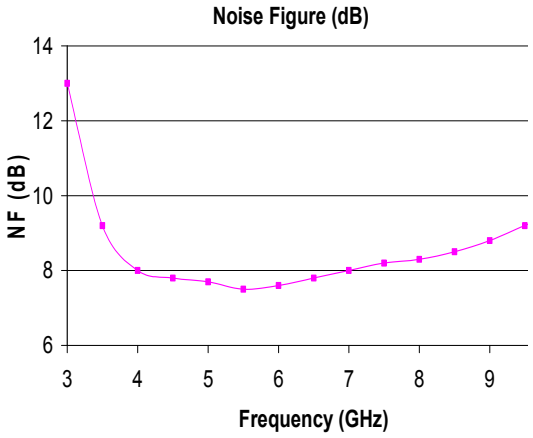
Close to the geometric average frequency $(f_L.f_U)^{0.5}$, the minimum noise figure, based on narrow band derivation described in [10], is written as :

$$NF_{\min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{g_{\min}} C_{GStot} \sqrt{\gamma.\delta.(1-|c^2|)} \tag{8}$$

With C_{GStot} the combination between M_{in} gate to source and 170 fF external capacitors, g_{mMin} the transconductance of M_{in}, $\gamma = 3/2$, c is the correlation term equals to j0.395, and δ is the coefficient of gate noise equals to 4/3.



(a)



(b)

Fig. 17. S_{21} and S_{11} versus frequency *(a)* NF versus frequency *(b)*

Operating under 2.5V, it achieves a 8,5 dB maximum gain, fig. 17(a), with a 8,5 mW power consumption. S_{11} remains lower than -10dB from 4.2 to 12 GHz thus depicting a very wide band input matching. The NF, fig. 17(b), smoothly increases from 7.5 dB@5.6GHz to 9.5 dB@9.8GHz. The measurement results of the circuit are summarized in Table III.

S_{11} (DB) [BW IN GHZ]	<-10 [4,2-12]
S_{21} (dB) [BW-3dB in GHz]	8.5 [4.4-10.6]
NF (dB)	7.5/9.5
Pdiss core (mW)	8.5
Area (mm²)	1

Table III. 0.25µm UWB LC ladder cascode LNA performances

The 4th order LC ladder LNA topology presented in the fig. 18 has been implemented and simulated in a 0.13µm CMOS technology. Two circuits have been designed according to the table IV, they perform a more than 10dB gain and a good input matching over the targeted bandwidth as showed in fig. 19. Supplied under 1.6V they roughly consume a 5mA.

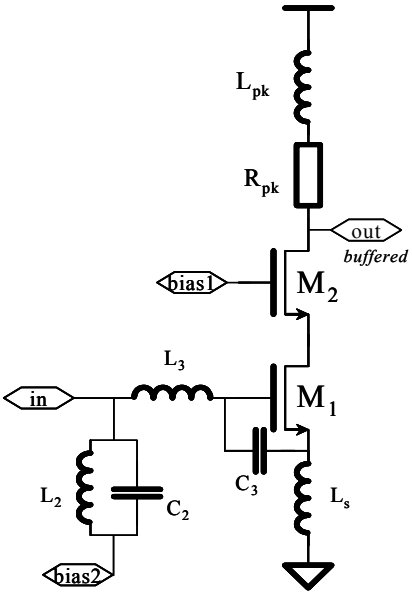
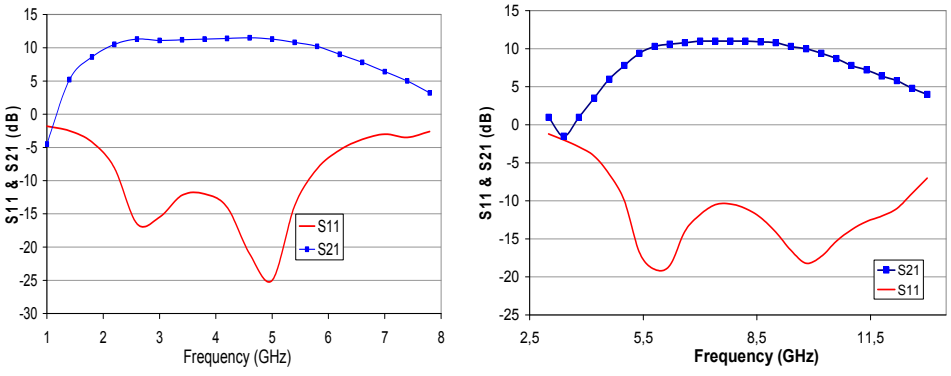


TABLE IV. DEVICE SIZES FOR 3-5GHZ AND 6-10GHZ

	3-5 GHZ	6-10 GHZ
L_2/C_2	*1.9nH/400fF*	*0.6nH/70fF*
L_3/C_3	*2.2nH/520fF*	*1.4nH/130fF*
L_S	*1.1nH*	*1.1nH*
$(W/L)_{M1}$	*40/0.13 µm*	*40/0.13 µm*
$(W/L)_{M2}$	*60/0.13 µm*	*50/0.13 µm*
R_{pk}	*50Ω*	*35Ω*
L_{pk}	*3nH*	*2nH*

Fig. 18. 4th order LC ladder LNA dedicated to 3-5GHz or 6-10GHz bands



(a) (b)

Fig. 19. Simulated S_{11} and S_{21} of a 4th order LC ladder cascode LNA dedicated to 3-5GHz *(a)* and 6-10GHz *(b)*

A wide band operation requires from active devices a large current consumption to ensure a sufficient high cutoff frequency. This means that the gate overdrive voltage of M_1 and M_2, fig. 18, must be selected within a 0.3 to 0.5V range, according to [17], thus limiting the minimum supply voltage of cascode topology compared to a narrow band design issue. The gain to VDD dependency is drawn in fig. 20 for the 6 to 10GHz circuit. A less than 10dB gain is achieved with the technology nominal voltage, 1.2V, and then it severally decreases for sub 1V operations.

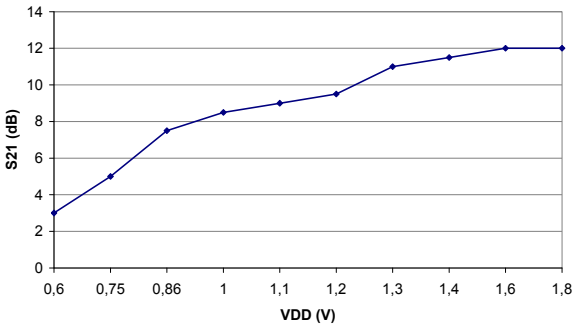


Fig. 20. 4th order LC ladder LNA gain versus supply voltage

So LC ladder network synthesis is a very efficient technique to perform wide band input matching in LNA designs. But the cascode topology would suffer from technology scaling in the near future because of supply voltage reduction. To find an alternative we investigate the combination of LC ladder with current reuse configuration.

3.2 Current reuse improvement

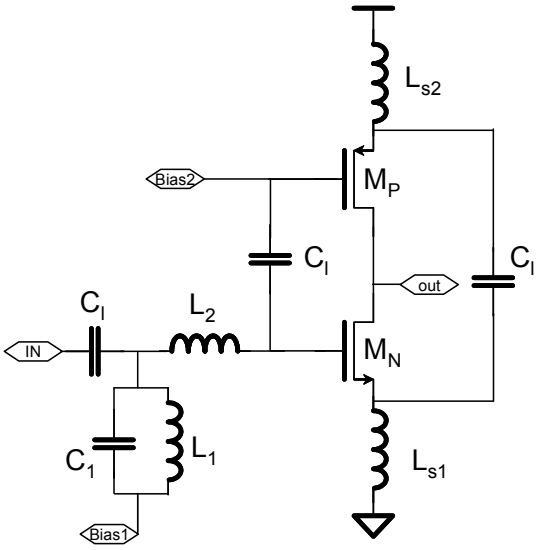


Fig. 21. LC ladder current reuse configuration

The theoretical topology of a LC ladder current reuse LNA is presented in fig. 21. It is here combined with a 4th order LC ladder filter and four inductors are needed for the synthesis. C_l shunting the two sources of the transistors in AC mode, Ls1 and Ls2 are in parallel and achieve the real part of the input impedance. The configuration of active load improves the voltage gain compared to a cascode topology.
The minimum supply voltage, keeping both the PMOS and NMOS transistors in saturation region, is derived in expression (9). It is drawn in the Fig. 22 based on the features of a 0.13µm CMOS technology. W_p is adjusted to 30 µm which implies a C_{gstot} equals to 300fF intended for 6 to 10 GHz range. It points out the ability of current reuse topology to sustain low voltage operation.

$$VDD_{\min} = \sqrt{\frac{2L_P I_D}{\mu_p C_{ox} W_P}} + \left|V_{TP}\right| \tag{9}$$

With L_p and W_p the PMOS transistor length and width respectively. μ_P is the hole mobility.

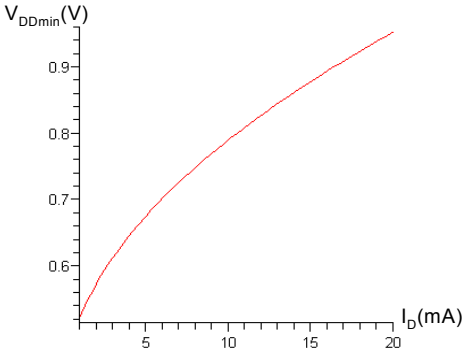


Fig. 22. Minimum supply voltage versus current consumption in a LC ladder current reuse topology. W_P=30µm, L_P=0.13µm, VT_{PMOS}=400mV

The expressions *(10)* and *(11)* derive the noise figure and the voltage gain of the circuit presented in Fig. 21. Driven with the same current both current reuse and cascode topologies perform similar cut-off frequency. Hence comparable NF_{min} and Gv are achieved. Though current reuse topology can support sub 1V operation, low noise and high gain performances require a higher supply voltage since it directly sets the current of the stage, as depicted in fig. 22.

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{g_{mtot}} C_{GStot} \sqrt{\gamma . \delta . (1 - \left|c^2\right|)} \tag{10}$$

$$G_v = \frac{g_{m\,tot} . (r_{dsn} \,//\, r_{dsp})}{2R_S . j\omega C_{GS\,tot}} \tag{11}$$

With $g_{mtot}=g_{mP}+g_{mN}$ and $C_{gstot}=C_{gsN}+C_{gsP}$

3.3 Measurement results

The simplified schematic of the circuit depicted in fig. 23 was implemented in a 6 metal levels 130nm CMOS technology from STM. This LNA is designed to cover the 6-10GHz upper band of European UWB standard. A DC Feedback (DCFB) loop regulates the output DC voltage of the first stage. The nominal supply is set to 1.6V to ensure both high gain and low noise figure. The buffer is loaded with peaking inductors which compensate for the roll-off occurring in the first stage.

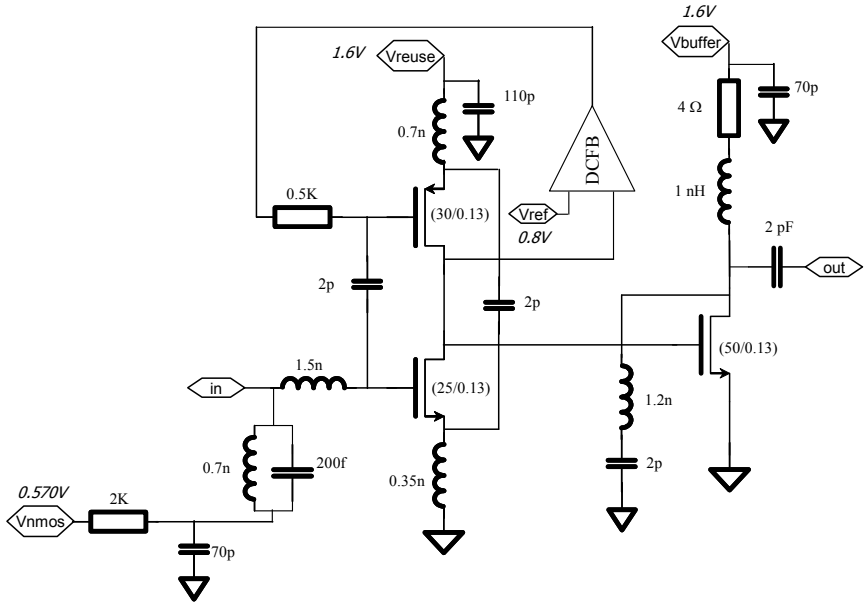


Fig. 23. UWB LC ladder current reuse LNA

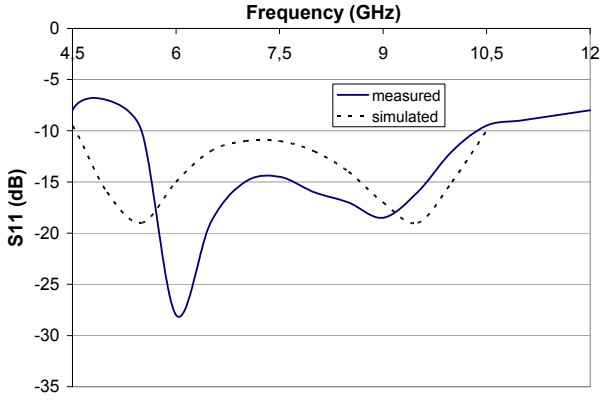


Fig. 24. Measured x Simulated S_{11} parameter

The measurement results have been performed with a GSG probe bench combined with a HP 8510B network analyzer and a HP 8970 NF-meter. The input matching, based on a 4th order pass-band filter, exhibits two minimum at 6 and 10 GHz as depicted in fig. 24. The S_{11} parameter is kept lower than -10 dB from 5.4 to 10.2 GHz. The discrepancy between simulation and measurement forms emphasizes the sensitivity of LC ladder implementation to parasitic elements.
Intended for 6-10GHz, the circuit, operating under 1.6V, achieves a more than 10dB quasi flat band gain from 5.6 to 8.8 GHz with a maximum 12.2dB at 6.5GHz, Fig. 25. A -3dB attenuation is here provided by the buffer. So the current reuse stage performs a roughly 15dB maximum gain for a 3mA current consumption. After retro-simulations it has been underlined extra capacitors, at the output node, strengthen the voltage roll-off of the first stage. As a matter of consequence it is not fully compensated by the peaking load above 9 GHz.

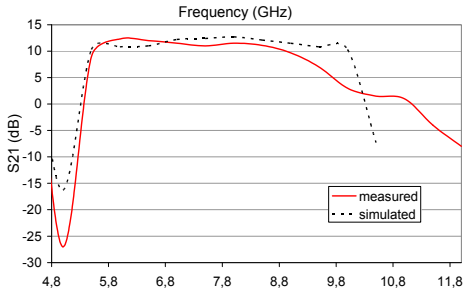


Fig. 25. Measured x Simulated S_{21} parameter

From noise point, M_N and M_P transistors are sized to provide the lowest NF at 7GHz that is a good tradeoff regarding the 6 to 10 GHz frequency band of interest. Likewise input matching, the form of the NF measurements is shifted to low frequency in fig. 26. The LC ladder technique remains lower noise than its resistive feedback counterpart. Indeed the NF is kept constant at 4.5dB from 4.5 GHz to 7.5 GHz, then it smoothly increases until 7dB at 10 GHz.

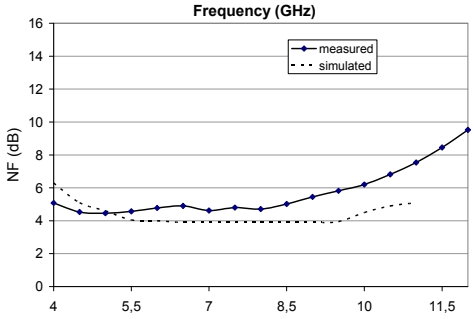


Fig. 26. Measured x Simulated NF

The voltage gain and minimum noise figure versus V_{dd} are drawn in fig. 27. A less than 3dB attenuation is observed where as the supply is reduced from 1.6 to 1V. This behavior is

driven by the DC feedback loop which tracks and compensates for the supply variations. The NF_{min} is kept lower than 4.6dB up to 1.1V operation. For sub-1V operation it smoothly increases with respect to the S_{21} drop off. The input matching as well as the circuit bandwidth are sustained until 1V.

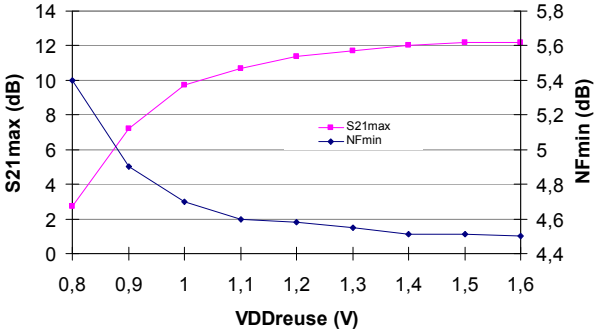


Fig. 27. S_{21} and NF_{min} versus supply voltage

The -1dB input compression point versus supply variation is reported in fig. 28. It first decreases with the voltage reduction. The LNA still performs a more than 10dB gain within a 1 to 1.6V range, fig. 27, so the output voltage range preventing from MOS linear region operation shrinks with the supply lessening thus degrading the ICP1. For sub-1V operation the lack of gain permits large signal processing improving the ICP1.

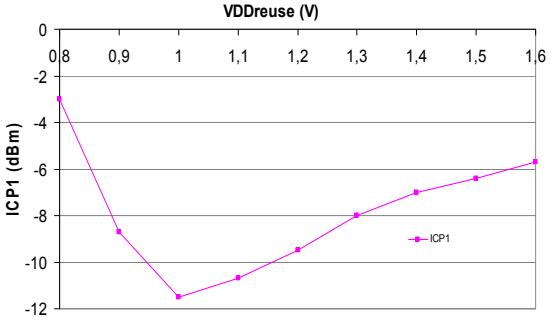


Fig. 24. ICP1 versus supply voltage

4. Design trend discussion

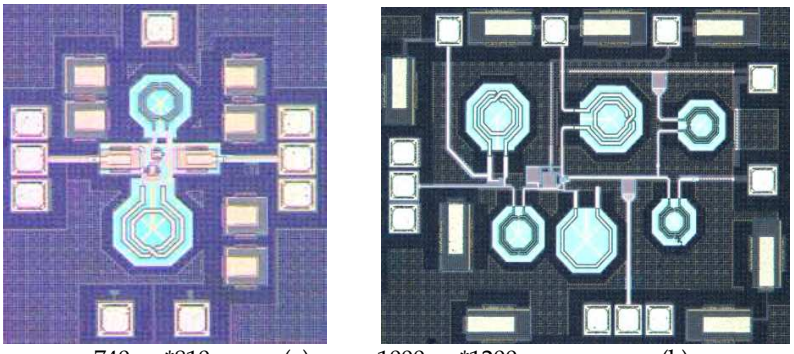
Though UWB systems are dedicated to mass market, the silicon area is a significant matter of concern since it directly impacts the chip cost. The micrographs of the two current reuse LNA reported in this work are depicted in fig. 29. The resistive FB topology, 0.6mm², fig. 29(a), allows silicon saving compared to its LC ladder counterpart, 1mm², fig. 29(b). However these considerations also need to be discussed at system level. The resistive feedback technique exhibiting a wide band response requires a pre-filtering stage which achieves strong out band rejection.

DESIGN	GAIN [DB] (BW IN GHZ)	NF [DB] (BW IN GHZ)	S11 [DB] (BW IN GHZ)	S22 [DB (BW IN GHZ)	INPUT TYPE	CHIP AREA (ACTIVE)	P_{DC} (WITHOUT BUFFER)
0.13µm CMOS [TW1]*	12.3±2dB (5.6-8.8)	4.4 to 7 (4–10)	<-10dB (5.4–10)	<-10dB (5.2 – 12)	LC ladder	1.2mm²	5mW@1.6V
0.13µm CMOS [TW2]*	11.5±1dB (2–9)	4.45 to 9 (3–10)	<-10dB (1–14.6)	<-10dB (1 – 14.2)	Resistive feedback+L	0.6mm²	17mW@1.4V
0.18µm CMOS [6]	9±1.5dB (2.3-9.3)	4 to 9.2 (3 –10)	<-9.9 (2.6 – 11.7)	<-13 (3 – 10)	LC ladder	1.1mm²	9mW@1.8V
0.25µm BiCMOS [13]	8.5±3dB (4.4 – 10.6)	7.5 to 9.5 (3 - 11)	<-10 (4.2 – 12)	<-9dB (2.8 – 11)	LC ladder	1.3mm²	8.5mW@2.5V
0.18µm CMOS [15]	13.5±3dB (2 – 9)	2.3 to 7.4 (2 – 9)	<-8.8dB (2 – 9)	<-15dB (2 – 10)	Resistive feedback+L	0.9mm²	25mW@1.8V
0.18µm CMOS [16]	9.8±3dB (2 – 4.6)	2.3 to 6 (3 – 5.4)	<-10dB (3 – 6)	<-10dB (2 – 6)	Resistive feedback+LC	0.9mm²	12mW@1.8V

**TW means This Work*

Table V. Measured performance summary and comparison

To do so BWA or SAW filters are mandated thus increasing the device price. LC ladder topologies performing pass-band response help in out band rejection thus lowering the rejection constrains on the pre-filtering stage. The silicon integration of such a filter can be expected lessening the device cost. Hence both approaches must be considered at transistor and system levels with respect to the specifications.



740µm*810µm (a) 1000µm*1200µm (b)

Fig. 29. Chip micrograph of resistive FB current reuse LNA (a) and LC ladder current reuse LNA (b)

The table V summarizes the performances of the circuits and prior published works. It is worth noting UWB devices intended for wireless applications must be low power compatible. The LC ladder references [TW1], [6] and [13] perform comparable performances with resistive architectures [TW2], [15] and [16] for a roughly half power consumption making this technique well suited for RF systems. However it has been demonstrated in section II that the performances of resistive feedback circuits, especially the bandwidth and the power consumption, are technology dependent. We can estimate the implementation of resistive LNA in newer technologies, 65nm or 40nm nodes as instance, would compete with LC ladder approaches.

Furthermore the table V clearly demonstrates that current reuse approach is a promising configuration for ultra wide band LNA. Indeed comparing the circuits, here presented, [TW1] and [TW2] with proposed references [6], [13] and [15] it allows both a lower supply voltage operation and a power saving. Since current reuse configuration is not a wideband dedicated technique, the improvements, here reported, can even be extended to the general purpose of CMOS LNA design under low power and low voltage constrains.

5. Perspectives

About Software Radio

The concept of Software Radio (SR) was first introduced by the US Army. The main goal was to secure communications on hostile battlefield. The project "Speakeasy" was the first stone brought to researches and opened all a new field in the telecommunication industry, military and civil ones. Mitola exposed a defined concept of Software Radio in 1999. It is described as a fully reconfigurable wireless device that adapts its communication radio in response to network and user demands.

The telecommunication industry has seen the opportunity to work on a very promising principle. It is summed up by replacing several receiving chain in mobile phones, each one addressing a standard, through a one-chip-solution. This unique chip would enable the reception of pre-defined and unknown telecommunication standards by self reconfiguration. In a few words the SR device, presented in Fig. 30, is expected to be the ultimate radio system. To compete with advanced multi-standard solutions under development SR solution must cope with stringent constrains among them are:

- a reduced cost of design
- a reduced cost of power consumption
- a reduced cost of human investment

The first assessment implies a CMOS implementation. The second one issues from the huge power consumption of the solutions based on multi RF front end. The last point assumes the focus of the whole engineer staff on a single project would lead to a cost effective development.

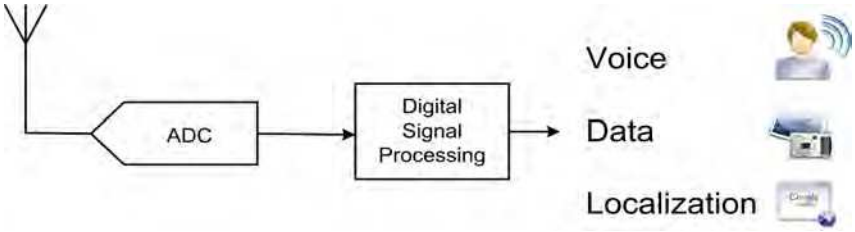


Fig. 30. The software radio solution

Nowadays, some technological bottlenecks make difficult the development of a full SR receiver intended for mobile terminals. Indeed, in Fig. 30, the input signals coming from the antenna have to be converted into digital at least at twice the RF frequencies, a roughly 10GHz, with a high resolution, 16 bits. Such kind of Analog to Digital Convertor (ADC) does not exist and are not expected before 15 years on silicon. So today SR is rather derived into Software Defined Radio (SDR). These systems allow reconfigurations among pre-

defined wireless standards [18][19][20][21]. The solution proposed in the Fig. 31 is based on a conventional heterodyne receiver with reconfigurable building blocks. But the adjusting of some functions like filters and antenna remains intricate and limits the covering of the receiver to a few of applications. The successful of SR implementation needs a new deal in radio schemes.

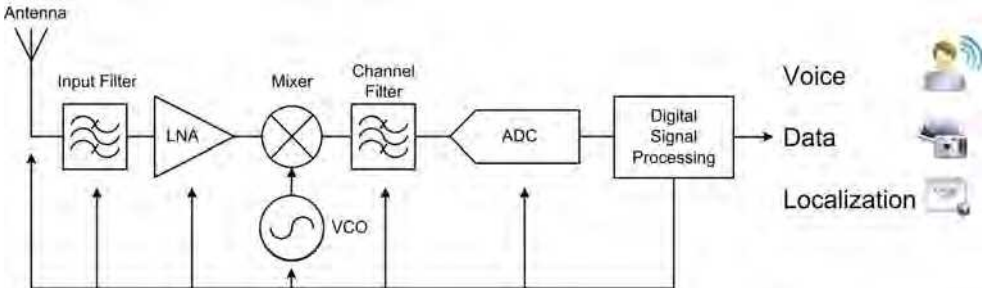


Fig. 31. A software defined radio solution based on conventional radio scheme

Other works on disruptive solution with an intensive research in analog Front End are proposed. Some explore discrete time analog signal processing in order to translate into analog domain the processing work usually done into digital [22]. It enables better trade-off between reconfigurability and power consumption. Among the most promising solution under study is the Sampled Analog Signal Processor (SASP) [23], fig. 32. The SASP uses the principle of an analog discrete Fourier transforms to translate into frequency domain the RF signal [sasp7]. The calculation is based on voltage samples.

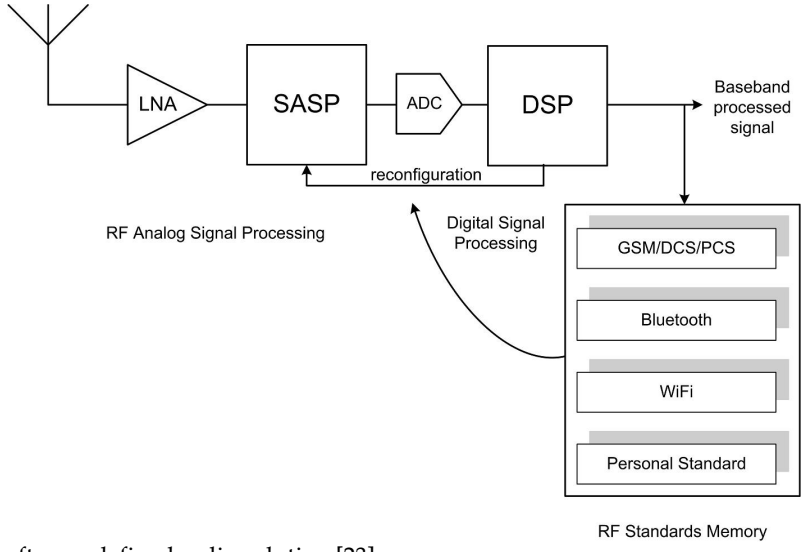


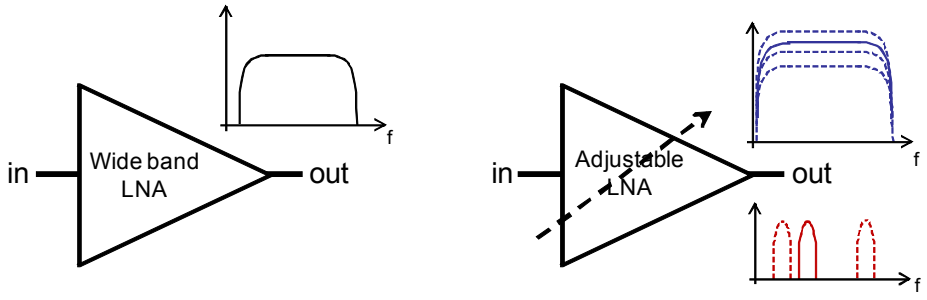
Fig. 32. A software defined radio solution [23]

Once the spectrum containing the information in a 0 to 5GHz range is processed, it is a matter to select the only one (or several) signal envelops to be demodulated. It is composed by few voltage samples among thousands. These samples are converted into digital for a digital signal processing. This system is able to cover any RF standards according to a low power consumption given by analog signal processing and flexibility offered by a DSP. The DSP manages the use of stored standards and reconfigures as needed the parameters of the SASP. The standard memory can be updated and accepts news standards through old standards, Fig. 32.

This brief on next SDR and SR solutions emphasizes the coming revolution in radio scheme of future wireless handsets. Hence the conventional solutions lying on (super) heterodyne receivers will blow up leaving the corner to an embedded analog/digital processing of the RF signal. These novel frontends, like SASP in Fig. 32, will still need two traditional building blocks: an antenna and a LNA.

What would LNA for SR be?

The answer does not depend on the choice between SR or SDR solution. In both cases the amplifier would cover a wide bandwidth. It must features good performances, NF, gain and linearity, making voltage samples suited for analog and digital processing.



(a) *(b)*

Fig. 33. Behavioral LNA solution for SR receivers: wide band *(a)* adjustable *(b)*

A first solution, Fig. 33(a), would rely on a wide band LNA achieving the best performances, required by the most stringent standard, over its whole bandwidth. But it is not an optimized approach, in particularly from power saving, since the LNA often provides useless skills regarding the application needs. A smart management is to adjust the LNA performances according to the standard requirements. As reported in expressions (1), (2), (7), (8), (10) and (11), both the NF and gain depend on the current consumption through the transconductance of the input transistors. These features can be so tuned by varying the biasing of the LNA. Considering the linearity, the wide band operation puts on the receiver some stringent constrains from intermodulation rejections. The IIP3 and IIP2 can be improved by a narrow band response of the circuit. So we can draw the behavior of a SR LNA as it follows, Fig. 33(b):

- a wide band operation for signal tracking
- a tunable topology to adjust the performances with the targeted applications
- a narrow band response to fill high IIP_i requirements

As mentioned in [24], the performances of a SASP unit, and later SR devices, are technology dependent. The narrower the transistor is the higher the operating frequency

and the resolution is. So each new CMOS generation will directly impact on SR capabilities. This means that the scaling constrains on LNA design, above mentioned, will be further stringent. Based on the investigations reported in this work, the circuit depicted in Fig. 34 proposes a SR LNA topology suited for low voltage supply.

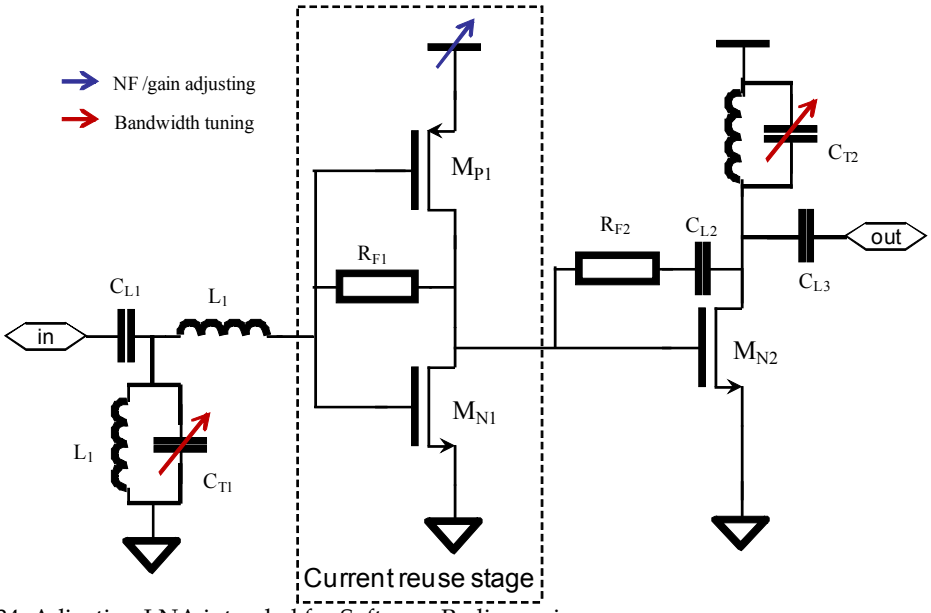


Fig. 34. Adjusting LNA intended for Software Radio receiver

The core of the LNA is a current reuse configuration to be low voltage compatible. The resistive feedback approach ensures a very wide band response for signal tracking mode. The supply control, blue arrow, allows NF and Gv variations according to Fig. 13. The variable capacitors, red arrows, synthesizing filters adjust the bandwidth and operating frequency in narrow band mode.

If full SR systems make useless some building blocks like mixer and VCO, they open a large field of investigations for LNA. The complexity of such next radio solution would focus the interest of front-end designers in the years to come. A first question that they would answer is: what is the best suited LNA behavior for a SR receiver? The circuits will cope with some new concepts of frequency agility, from low to high frequency in narrow and/or wide band operations. Both a system management and a reconfigurable architecture are expected to fill this point. The requirement for adjusting NF and gain characteristics will also challenge the implementation of LNA. Novel circuit techniques are mandated in such case.

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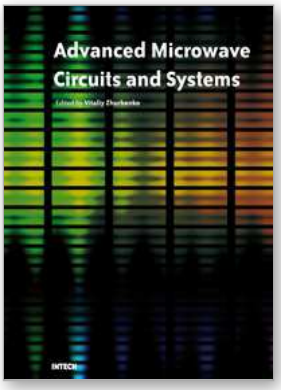

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This book is based on recent research work conducted by the authors dealing with the design and development of active and passive microwave components, integrated circuits and systems. It is divided into seven parts. In the first part comprising the first two chapters, alternative concepts and equations for multiport network analysis and characterization are provided. A thru-only de-embedding technique for accurate on-wafer characterization is introduced. The second part of the book corresponds to the analysis and design of ultra-wideband low- noise amplifiers (LNA).

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