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CMOS Voltage and Current Reference Circuits consisting of Subthreshold MOSFETs

— Micropower Circuit Components for Power-aware LSI Applications —

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1. Introduction

The development of ultra-low power LSIs is a promising area of research in microelectronics. Such LSIs would be suitable for use in power-aware LSI applications such as portable mobile devices, implantable medical devices, and smart sensor networks [1]. These devices have to operate with ultra-low power, i.e., a few microwatts or less, because they will probably be placed under conditions where they have to get the necessary energy from poor energy sources such as microbatteries or energy scavenging devices [2]. As a step toward such LSIs, we first need to develop voltage and current reference circuits that can operate with an ultra-low current, several tens of nanoamperes or less, i.e., sub-microwatt operation. To achieve such low-power operation, the circuits have to be operated in the subthreshold region, i.e., a region at which the gate-source voltage of MOSFETs is lower than the threshold voltage [3; 4]. Voltage and current reference circuits are important building blocks for analog, digital, and mixed-signal circuit systems in microelectronics, because the performance of these circuits is determined mainly by their bias voltages and currents. The circuits generate a constant reference voltage and current for various other components such as operational amplifiers, comparators, AD/DA converters, oscillators, and PLLs. For this purpose, bandgap reference circuits with CMOS-based vertical bipolar transistors are conventionally used in CMOS LSIs [5; 6]. However, they need resistors with a high resistance of several hundred megaohms to achieve low-current, subthreshold operation. Such a high resistance needs a large area to be implemented, and this makes conventional bandgap references unsuitable for use in ultra-low power LSIs. Therefore, modified voltage and current reference circuits for lowpower LSIs have been reported (see [7]-[12], [14]-[17]). However, these circuits have various problems. For example, their power dissipations are still large, their output voltages and currents are sensitive to supply voltage and temperature variations, and they have complex circuits with many MOSFETs; these problems are inconvenient for practical use in ultra-low power LSIs. Moreover, the effect of process variations on the reference signal has not been discussed in detail. To solve these problems, I and my colleagues reported new voltage and current reference circuits [13; 18] that can operate with sub-microwatt power dissipation and with low sensitivity to temperature and supply voltage. Our circuits consist of subthreshold MOSFET circuits and use no resistors.

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The following sections provide overviews of previous reported low-power reference circuits and a detailed explanation of our circuits. Section 2 describes the subthreshold current of MOSFETs and shows the temperature and process sensitivity of the current with a SPICE simulation. Section 3 describes the principle of conventional voltage and current reference circuits based on bandgap reference circuits. Sections 4 and 5 explain the operation principle of the reported voltage and current reference circuits and show the characteristics of prototype devices we made using 0.35-μm standard CMOS process technology. Finally, concluding remarks are presented in Sect. 6.

2. Subthreshold region (or weak inversion region) of MOSFETs

When the gate-source voltage of a MOSFET is lower than the threshold voltage, subthreshold current can be obtained. The subthreshold current through a MOSFET is an increasing exponential function of the gate-source voltage, and the current value is on the order of nanoamperes. Moreover, the subthreshold current is sensitive to temperature and process variations. The temperature and process characteristics of the subthreshold current are analyzed as follows.

Figure 1 shows the measured transfer curves of an nMOSFET in 0.35-μm CMOS process at different temperatures from –20 to 100°C. The drain-source voltage was set to 1 V. The threshold voltage is about 0.5 V in this device. The subthreshold drain current I_{DS} of a MOSFET is an exponential function of the gate-source voltage V_{GS} and the drain-source voltage V_{DS} and is given by

$$I_{DS} = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right), \tag{1}$$

$$I_0 = \mu C_{OX}(\eta - 1)V_T{}^2$$

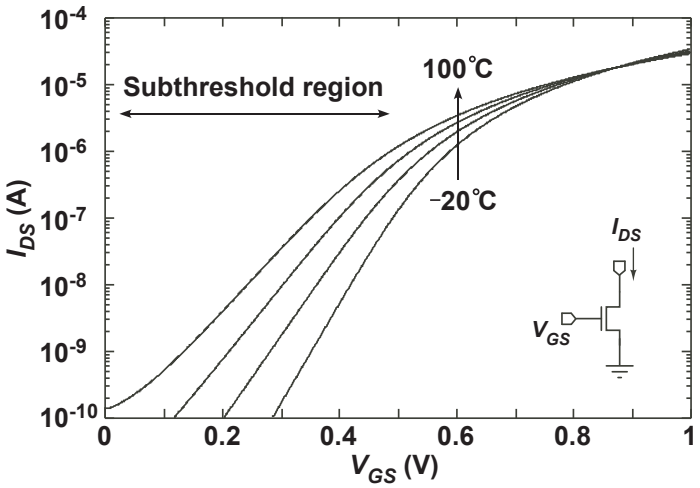


Fig. 1. Measured transfer curves of nMOSFET as a function of gate-source voltage V_{GS} at different temperatures.

where K is the aspect ratio (=W/L) of the transistor, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, V_T(=k_BT/q) is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor [3], [19]. For V_{DS} > 0.1 V, current I_{DS} is independent of V_{DS} and is given by

$$I_{DS} = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right). \tag{2}$$

The temperature dependence of the threshold voltage V_{TH} and the mobility μ of MOSFET can be given by

$$V_{TH} = V_{TH0} - \kappa T, \tag{3}$$

$$\mu(T) = \mu(T_0)(T / T_0)^{-m} \tag{4}$$

where $\mu(T_0)$ is the carrier mobility at room temperature T_0, m is the mobility temperature exponent, V_{TH0} is the threshold voltage at 0 K, and κ is the temperature coefficient of V_{TH} [20].

The temperature coefficient (T.C.) of the subthreshold current with fixed gate-source voltage is given by

$$\begin{aligned} T.C. &= \frac{1}{I_{DS}}\frac{dI_{DS}}{dT} \\ &= \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{V_T^2}\frac{dV_T^2}{dT} + \frac{1}{\exp((V_{GS} - V_{TH})/\eta V_T)}\frac{d}{dT}\exp((V_{GS} - V_{TH})/\eta V_T) \\ &= \frac{2-m}{T} + \frac{\kappa - (V_{GS} - V_{TH})/T}{\eta V_T}. \end{aligned} \tag{5}$$

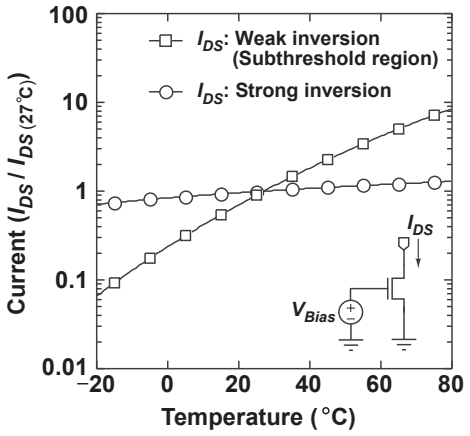
Process variations can be classified into two categories: i.e., within-die (WID) (intra-die) variation and die-to-die (D2D) (inter-die) variation [21]-[23]. The WID variation is caused by mismatches between transistor parameters within a chip and affects the relative accuracy of the parameters. In contrast, the D2D variation affects the absolute accuracy of transistor parameters between chips.

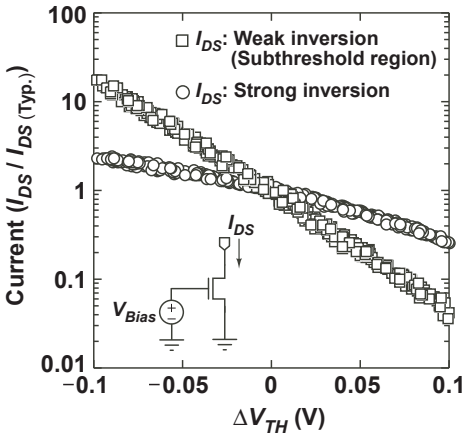
The process dependence of the subthreshold current can be expressed by

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{1}{I_{DS}}\left(\frac{\partial I_{DS}}{\partial \mu}\Delta\mu + \frac{\partial I_{DS}}{\partial V_{TH}}\Delta V_{TH}\right) = \frac{\Delta\mu}{\mu} - \frac{\Delta V_{TH}}{\eta V_T}. \tag{6}$$

The mobility variation $\Delta\mu$ is generally smaller than the threshold voltage variation ΔV_{TH}, so the current depends mainly on ΔV_{TH}.

Figure 2 shows the simulated subthreshold current with fixed gate-source voltages, obtained with a SPICE simulation with a set of 0.35-μm standard CMOS process. Current operating in the strong inversion region is also plotted for comparison. Fixed gate-source voltages were set to V_{TH}–0.2 V (weak inversion), and V_{TH}+0.2 V (strong inversion), respectively. Although





	T.C.	$\Delta I_{DS}/\Delta V_{TH}$
I_{DS} : Weak inversion (V_{Bias}=V_{TH}−0.2)	3%/℃	2.5%/mV
I_{DS} : Strong inversion (V_{Bias}=V_{TH}+0.2)	0.5%/℃	0.8%/mV

Fig. 2. (A). Simulated drain currents as a function of temperature. Fixed gate biases were set to V_{TH}–0.2 V (weak inversion), and V_{TH}+0.2 V (strong inversion). (B). Drain currents as a function of D2D threshold voltage variation ΔV_{TH}, as obtained from Monte Carlo simulation of 300 runs.

the current in the strong inversion region has a small temperature dependence (0.5%/°C), the subthreshold current has a large temperature dependence (3%/°C), as shown in Fig. 2-(A). Figure 2-(B) shows the simulated subthreshold current as a function of the threshold voltage variation ΔV_{TH}, as obtained from Monte Carlo simulation of 300 runs, assuming both die-to-die (D2D) variation (e.g., ΔV_{TH}, $\Delta\mu$, ΔT_{OX}, ΔL, ΔW) and within die (WID) variation (e.g., $\sigma_{V_{TH}}$, σ_{μ}, $\sigma_{T_{OX}}$, σ_{L}, σ_{W}) in transistor parameters [21; 22; 23]. Each open circle and square show I_{DS} for a run. The subthreshold current depends strongly on the threshold voltage variation (2.5%/mV) in comparison with the strong inversion current (0.8%/mV). Therefore, the subthreshold current is strongly dependent on temperature and process variations. In circuit designs, the process sensitivity of the subthreshold current has to be reduced by using large-sized transistors [23] and various analog layout techniques [24]. On the other hand, the exponential behavior and the high sensitivity to temperature of the subthreshold current can be used to compensate for temperature variation of a constant voltage, such as voltage reference circuits.

3. Voltage and current references based on bandgap reference circuits

Bandgap voltage reference circuits are widely used as voltage references. Figure 3 shows conventional bandgap voltage reference circuits [5],[6]. The circuits generate reference voltages independent of the process, supply voltage, and temperature, and consist of the MOSFET circuits, substrate pnp bipolar transistors, and resistors. The operation principles are as follows.

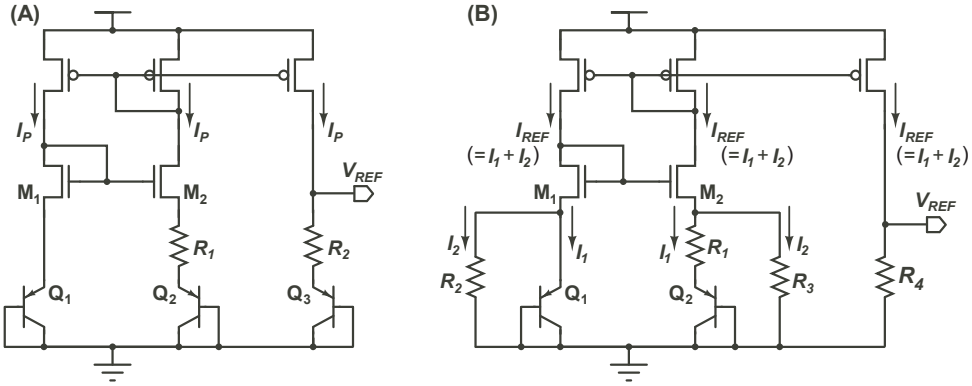


Fig. 3. (A). Conventional bandgap voltage reference circuit [5]. (B) Sub-1-V output bandgap voltage reference circuit [6] and current reference circuit [25].

3.1 Operation as voltage reference circuit

The collector current I_C of the bipolar transistor is given by

$$I_C = KI_S \exp\left(\frac{V_{BE}}{V_T}\right) \tag{7}$$

where K is the transistor size, I_S is the saturation current, and V_{BE} is the base-emitter voltage [5]. In the circuit in Fig. 3-(A), the operation current I_P is determined by the bipolar transistors Q_1 and Q_2 with different transistor sizes and the resistor R_1, and is given by

$$I_P = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{V_T \ln(K_2 / K_1)}{R_1}. \tag{8}$$

The current I_P is proportional to absolute temperature (PTAT). The resistor R_2 and the transistor Q_3 accept the current through the current mirror circuit and produce the output voltage, which is given by

$$V_{REF} = V_{BE3} + I_P R_2 = V_{BE3} + \frac{R_2}{R_1} V_T \ln(K_2 / K_1). \tag{9}$$

Equation (9) shows that V_{REF} can be expressed as a sum of the base-emitter voltage and thermal voltage scaled by the resistor ratio. Because V_{BE} has a negative T.C. and V_T has a positive T.C., output voltage V_{REF} with a zero T.C. can be obtained by adjusting the resistor ratio. The reference voltage is based on the bandgap energy of silicon, which is about 1.25 V. Banba *et al.* proposed a modified bandgap voltage reference circuit as shown in Fig. 3-(B). The circuit generates sub-1-V reference voltage. The operation currents I_1 and I_2 are given by

$$I_1 = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{V_T \ln(K_2 / K_1)}{R_1}, \qquad I_2 = \frac{V_{BE1}}{R_2}. \tag{10}$$

The resistor R_4 accepts the current I_{REF}(=I_1+I_2) through a current mirror circuit and produces output voltage, so the output voltage can be expressed as

$$V_{REF} = I_{REF}R_4 = \frac{R_4}{R_2}V_{BE1} + \frac{R_4}{R_1}V_T \ln(K_2 / K_1). \tag{11}$$

Therefore, adjusting the resistor ratio, the circuit generates sub-1-V reference voltage that is independent of temperature.

3.2 Operation as current reference circuit

The circuit as shown in Fig. 3-(B) can be used as a current reference generator [25]. The temperature dependence of resistors is given by $R = R_0(1+ \alpha T)$, where R_0 is the resistance value at absolute zero temperature, and α is the temperature coefficient of the resistor. Because V_{BE} and $\Delta V_{BE}(=V_{BE1} - V_{BE2})$ have a negative and a positive temperature dependence, respectively, the temperature dependences can be expressed simply by $V_{BE}=V_{BE0}(1 - AT)$ and $\Delta V_{BE}=BT$, where A and B are the T.C. of V_{BE} and ΔV_{BE}, respectively, and V_{BE0} is the baseemitter voltage at absolute zero temperature. Therefore, the reference current $I_{REF}(=I_1+I_2)$ is given by

$$\begin{aligned} I_{REF} = I_1 + I_2 &= \frac{\Delta V_{BE}}{R_1} + \frac{V_{BE1}}{R_2} = \frac{BT}{R_{01}(1+\alpha T)} + \frac{V_{BE0}(1-AT)}{R_{02}(1+\alpha T)} \\ &= \frac{1}{R_{01}}(BT)(1-\alpha T) + \frac{V_{BE01}}{R_{02}}(1-AT)(1-\alpha T) \\ &\approx \frac{1}{R_{01}}(BT) + \frac{V_{BE01}}{R_{02}}(1-(A+\alpha)T). \end{aligned} \tag{12}$$

The left and right terms in Eq. (12) have negative and positive temperature dependence, respectively. Therefore, adjusting the appropriate resistor values, the circuit generates a reference current that is independent of temperature.

These circuits generate stable reference voltages and currents. However, the power dissipations of these circuits are too large (from 5 to 500 μW), so they need resistors with a high resistance of several hundred megaohms to achieve low-current, sub-microwatt operation. Such high resistance needs a large area to be implemented, and this makes conventional bandgap references unsuitable for use in ultra-low-power LSIs.

4. Overview of low-power voltage reference circuits

To achieve ultra-low-power operation and small area, modified voltage reference circuits without bipolar transistors have been reported (see [12]-[18]). These circuits consist of CMOS circuits that operate in the strong inversion and the subthreshold regions of MOSFET. The circuits generate a reference voltage that is independent of temperature and supply voltage. The next sections provide an overview of the reported low-power voltage reference circuits.

4.1 Voltage references based on ΔV_{GS}

Figure 4 shows voltage reference circuits based on the difference between the gate-source voltages of (A) two nMOS transistors, and (B) nMOS and pMOS transistors as reported by Song *et al.* [7] and Leung *et al.* [8], respectively. All MOSFETs operate in the strong inversion region.

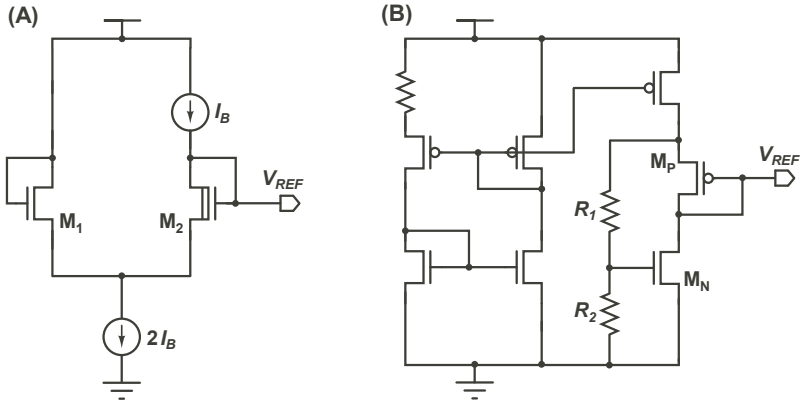


Fig. 4. Voltage reference circuits based on difference between gate-source voltages of (A) two nMOS transistors [7], and (B) nMOS and pMOS transistors [8].

The drain current I_{DS} that operates in the strong inversion, saturation region can be expressed as

$$I_{DS} = \frac{K\beta}{2}(V_{GS} - V_{TH})^2 \tag{13}$$

where K is the aspect ratio of the transistors, and $\beta(= \mu C_{OX})$ is the current gain factor.
The circuit in Fig. 4-(A) consists of M_1 and M_2 with different threshold voltage devices. The reference voltage is given by

$$\begin{aligned} V_{REF} &= V_{GS1} - V_{GS2} \\ &= (V_{TH01} - \kappa T) - (V_{TH02} - \kappa T) + \sqrt{\frac{2I_B}{\beta}}\left(\frac{1}{\sqrt{K_1}} - \frac{1}{\sqrt{K_2}}\right) \\ &\approx V_{TH01} - V_{TH02}. \end{aligned} \tag{14}$$

A low bias current I_B is used so that the temperature dependence of β can be ignored. Therefore, the reference voltage based on the difference between the threshold voltages can be obtained. However, the circuit requires a multiple-threshold voltage process, and, to cancel the temperature dependence of the reference voltage, the process must be controlled carefully so that the temperature coefficients κ of the two threshold voltages have the same value in each MOSFET.
Figure 4-(B) shows another voltage reference circuit based on the difference between the gate-source voltages of nMOS and pMOS transistors using a standard CMOS process. The reference voltage is given by

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right)V_{GSN} - V_{GSP}. \tag{15}$$

Therefore, adjusting the resistor ratio and the transistor sizes, the temperature dependence of the threshold voltages can be canceled, while the temperature dependence of the

mobilities can be canceled only at room temperature. Consequently, the T.C. of the output voltage will be degraded for a wide temperature range. As reported in [8], a measured T.C. of 36.9 ppm/°C and a power dissipation of 30 μW were obtained. However, the power dissipation is still too large for use with sub-microwatt operation. To reduce the power dissipation, the circuit requires resistors with high resistance.

4.2 Voltage references operating in the strong inversion region of MOSFETs

Vita *et al.* proposed a voltage reference circuit consisting of transistors M_3–M_8 operating in the strong inversion region, and M_1 and M_2 operating in the subthreshold region as shown in Fig. 5-(A) [9]. In this circuit, the gate-source voltages for the four MOSFETs (M_1 through M_4) form a closed loop, so we find that $V_{GS3} + V_{GS1} = V_{GS2} + V_{GS4}$, i.e.,

$$\eta V_T \ln(K_2 / K_1) = \sqrt{2I_B / K_4\beta} - \sqrt{2I_B / K_3\beta}. \tag{16}$$

Therefore, the bias current I_B can be expressed by

$$I_B = \frac{K_4\beta}{2}\eta^2 V_T^2 \ln^2(K_2 / K_1)\left(\frac{\sqrt{K_3}}{\sqrt{K_3} - \sqrt{K_4}}\right)^2. \tag{17}$$

Transistors M_5–M_8 accept the current I_B and generate the output voltage. Most of the bias current I_B must flow through M_7 and M_8 rather than through M_5 and M_6 to compensate for the temperature dependence of the mobility μ. Therefore, the output voltage can be given by

$$V_{REF} = V_{GS8} + V_{GS5} - V_{GS7} = V_{TH} + \sqrt{\frac{2I_B}{\beta}}\left(\frac{1}{\sqrt{K_8}}\left(1 + \sqrt{\frac{K_6}{K_5}}\right) - \frac{1}{\sqrt{K_7}}\right)$$

$$= V_{TH} + \eta V_T \ln(K_2 / K_1)\frac{\sqrt{K_3 K_4}}{\sqrt{K_3} - \sqrt{K_4}}\left(\frac{1}{\sqrt{K_8}}\left(1 + \sqrt{\frac{K_6}{K_5}}\right) - \frac{1}{\sqrt{K_7}}\right). \tag{18}$$

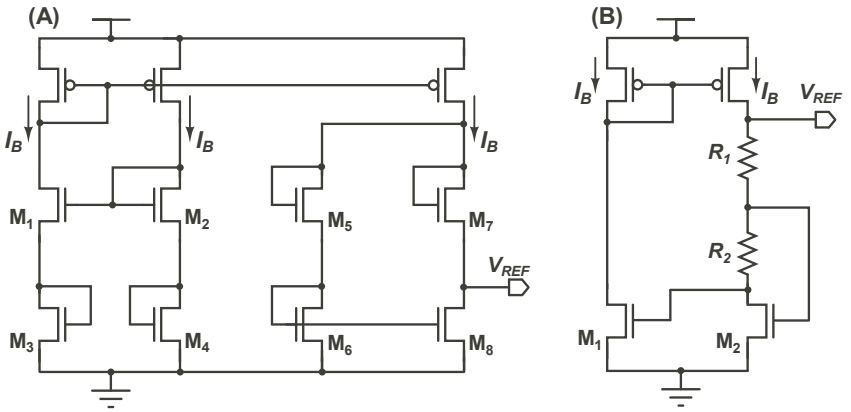


Fig. 5. Voltage reference circuit (A) operated in the strong inversion region [9], and (B) based on peaking current mirror circuit [10].

Because V_{TH} in Eq. (3) has a negative T.C. and V_T has a positive T.C., output voltage V_{REF} with a zero T.C. can be obtained by adjusting the size of the transistors.
As reported in [9], a measured T.C. of 12 ppm/°C and a power dissipation of 0.12 μW were obtained. Although the operation current of the circuit is on the order of nanoamperes, transistors M_3–M_8 operate in the strong inversion, saturation region. So, designs with careful transistor sizing are required for operation in each of the regions in MOSFETs.

4.3 Voltage references operating in the subthreshold region of MOSFETs

Cheng *et al.* developed a voltage reference using a peaking current mirror circuit as shown in Fig. 5-(B) [10]. All MOSFETs operate in the subthreshold region. The circuit forms a closed loop, i.e., $V_{GS1} = V_{GS2} - I_B R_2$, so the bias currents I_B can be expressed by

$$I_B = \frac{V_{GS2} - V_{GS1}}{R_2} = \frac{\eta V_T \ln(K_1 / K_2)}{R_2}. \tag{19}$$

The output voltage is given by

$$\begin{aligned} V_{REF} &= V_{GS2} + I_B R_1 \\ &= V_{GS2} + \frac{R_1}{R_2} \eta V_T \ln(K_1 / K_2). \end{aligned} \tag{20}$$

Because V_{GS} and V_T have a negative and a positive T.C., respectively, output voltage V_{REF} with a zero T.C. can be obtained by adjusting the resistor ratio. As reported in [10], a measured temperature coefficient of 62 ppm/°C and a power dissipation of 4.6 μW were obtained.
Huang *et al.* proposed a voltage reference circuit based on subthreshold MOSFETs [11] as shown in Fig. 6. The bias currents I_1 and I_2 are given by

$$I_1 = \frac{V_{GS8} - V_{GS9}}{R_2} = \frac{\eta V_T \ln(K_9 / K_8)}{R_2}, \qquad I_2 = \frac{V_{GS3}}{R_1} - \frac{K_5}{K_6} I_1. \tag{21}$$

Therefore, the output voltage can be expressed by

$$\begin{aligned} V_{REF} &= \left(\frac{K_{10}}{K_7} I_1 + \frac{K_{11}}{K_2} I_2 \right) R_3 \\ &= \frac{K_{11}}{K_2} \frac{R_3}{R_1} V_{GS3} + \left(\frac{K_{10}}{K_7} - \frac{K_{11} K_5}{K_2 K_6} \right) \frac{R_3}{R_2} \eta V_T \ln(K_9 / K_8). \end{aligned} \tag{22}$$

Because V_{GS} has a negative T.C. and V_T has a positive T.C., output voltage V_{REF} with a zero T.C. can be obtained by adjusting the resistor ratio and the transistor sizes. As reported in [11], a measured temperature coefficient of 271 ppm/°C and a power dissipation of 3.3 μW were obtained. In the circuits as shown in Figs. 5-(B) and 6, however, the power dissipations are still large. To achieve sub-microwatt operation, these circuits require resistors with a high resistance of several hundred megaohms.

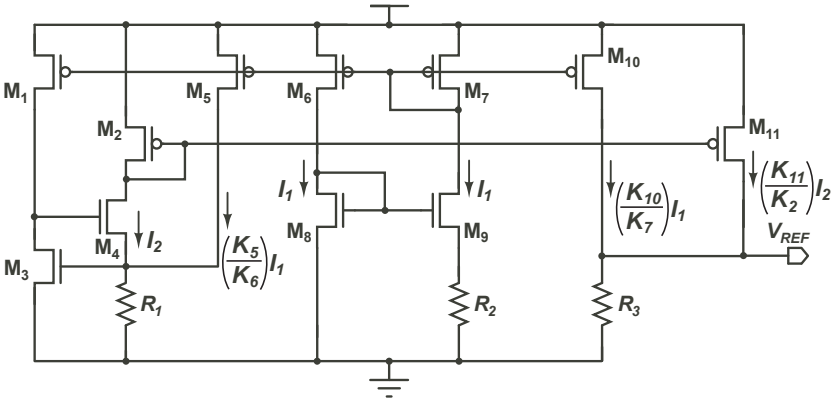


Fig. 6. Voltage reference circuit operated in the subthreshold region [11].

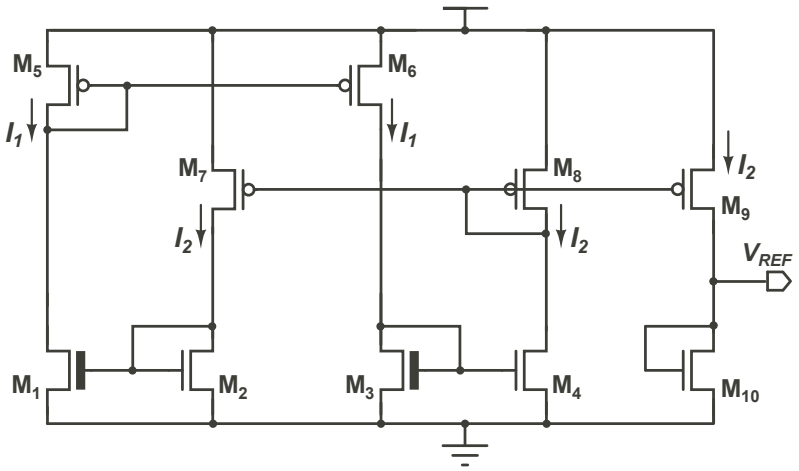


Fig. 7. Voltage reference circuit operated in the strong inversion and subthreshold regions using high-V_{TH} devices [12].

Vita *et al.* proposed a voltage reference circuit using two different threshold voltage devices as shown in Fig. 7 [12]. Transistors M_1 and M_3 with high-V_{TH} devices are operated in the subthreshold region, and M_2 and M_4 are operated in the strong inversion region. From $V_{GS1} = V_{GS2}$ and $V_{GS3} = V_{GS4}$, i.e.,

$$V_{TH_{HIGH}} + \eta V_T \ln\left(\frac{I_1}{K_1 I_0}\right) = V_{TH} + \sqrt{\frac{2I_2}{K_2\beta}}$$

$$V_{TH_{HIGH}} + \eta V_T \ln\left(\frac{I_1}{K_3 I_0}\right) = V_{TH} + \sqrt{\frac{2I_2}{K_4\beta}}. \tag{23}$$

Therefore, the output load current I_2 can be expressed as

$$I_2 = \frac{K_4\beta}{2(\sqrt{K_4 / K_2} - 1)^2}\eta^2 V_T^2 \ln^2(K_3 / K_1). \tag{24}$$

Transistor M_{10} accepts the current I_2, and the output voltage can be given by

$$V_{REF} = V_{TH} + \sqrt{\frac{2I_2}{K_{10}\beta}}$$

$$= V_{TH} + \eta V_T \ln(K_3 / K_1)\frac{\sqrt{K_4 / K_{10}}}{\sqrt{K_4 / K_2} - 1}. \tag{25}$$

Because V_{TH} has a negative T.C. and V_T has a positive T.C., output voltage V_{REF} with a zero T.C. can be obtained by adjusting the size of the transistors.
As reported in [12], a measured T.C. of 10 ppm/°C and a power dissipation of 0.036 μW were obtained. However, the circuit requires a high-V_{TH} devices.

4.4 Voltage references consisting of subthreshold MOSFETs

Figure 8 shows our voltage reference circuit, which consists of a current source subcircuit and a bias-voltage subcircuit [13]. The current source subcircuit is a modified β multiplier self-biasing circuit that uses a MOS resistor M_{R1} instead of ordinary resistors. All the MOSFETs except for M_{R1} operate in the subthreshold region. MOS resistor M_{R1} is operated in a strong-inversion, deep-triode region. The circuit generates two voltages, one with a negative T.C. and one with a positive T.C., and combines them to produce a constant voltage with a zero T.C..
In the current source subcircuit, the current I_P is determined by two transistors M_1 and M_2, and the MOS resistor M_{R1}. The current I_P is given by

$$I_P = \frac{V_{DSR1}}{R_{M_{R1}}}$$

$$= K_{R1}\mu C_{OX}(V_{REF} - V_{TH})\eta V_T \ln(K_2 / K_1). \tag{26}$$

In the bias-voltage subcircuit, the gate-source voltages (V_{GS3} through V_{GS7}) of the transistors form a closed loop [26], and the currents in M_4 and M_6 are $3I_P$ and $2I_P$. Therefore, we find that output voltage V_{REF} of the circuit is given by

$$V_{REF} = V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7}$$

$$= V_{GS4} + \eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right)$$

$$= V_{TH} + \eta V_T \ln\left(\frac{3I_P}{K_4 I_0}\right) + \eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right) \tag{27}$$

where we assume that the mismatch between the threshold voltages of the transistors can be ignored. Equation (27) shows that V_{REF} can be expressed as a sum of the gate-source voltage V_{GS4} and thermal voltage V_T scaled by the transistor sizes. Because V_{TH} in Eq. (3) has a

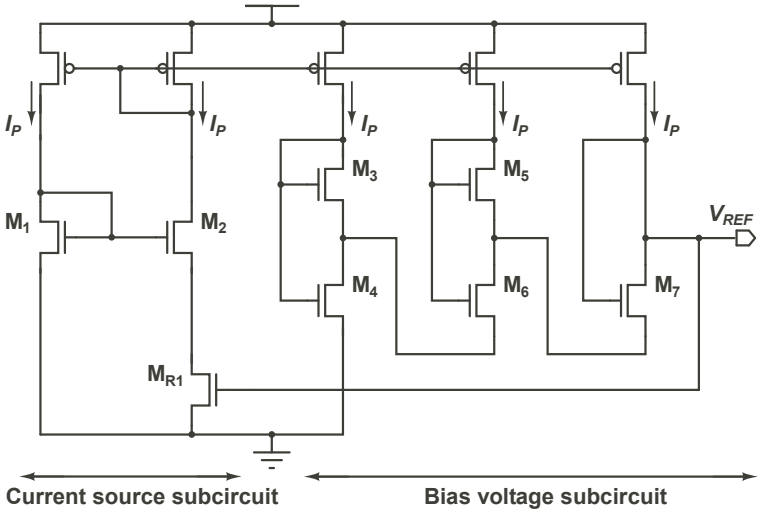


Fig. 8. Schematic of our voltage reference circuit [13]. All MOSFETs are operated in subthreshold region, except for MOS resistor M_{R1}, which is operated in strong-inversion, triode region.

negative T.C. and V_T has a positive T.C., output voltage V_{REF} with a zero T.C. can be obtained by adjusting the size of the transistors.
On the condition that $V_{REF} - V_{TH0} \ll \kappa T$ and $\eta V_T \ll \kappa T$, the T.C. of V_{REF} can be rewritten as

$$\frac{dV_{REF}}{dT} = -\kappa + \frac{\eta k_B}{q} \ln\left\{ \frac{6q\eta\kappa}{k_B(\eta-1)} \frac{K_{R1}K_3K_5}{K_4K_6K_7} \ln\left(\frac{K_2}{K_1}\right)\right\}. \tag{28}$$

Therefore, a zero T.C. voltage can be obtained by setting the aspect ratios K_i in accordance with T.C.=0 (i.e., Eq. (28)=0). From Eqs. (27) and (28), we find that

$$V_{REF} = V_{TH0}. \tag{29}$$

This shows that the circuit generates a voltage equal to the threshold voltage of MOSFETs at 0 K. Using Eqs. (26) and (29), we can express current I_P as

$$I_P = K_{R1}\mu C_{OX}\kappa T\eta V_T \ln\left(\frac{K_2}{K_1}\right). \tag{30}$$

The current is determined only by the aspect ratios (K_1, K_2, and K_{R1}) and the temperature coefficient (κ) of the threshold voltage of MOSFETs, and it is independent of the threshold voltage V_{TH}, so the current I_P is less dependent on process variations as shown in the next section. The T.C. of the current can be given by

$$\frac{1}{I_P}\frac{dI_P}{dT} = \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{T}\frac{dT}{dT} + \frac{1}{V_T}\frac{dV_T}{dT} = \frac{2-m}{T}. \tag{31}$$

The value of m is about 1.5 in standard CMOS process technologies, so current I_P has a positive T.C. and increases with temperature.

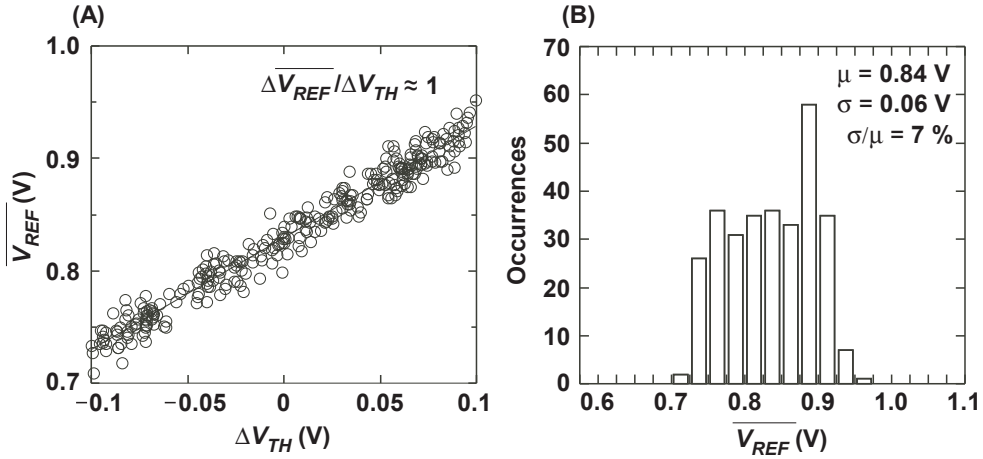


Fig. 9. (A). Average output voltage as a function of D2D variation ΔV_{TH} of threshold voltage, as obtained from Monte Carlo simulation of 300 runs. Output voltage shows a linear dependence on threshold voltage ($\Delta \overline{V_{REF}} / \Delta V_{TH} \approx 1$). (B). Distribution of output voltage, as obtained from Monte Carlo simulation.

4.4.1 Simulation and experimental results

We demonstrated the operation of our circuit with the aid of a SPICE simulation using a set of 0.35-μm standard CMOS parameters and assuming a 1.5-V power supply. To study the dependence of the output voltage on process variations, we performed Monte Carlo simulations assuming both D2D variation (e.g., ΔV_{TH}, $\Delta\mu$, ΔT_{OX}, ΔL, ΔW) and WID variation (e.g., $\sigma_{V_{TH}}$, σ_{μ}, $\sigma_{T_{OX}}$, σ_{L}, σ_{W}) in transistor parameters.

The results for 300 runs are depicted in Fig. 9. Figure 9-(A) shows the dispersion of V_{REF} from the average value ($\overline{V_{REF}}$) of V_{REF} from –20 to 80°C as a function of D2D threshold-voltage variation ΔV_{TH}. Each open circle shows $\overline{V_{REF}}$ for a run. As expected from Eq. (29), V_{REF} varies significantly with each run in a range from 0.75 to 0.95 V; this reflects the variation in transistor parameters for each run. The value of $\overline{V_{REF}}$ depends linearly on ΔV_{TH} because the circuit produces the voltage equal to the 0-K threshold voltage of MOSFETs. Figure 9-(B) shows the distribution of $\overline{V_{REF}}$. The average of $\overline{V_{REF}}$ was 840 mV, and the standard deviation was 60 mV. The coefficient of variation (σ/μ) was 7%, including D2D and WID variations.

We fabricated a prototype chip, using a 0.35-μm, 2-poly, 4-metal standard CMOS process. Figure 10-(A) shows measured output voltage V_{REF} as a function of temperature with supply voltage V_{DD} as a parameter. Almost constant voltage was achieved. The average of the output voltage was 745 mV. The temperature variation was 0.48 mV in a temperature range from –20 to 80°C, so the temperature coefficient was 7 ppm/°C. The line regulation was 20 ppm/V in the supply range of 1.4 to 3 V.

Figure 10-(B) shows measured current I_P as a function of temperature with power supply voltage as a parameter. The current I_P was about 36 nA at room temperature and reached the maximum of 39 nA at 80°C. The power dissipation of the circuit with a 1.5-V power supply was 0.32 μW at room temperature and varied from 0.28 to 0.35 μW at temperatures from –20 to 80°C. The temperature variation of the power dissipation was 0.2%/°C.

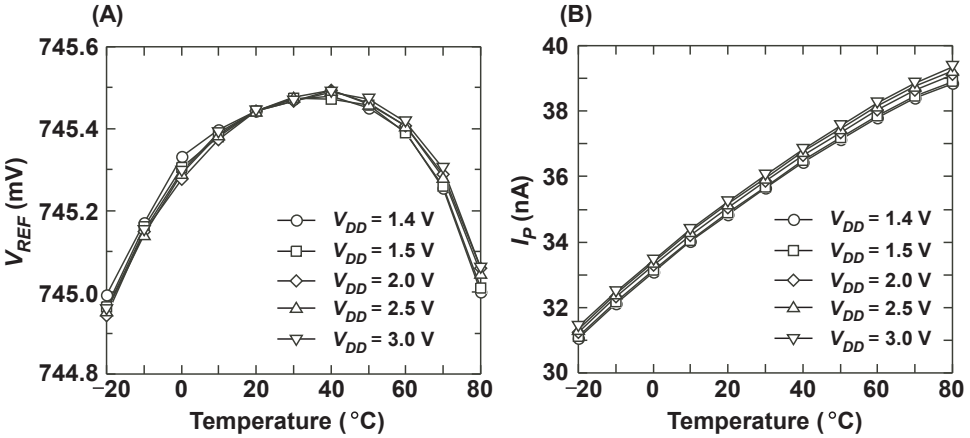


Fig. 10. (A). Measured output voltage V_{REF} as a function of temperature, with various supply voltages. Temperature coefficient was 7 ppm/°C and the supply regulation was 20 ppm/V. (B). Measured current I_P as a function of temperature for different supply voltages.

Table I summarizes the characteristics of our circuit [13] in comparison with other low-power CMOS voltage references reported in [8]-[12]. Our device is comparable to other circuits in power dissipation, PSRR, and chip area, and it is superior to others in T.C. and line sensitivity. Our circuit is therefore useful as a voltage reference for power-aware LSIs.

	This work [13]	JSSC '03 [8]	VLSI Symp. [9]
Process	0.35-μm, CMOS	0.6-μm, CMOS	0.35-μm, CMOS
Temperature range	–20 - 80℃	0 - 100℃	0 - 80℃
V_{DD}	1.4 - 3 V	1.4 - 3 V	1.5 - 4.3 V
$\overline{V_{REF}}$	745 mV	309 mV	891 mV
Power	0.3 μW(@1.4 V) Room temp.	29 μW(@3 V) Max. temp.	0.12 μW(@1.5 V) Room temp.
T.C.	7 ppm/℃	36.9 ppm/℃	12 ppm/℃
Line regulation	20 ppm/V	800 ppm/V	4600 ppm/V
PSRR	–45 dB(@100 Hz)	–47 dB(@100 Hz)	–59 dB(@100 Hz)
Chip area	0.055 mm^2	0.055 mm^2	0.015 mm^2

	Elec. Lett. '05 [10]	TCAS-II [11]	JSSC '07 [12]
Process	0.35-μm, CMOS	0.18-μm, CMOS	0.35-μm, CMOS
Temperature range	0 - 70℃	20 - 120℃	0 - 80℃
V_{DD}	1.4 - 3 V	0.85 - 2.5 V	0.9 - 4 V
$\overline{V_{REF}}$	579 mV	221 mV	670 mV
Power	4.6 μW(@2 V) N.A.	3.3 μW (@0.85 V) Average	0.036 μW (@0.9 V) Room temp.
T.C.	62 ppm/℃	271 ppm/℃	10 ppm/℃
Line regulation	6700 ppm/V	9000 ppm/V	2700 ppm/V
PSRR	–84 dB(@1 kHz)	N.A.	–47 dB(@100 Hz)
Chip area	0.126 mm^2	0.24 mm^2	0.045 mm^2

Table 1. Comparison of reported low-power CMOS voltage reference circuits

4.4.2 Discussion

Our circuit has several possible applications. The output voltage of our circuit can be used as a monitor signal for the D2D process variation in MOSFET threshold voltage because the output voltage is equal to the 0-K threshold voltage of MOSFETs in an LSI chip and is linearly dependent on the V_{TH} variation, as shown in Fig. 9-(A). This output voltage can be used to compensate for the threshold voltage variation in LSI chips. For example, consider the application to a reference current source. The process variation of the current I_P flowing in the circuit as shown in Fig. 8 (see Eq. (30)) can be expressed as

$$\frac{\Delta I_P}{I_P} = \frac{1}{I_P}\left(\frac{\partial I_P}{\partial \mu}\Delta\mu + \frac{\partial I_P}{\partial C_{OX}}\Delta C_{OX} + \frac{\partial I_P}{\partial \kappa}\Delta\kappa\right)$$

$$= \frac{\Delta\mu}{\mu} + \frac{\Delta C_{OX}}{C_{OX}} + \frac{\Delta\kappa}{\kappa}. \tag{32}$$

The current is independent of the threshold voltage variation. Although the current depends on the variation of the mobility $\Delta\mu/\mu$, gate-oxide capacitance $\Delta C_{OX}/C_{OX}$, and the temperature coefficient of the threshold voltage $\Delta\kappa/\kappa$, these variations are far smaller than the threshold voltage variation.

This way, the circuit can be used as an elementary circuit block for on-chip D2D process compensation systems, such as process- and temperature-compensated current references [27].

5. Overview of low-power current reference circuits

Current references with nanoampere-order currents are required to ensure circuit operation that is stable and highly precise, because power dissipation and performance of circuits are determined mainly by their bias currents. Nanoampere-current references for ultra-low-power LSIs have been reported in several papers [13]-[15]. The next sections provide an overview of the reported nanoampere current reference circuits.

5.1 Current references based on weak and strong inversion regions of MOSFETs

Sansen *et al.* developed a current reference circuit without resistors as shown in Fig. 11 [14]. Transistors M_2–M_{11} operate in the subthreshold region, and M_1 and M_{12} operate in the strong inversion region. The gate-source voltages of M_1–M_{12} form a closed loop, so we find that

$$V_{GS1} = V_{GS12}+V_{GS10}-V_{GS11}+V_{GS8}-V_{GS9}+V_{GS6}-V_{GS7}+V_{GS4}-V_{GS5}+V_{GS2}-V_{GS3}. \tag{33}$$

Assuming that the body effects of M_2–M_{10} are ignored, the output current I_{REF} is given by

$$I_{REF} = \frac{\beta}{2}\eta^2 V_T^2 \ln^2\left(120\cdot\frac{K_{11}K_9K_7K_5K_3}{K_{10}K_8K_6K_4K_2}\right)\left(\frac{K_1K_{12}}{K_{12}-K_1}\right). \tag{34}$$

The T.C. of the reference current is given by

$$T.C. = \frac{1}{I_{REF}}\frac{dI_{REF}}{dT} = \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{V_T^2}\frac{dV_T^2}{dT} = \frac{2-m}{T}. \tag{35}$$

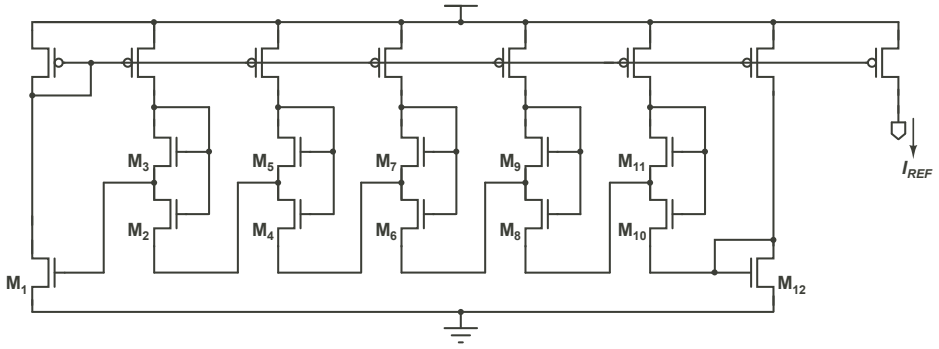


Fig. 11. Simplified schematic of current reference circuit without resistors [14]. Transistors M_2–M_{11} are operated in the subthreshold region, and M_1 and M_{12} are operated in the strong inversion region.

In a standard CMOS process, the mobility temperature exponent m is 1.5. Therefore, the output current has positive temperature dependence. As reported in [14], a measured temperature coefficient of 375 ppm/°C and a power dissipation of 10 μW were obtained, but the power dissipation is still large for use with sub-microwatt operation. Additionally, although the bias current of transistors M_2–M_{11} and M_1, M_{12} have the same value, nanoampere-order current, each transistor operates in a different region of the MOSFET. So, designs with careful transistor sizing and transistor matching are required.

5.2 Current references based on square root circuit

Lee *et al.* proposed a current reference circuit based on a square root circuit as shown in Fig. 12 [15]. Transistors M_1–M_4 operate in the subthreshold region, and other transistors operate in the strong inversion region. The gate-source voltages for the four MOSFETs (M_1 through M_4) form a closed loop, so we find that $V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4}$. From the translinear principle [26], we can obtain

$$I_{REF} = \sqrt{\frac{K_3 K_4}{K_1 K_2} \cdot I_1 \cdot I_2}. \tag{36}$$

Current I_1 is determined by the gate-source voltages of M_5, M_6, and M_7. We find that $V_{GS7} + V_{GS6} = V_{DD} - V_{GS5}$, so current I_1 can be given by

$$I_1 = \frac{\beta (V_{DD} - 3V_{TH})^2}{2(1 + 2\sqrt{K_5 / K_6})^2} \tag{37}$$

where K_6=K_7 is assumed.

The β-multiplier self-biasing circuit consisting of M_{16}–M_{19} and a resistor R generates current I_2. From $V_{GS18} = V_{GS16} + I_2 R$, current I_2 is given by

$$I_2 = \frac{2}{\beta R^2}\left(1 - \sqrt{K_{18} / K_{16}}\right)^2. \tag{38}$$

From Eqs. (36), (37), and (38), the output current can be rewritten as

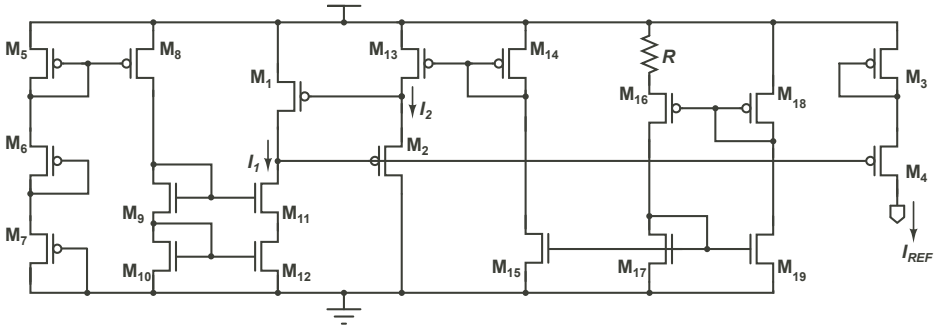


Fig. 12. Current reference circuit based on square root circuit [15]. Transistors M_5–M_{12} generate I_1, and transistors M_{13}–M_{19} generate I_2.

$$I_{REF} = \sqrt{\frac{K_3 K_4}{K_1 K_2}} \cdot \frac{1-\sqrt{K_{18}/K_{16}}}{1+2\sqrt{K_5/K_6}} \cdot \frac{V_{DD}-3V_{TH}}{R}. \tag{39}$$

Resistor R is an on-chip diffusion resistor, so the temperature dependence of the resistor is given by $R = R_0(1 + \alpha T)$, where R_0 is the resistance value at absolute zero temperature, and α is the temperature coefficient of the resistor. The T.C. of the output current can be expressed by

$$\begin{aligned} T.C. &= \frac{1}{I_{REF}}\frac{dI_{REF}}{dT} \\ &= (1+\alpha T)\frac{d}{dT}\left(\frac{1}{1+\alpha T}\right) + \frac{1}{(V_{DD}-3V_{TH})}\frac{d(V_{DD}-3V_{TH})}{dT} \\ &= -\frac{\alpha}{1+\alpha} + \frac{3\kappa}{V_{DD}-3V_{TH}}. \end{aligned} \tag{40}$$

As reported in [15], a measured T.C. of 230 ppm/°C was obtained. From Eqs. (39) and (40), however, the absolute value of the current and the T.C. depend strongly on the supply voltage V_{DD} and the threshold voltage V_{TH}.

5.3 Current references based on self-biasing technique without resistors

Figure13-(A) shows a β multiplier self-biasing circuit [31]. The circuit has a simple configuration and generates a PTAT current. However, the circuit requires large resistance of the resistor to reduce the operation current. To solve this problem, Oguey *et al.* developed a modified β multiplier self-biasing circuit that uses a MOS resistor, M_3, instead of ordinary resistors as shown in Fig. 13-(B) [16]. The gate-source voltage for MOS resistor M_3 is generated by a diode-connected transistor M_4. Transistors M_1 and M_2 operate in the subthreshold region. MOS resistor M_{R1} operates in a strong-inversion, deep-triode region, and the diode-connected transistor M_4 operates in the strong-inversion, saturation region.
The drain currents I_3 and I_4 in M_3 and M_4 are given by

$$I_3 = K_3\beta(V_{GS}-V_{TH})V_{DS3}, \tag{41}$$

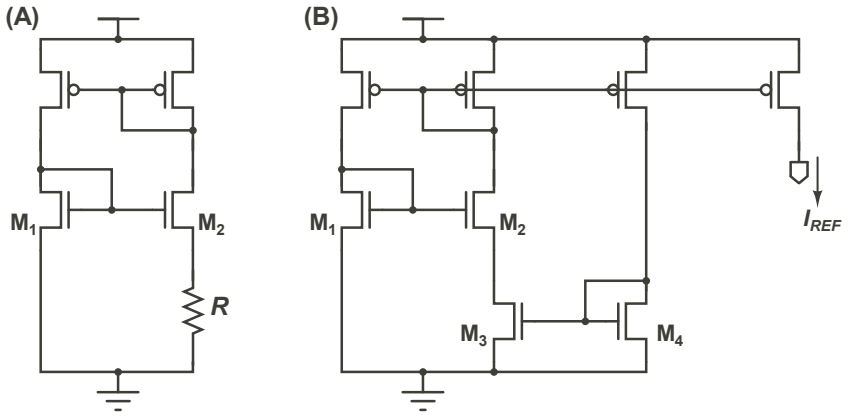


Fig. 13. (A). β-multiplier self-biasing circuit [31]. (B). Current reference circuit based on self-biasing circuit without resistors [16]. Transistors M_1 and M_2 operate in the subthreshold region, M_3 operates in the strong inversion, triode region, and M_4 is operated in the strong inversion, saturation region.

$$I_4 = \frac{K_4\beta}{2}(V_{GS} - V_{TH})^2. \tag{42}$$

The gate-source voltages of transistors M_3 and M_4 have the same value, so the output current can be expressed by

$$I_{REF} = K_3\beta\sqrt{\frac{2I_{REF}}{K_4\beta}}V_{DS} = \frac{2K_3^2\beta}{K_4}\eta^2V_T^2\ln^2(K_2 / K_1). \tag{43}$$

The temperature coefficient of the reference current is given by

$$T.C. = \frac{1}{I_{REF}}\frac{dI_{REF}}{dT} = \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{V_T^2}\frac{dV_T^2}{dT} = \frac{2-m}{T}. \tag{44}$$

Therefore, the output current has positive temperature dependence. In other words, the T.C. of the current will never be zero. As reported in [16], a measured temperature coefficient of 1100 ppm/°C was obtained. Note that the transistors M_1–M_2, M_3 and M_4 operate in different regions of the MOSFET with the same current value, which is on the order of nanoamperes. So, designs with careful transistor sizing and transistor matching using large-sized transistors are required.

5.4 Current references consisting of subthreshold MOSFETs

Figure 14 shows the current reference circuit we proposed [18]. The circuit consists of a bias-voltage subcircuit and a current-source subcircuit. The bias-voltage subcircuit is a modified β multiplier self-biasing circuit as reported in [16]. Bias voltage V_B for MOS resistorM_3 is generated by a diode-connected transistor M_4. The current-source subcircuit accepts bias voltage V_B and generates reference current I_{OUT} that is independent of temperature and supply voltage. All MOSFETs operate in the subthreshold region except for M_3 and M_4.

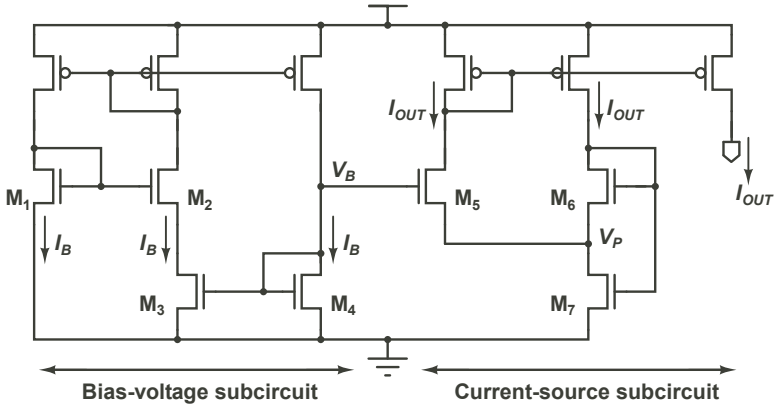


Fig. 14. Schematic of our current reference circuit [18]. All MOSFETs operate in the subthreshold region except for M_3 and M_4.

The current I_B is determined by the gate-source voltages of M_1 and M_2, and the drain-source voltage of M_3, so, we arrive at expression

$$I_B = \frac{V_{DS3}}{R_{M_3}}$$

$$= K_3 \mu C_{OX} (V_B - V_{TH}) \eta V_T \ln(K_2 / K_1) \tag{45}$$

for current I_B. Diode-connected transistor M_4 operates in the strong inversion and saturation regions. Its drain current I_B is given by

$$I_B = \frac{K_4 \mu C_{OX}}{2} (V_B - V_{TH})^2. \tag{46}$$

Because current I_B of M_3 is equal to I_B of M_4 (i.e., Eq. (45) = Eq. (46)), V_B is given by

$$V_B = V_{TH4} + \frac{2K_3}{K_4} \eta V_T \ln(K_2 / K_1). \tag{47}$$

Output current I_{OUT} through transistor M_5 can be given by

$$I_{OUT} = K_5 I_0 \exp\left(\frac{V_B - V_P - V_{TH5}}{\eta V_T} \right). \tag{48}$$

The source voltage V_P of transistor M_5 operated in the subthreshold region can be given by

$$V_P = V_{GS7} - V_{GS6}$$

$$= \eta V_T \ln(2K_6 / K_7) - \delta V_{TH76} \tag{49}$$

where δV_{TH76} is the difference between the threshold voltages of M_6 and M_7 with different transistor sizes (including the body effect in the transistors). From Eqs. (47), (48), and (49), we find that

$$I_{OUT} = I_0 \exp\left(\frac{\delta V_{TH}}{\eta V_T}\right)\frac{K_5 K_7}{2K_6}\left(\frac{K_2}{K_1}\right)^{2K_3/K_4} \tag{50}$$

where δV_{TH}(= $V_{TH7} + V_{TH4} - V_{TH6} - V_{TH5}$) is the difference between the threshold voltages of transistors M_4–M_7. The value of δV_{TH} depends on the transistor sizes [28],[29]. This way, we can obtain a reference current with nanoampere-order.
The temperature coefficient (T.C.) of the output current I_{OUT} is given by

$$\begin{aligned} T.C. &= \frac{1}{I_{OUT}}\frac{dI_{OUT}}{dT} \\ &= \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{V_T^2}\frac{dV_T^2}{dT} + \frac{1}{\exp\left(\frac{\delta V_{TH0}}{\eta V_T}\right)}\frac{d\exp\left(\frac{\delta V_{TH0}}{\eta V_T}\right)}{dT} \\ &= \frac{2 - m - (\delta V_{TH0} / \eta V_T)}{T} \end{aligned} \tag{51}$$

where δV_{TH0}(= $V_{TH07} + V_{TH04} - V_{TH06} - V_{TH05}$) is the difference between the threshold voltages at 0 K of transistors M_4–M_7. Therefore, the condition for a zero temperature coefficient can be given by

$$2 - m - (\delta V_{TH0} / \eta V_T) = 0. \tag{52}$$

Because the difference between the threshold voltages δV_{TH0} is insensitive to temperature, adjusting δV_{TH0} to an appropriate value will provide a zero T.C. at room temperature. Figure 15-(A) shows the calculated T.C. in Eq. (51) as a function of temperature with δV_{TH0} as a parameter. The mobility temperature exponent m was set to 1.5, and the subthreshold slope factor η was set to 1.3 [19; 30]. The T.C.s in the circuits reported in [13; 14; 16] are also plotted for comparison. The reported circuits [13; 14; 16] have a positive T.C. in a temperature range from –20 to 80°C, and these T.C.s will never be zero. On the other hand, our circuit can achieve a zero T.C. current at δV_{TH0}=17 mV and at room temperature.
In this way, we can obtain a zero T.C. current by setting an appropriate δV_{TH0}. The value of δV_{TH0} can be adjusted by the transistor sizes [28; 29].
Next, let us consider the effect of process variations on the output current. The process variations of the output current I_{OUT} can be expressed as

$$\begin{aligned} \frac{\Delta I_{OUT}}{I_{OUT}} &= \frac{1}{I_{OUT}}\left(\frac{\partial I_{OUT}}{\partial \mu}\Delta\mu + \frac{\partial I_{OUT}}{\partial \delta V_{TH}}\Delta\delta V_{TH}\right) \\ &= \frac{\Delta\mu}{\mu} + \frac{\Delta\delta V_{TH}}{\eta V_T}. \end{aligned} \tag{53}$$

The mobility variation is generally smaller than the threshold voltage variation, so the output current depends mainly on $\Delta\delta V_{TH}/\eta V_T$, which is the variation of the threshold-voltage difference between transistors in a chip. Therefore, reducing WID variation is important in our device. The WID variation can be reduced by using large-sized transistors [23] and various analog layout techniques [24].

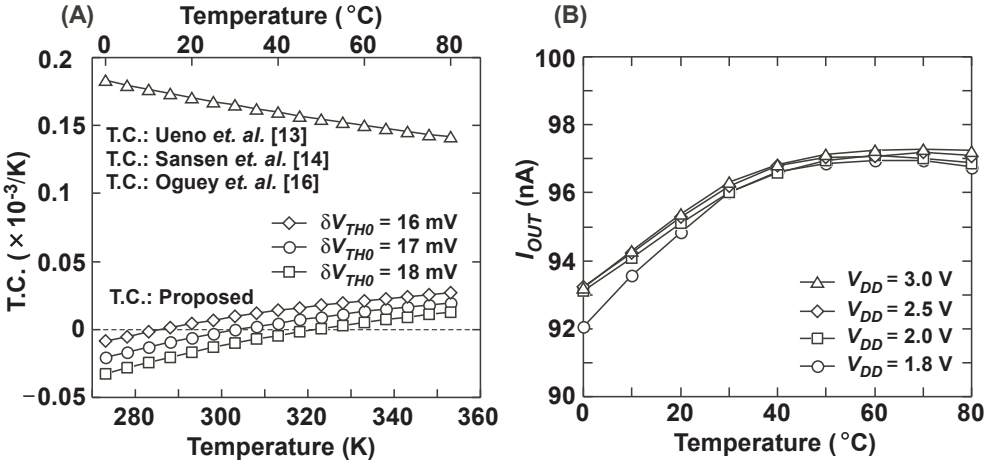


Fig. 15. (A). Calculated T.C.s of output currents as a function of temperature, with various δV_{TH0}; theoretical values obtained from Eqs. (31), (35), (44), and (51). (B). Measured output current I_{OUT} as a function of temperature with various supply voltages. T.C. was 520 ppm/°C.

5.4.1 Experimental results

We fabricated a prototype chip using a 0.35-μm, 2-poly, 4-metal standard CMOS process, and we designed the circuit so as to produce a 100-nA output current.

Figure 15-(B) shows measured output current I_{OUT} as a function of temperature with supply voltage V_{DD} as a parameter. The power supply voltage was set in a range from 1.8 to 3 V. The output current was about 96 nA and almost constant at temperatures in a range from 0 to 80°C. The temperature dependence and temperature coefficient were 50 pA/°C and 520 ppm/°C. An almost-constant reference current was obtained over a wide temperature range. The line regulation was 0.2%/V in a supply range of 1.8 to 3 V.

Table II summarizes the characteristics of our device in comparison with other low-power CMOS current references reported in [13]-[18]. Our device is superior to others in chip area. In the circuits reported in [13]-[18], there are trade-offs between the power dissipations and the T.C. of the reference currents. Our device achieved an acceptable trade-off. The power dissipation of our device was 1 μW at a 1.8-V power supply, and the load regulation was 0.02%/V.

6. Conclusion and discussion

In this chapter, overviews of previous reported low-power reference circuits and details of our circuits were provided. These circuits generate constant reference voltages and currents that are independent of supply voltage and temperature. However, to achieve sub-microwatt operation in circuits that consist of MOSFETs and resistors, they require resistors with a high resistance of several hundred mega ohms. Such a high resistance needs a large area to be implemented, and this is quite inconvenient for practical use in ultra-low power LSIs. Therefore, reference circuits for sub-microwatt operation have to be implemented without the use of resistors.

	This work [18]	JSSC '09 [13]	JSSC '88 [14]
Process	0.35-μm, CMOS	0.35-μm, CMOS	3-μm, CMOS
Temperature range	0 - 80℃	–20 - 80℃	0 - 80℃
V_{DD}	1.8 - 3 V	1.4 - 3 V	$\geq$3.5 V
$\overline{I_{OUT}}$	96 nA	36 nA	774 nA
Power	1 μW(@1.8 V) Room temp.	0.3 μW(@1.5 V) Room temp.	10 μW(@5 V) N.A.
T.C.	520 ppm/℃	2200 ppm/℃	375 ppm/℃
Line regulation	0.2%/V	0.002%/V	0.015%/V
Load regulation	0.02%/V	N.A.	0.004%/V
Chip area	0.014 mm^2	0.06 mm^2	0.2 mm^2

	Elec. Lett. '96 [15]	JSSC '97 [16]	TCAS-II '05 [17]
Process	2-μm, CMOS	2-μm, CMOS	1.5-μm, CMOS
Temperature range	0 - 75℃	–40 - 80℃	–20 - 70℃
V_{DD}	5 V	$\geq$1.2 V	$\geq$1.1 V
$\overline{I_{OUT}}$	285 nA	1 - 100 nA	0.41 nA
Power	N.A. N.A.	0.07 μW(@2.3 V) Room temp.	0.002 μW(@1.1 V) N.A.
T.C.	230 ppm/℃	1100 ppm/℃.	2500 ppm/℃
Line regulation	N.A.	10%/V	6%/V
Load regulation	N.A.	N.A.	N.A.
Chip area	N.A.	0.06 mm^2	0.046 mm^2

Table 2. Comparison of reported low-power CMOS current reference circuits

In the voltage reference circuits, reference voltages based on the difference between the threshold voltages (ΔV_{TH}), the difference between the gate-source voltages (ΔV_{GS}), and the threshold voltage at 0 K (V_{TH0}) have been proposed. However, the reference circuits based on ΔV_{TH} require a multiple-threshold voltage process, and the temperature dependence of the reference circuits based on ΔV_{GS} cannot be canceled for a wide temperature range. Therefore, these are unsuitable for practical use in ultra-low power LSIs. The voltage reference circuits based on V_{TH0} are promising circuit configurations because of their simple circuitries, sub-microwatt operation, and reference voltages that are insensitive to temperature over a wide temperature range. In our prototype, the T.C. and line regulation of the output voltage were 7 ppm/°C and 20 ppm/V and a power dissipation of 0.3 μW was obtained. However, because the absolute value of the reference voltages changes with the process variations of the threshold voltage, the circuit cannot be used as a reference voltage in conventional circuit systems. Therefore, the circuits require calibration techniques such as programmable MOS transistor arrays or adjustment of the bulk voltage of the MOSFET. Because the temperature dependence of the reference voltages can be canceled, one-point calibration techniques will enable us to compensate for process variations.

As other applications, because the output voltage shows a linear dependence on the threshold voltage variation, the reference voltage can be utilized as a D2D process variation signal for the techniques to compensate for the threshold voltage variation in an LSI chip.

Current reference circuits consisting of MOSFET circuits operating in the strong inversion region and the subthreshold region have been proposed. Because each MOSFET in the circuits operates in a different region with the same current value, which is on the order of

nanoamperes, careful transistor sizing and reducing WID variation in the design are important. The WID variation can be reduced by conventional circuit design techniques. In our circuit, techniques such as using large-sized transistors and common centroid layout were used to reduce the effect of the WID variation.

From the theoretical results in the reported current references, the reference currents have a positive temperature dependence. Therefore, the circuits cannot be used as reference current circuits in environments with temperature changes. To solve this problem, we developed a temperature compensated current reference circuit with simple circuitry and a small area, and fabricated a prototype chip that generates a 100-nA output current. The T.C. and line regulation of the output current were 520 ppm/°C and 0.2%/V. A power dissipation of 1 μW was obtained.

These circuits will be useful as voltage and current reference circuits for subthreshold-operated, power-aware LSI applications such as RFIDs, mobile devices, implantable medical devices, and smart sensor networks.

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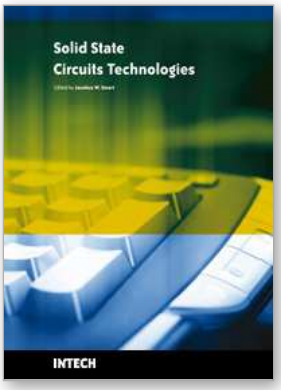

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The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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