Chapter 7

Implantable Biomedical Devices

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Additional information is available at the end of the chapter

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1. Introduction

Almost a decade after the invention of the first semiconductor transistor in 1948, it took around a decade for the revolutionary technology to evolve from producing single devices to the integration of a few transistors as the first *integrated circuit* in 1958. Since then, integrated circuits have been in continuous progress for more than half a century as predicted by the well-known *Moore's law*. While integrated circuits still continue their progress with the same exponential pace, it is almost a decade that a new branch of science and technology has emerged, known as *integrated microsystems*. This can be taken as the natural technological evolution from individual circuit chips and non-circuit modules, e.g., microelectromechanical systems (MEMS) devices, and subsequently to complete systems in small physical dimensions and with light weight. Integrated microsystems have opened windows of hope to providing efficient solutions to some of the problems that have not been resolvable by any other means so far.

Among the many kinds of microsystems being developed for a wide variety of applications, *implantable biomedical microsystems* are of increasing interest to both medical and engineering communities. This is mainly because of the capabilities such devices are expected to provide on the medical side, and also the technical challenges available on the engineering side. Examples of biomedical implants are pacemakers, cochlear implants, visual prostheses, neural recording microsystems, and deep brain stimulators.

This chapter provides an introduction to visual prostheses and intra-cortical neural recording devices. These are, indeed, two types of implantable biomedical microsystems, which are on the forefront of research.

2. Neural recording microsystems

Nowadays, several neural recording approaches, *e.g.*, electro-encephalography (EEG) and magnetic resonance imaging (MRI), are widely used as successful medical diagnostic

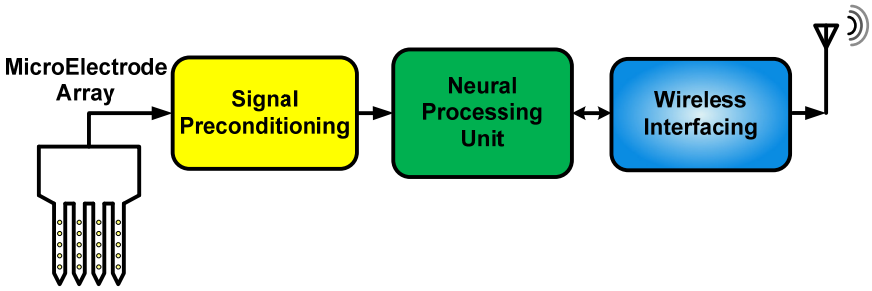

Figure 1. Simplified block diagram of a typical implantable neural recording microsystem

methods. What makes these approaches attractive is the fact that they are non-invasive, meaning that they do not make any harm to the subject. These methods, however, are capable of reporting averaged neural activities in the brain. In some branches of advanced research, for instance in medical sciences, cognitive sciences, and in brain-machine interfacing, researchers and scientists need to record neural activities with much higher spatial resolution than what the aforementioned non-invasive approaches are capable of providing. This section reviews general aspects of extracellular neural recording microdevices designed to intra-cortically record neural activities with rather high spatial resolution. Development of such devices is indeed an interesting example of multi-disciplinary research as it brings together several different specialties, such as electrical engineering, microfabrication technology, material sciences, chemical engineering, signal processing, and neuroscience.

As illustrated in the simplified block diagram of Figure 1, an implantable neural recording microsystem generally comprises one or more recording probes, a signal preconditioning module, a neural processing unit, and a wireless interfacing module.

2.1. Analog signal preconditioning (analog front-end)

In intra-cortical neural recording, electrical signals sensed by recording probes (also known as electrode arrays or microelectrode arrays (MEAs) when recording multiple channels) contain two different types of neural information: *Action Potentials* (APs) and *Local Field Potentials* (LFPs). Action potentials represent the firings of individual neurons, while local field potentials exhibit averaged synaptic activities of the mass of neurons in vicinity of electrode arrays. The former contains frequencies from 100 Hz to around 10 kHz with up to hundreds of μV of amplitude [1], and the latter contains frequencies from 0.01 Hz to around 200 Hz with amplitudes sometimes as large as a few mV [2].

The main task of a neural signal preconditioning module is the amplification of weak neural signals as well as filtering out frequencies beyond the bandwidth of interest. This is usually done using a preamplifier followed by or combined with a bandpass filter. In some cases, both gain and cut-off frequencies of the signal preconditioning module are either programmable or at least tunable.

2.1.1. Neural amplifier design parameters

As an important part of the signal preconditioning module, neural amplifiers need to be designed carefully. This is because they significantly contribute to the quality of the signals recorded in terms of the strength of the neural activities recorded and also their signal-to-noise ratio. As a result, neural amplifiers are designed with high enough mid-band gain and low input-referred noise. Considering the fact that in high-density neural recording per-channel amplifiers are used, it is of crucial importance to design these amplifiers with low power consumption and small silicon area. Key design parameters for neural amplifiers are therefore briefly reviewed as follows:

- **Noise**
  In intra-cortical extracellular neural recording peak-to-peak amplitude of action potentials at the input of the signal preconditioning module is in the order of tens to hundreds of microVolts. As a result, input-referred noise of neural amplifiers for this type of recording is typically kept below 5-30 μV [3].
  Input-referred noise of a neural amplifier has two main components: *thermal* noise and *flicker* noise. The former is caused by recording electrodes and amplifier transistors, and the latter is caused by existing amplifier transistors. The thermal noise component can be reduced by choosing larger transconductance for the transistors used at the input of the neural amplifier. In low-frequency applications such as neural recording, extra care should be taken to keep the flicker noise low. This is because flicker noise significantly increases at low frequencies. There are two techniques used to reduce the contribution of the flicker noise component in the input-referred noise. As a device-level technique, *pMOS* transistors with considerably large channel area are used as the amplifier input transistors. As a circuit-level technique, *Chopper* technique is used to eliminate both the offset of the amplifier and the flicker noise component, which are both of low-frequency nature [4]. To implement this technique an auxiliary amplifier and a few integrated capacitors are needed, which makes it difficult to achieve low flicker noise, low power consumption, and small silicon area occupation at the same time.

- **Silicon area**
  As a general prerequisite for being implantable, neural amplifiers need to be small in physical dimensions. This consideration becomes much more important when designing implantable microsystems to record tens to hundreds (and even thousands) of neural signals in parallel. A neural amplifier is therefore expected to consume small chip area and contain no off-chip components.

- **Power**
  For a neural amplifier, consuming as low power as possible is of importance from two standpoints. First, affordable power budget for the operation of implantable microsystems are limited, whether they are battery operated or telemetry powered. Secondly, from a biological point of view, the heat generated by the circuits that dissipate rather large power can potentially cause damage to the neighboring living

tissues [5]. However, there exists a sever trade-off between the noise of a circuit and its power consumption. In other words, for a specific level of noise, power consumption of a neural amplifier cannot be reduced as much as the circuit designer wishes.

- **NEF**
  Noise Efficiency Factor (NEF) is a Figure of merit that expresses how well the trade-off between the power consumption and the input-referred noise level is considered in the design of a circuit [6]. For a neural amplifier, NEF is given as:

$$NEF = V_{ni.rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}}$$

  where $V_{ni,rms}$ is the input referred noise, I_{tot} is the total current the amplifier draws from the power supply, U_T is the thermal voltage (KT/q), and BW is the bandwidth of the amplifier. Achieving small values for the NEF of a circuit means that the circuit has been designed efficiently in terms of obtaining low input-referred noise and consuming small power.

- **Input offset voltage**
  To exhibit ideal operation, differential amplifiers need to be designed and implemented symmetrically, both in topology and from the standpoint of the components they contain. This is, of course, the ideal case, which is never expected to happen in the real world, and neural amplifiers are not exceptions. In reality, asymmetric implementation and operation of such amplifiers causes a slight shift in the input-output transfer characteristics of the amplifier, which is modeled as the *offset voltage*.

- **Output voltage swing**
  Output voltage swing of a neural amplifier needs to be as wide as possible in order to allow for the proceeding signal processing to be performed more precisely. This issue becomes more critical as the microfabrication technology is being continually scaled down, resulting in smaller supply voltages, and demanding for the employment of low-voltage circuit design techniques in order to provide enough room for the amplified neural signal to swing.

- **Cut-off frequency**
  Frequency contents of action potentials in a typical intra-cortically recorded neural signal is spread from 100 Hz to around 10 KHz, while that of local field potentials is usually located in the sub-Hz up to a few tens of Hz. Neural amplifiers are designed with a low cut-off frequency of below 1 Hz or around 100 Hz depending on whether LFPs are to be amplified or not. Upper cut-off frequency for a neural amplifier is usually set somewhere between 7 KHz and 10 KHz.

- **CMRR**
  To discriminate between the signal of interest and the non-useful common-mode components of the input signal, (*e.g.*, certain kinds of motion artifacts, noise components induced at the input, and low-frequency variations resulted from probe-

tissue electrochemical interactions) neural amplifiers usually need to have high *common-mode rejection ratio (CMRR)*.

- **PSRR**
  As explained before, input signal to neural amplifiers is very weak in amplitude, typically in the order of tens to hundreds of microVolts. On the other hand, implantable neural recording microsystems are usually powered via power telemetry. As a result, the supply voltage in such systems is susceptible to some voltage ripples and even fluctuations, which can easily be significantly larger than the input signal. Hence, it is of crucial importance for neural amplifiers to have a high *power-supply rejection ratio (PSRR)* in order to suppress supply voltage variations while amplifying the input neural signal by a rather large gain.

2.1.2. Different types of neural amplifiers

It is because of the key role they play in the quality of signals recorded that a wide variety of techniques have been employed for the design of neural amplifiers. Hence, neural amplifiers can be categorized in different ways:

From the standpoint of *system-level architecture*, neural amplifiers can be classified into *feedback amplifiers* and *open-loop amplifiers*. Negative feedback is usually used in the design of amplifiers in order to benefit from some (or all) of the following advantages:

- desensitization of the closed-loop gain against variations of open-loop circuit parameters,
- improvement of the impedance seen into the input and output ports of the amplifier,
- improvement in the bandwidth of the amplifier, and
- improvement in the linearity of the amplifier.

The designer should, however, be aware of the undesired impact of the feedback used on the stability of the amplifier. As a common solution for this problem, there are frequency compensation techniques that are used to stabilize the closed-loop amplifier as desired [7].

According to their *circuit-level architecture*, neural amplifiers also differ in the number of amplifying stages. Typically, a mid-band gain of about 40 dB to 60 dB, and a bandwidth of sub-Hz to 10 KHz are expected for a neural amplifier. Although sometimes a single-stage amplifier is a good choice but because of limited output voltage swing of cascode amplifiers and the lack of programmability of gain and bandwidth in a single-stage amplifier, there is a tendency to use two- or multi-stage amplifiers. One of the best choices for state-of-the-art neural amplifiers is to use a *Low-Noise Amplifier* (LNA) in the first stage, and a second stage to achieve the required gain and bandwidth adjustment. If necessary, a third stage can be used to achieve programmable gain for the neural amplifier [8].

The *signaling approach* used in the design of the amplifier can classify neural amplifiers into *single-ended amplifiers* and *differential amplifiers*. Because of the benefits of differential circuits such as input common-mode DC voltage adjustment, the input stage of the most of neural

amplifiers is implemented differentially. But because of not necessity of very wide dynamic range for the neural amplifiers, although the fully-differential amplifiers have advantages such as twice output voltage swing, twice SNR, more linearity and higher CMRR and PSRR in comparison to their single-ended counterparts, but because of requirement of common-mode feedback loop and more power consumption, so the best choice for neural amplification applications is single-ended configuration.

From the *time-domain continuity* point of view, neural amplifiers are categorized into *continuous-time amplifiers* and *discrete-time amplifiers*. The switched-capacitor circuits are often introduced as discrete-time circuits. The most important advantages of switched-capacitor neural amplifiers in comparison to their continuous-time counterparts are, more accurate and adjustable frequency response, and wider dynamic range. In contrast, these circuits are slower at the same power and more silicon area occupier.

Also, *user-controllability* on the specifications of the amplifier (e.g., gain and bandwidth) can be used to classify neural amplifiers *programmable/tunable amplifiers* and *regular amplifiers*.

- Bandwidth Adjustment
  - Amplifiers with RC Filters
    The most common way of bandwidth adjustment for neural amplifiers is the use of resistor and capacitor to realize the filter. However, to achieve sub-Hz lower cut-off frequencies, very large resistors ($R > 10\ G\Omega$) are needed. Of course, this amount of resistance is achievable using diode-connected transistors, but not very linear. The Figure 2 shows the most common and simple single-stage feedback neural amplifier using an *Operational Transconductance Amplifier* (OTA), integrated resistors, and integrated capacitors. The voltage gain for this amplifier can be given as follows [9].

$$\frac{V_{out}}{V_{in}^{+}-V_{in}^{-}}=\frac{C_1}{C_2}\cdot\frac{1-sC_2/G_m}{\left(\frac{1}{sR_2C_2}+1\right)\left(s\frac{C_LC_1}{G_mC_2}1\right)}=A_M\frac{1-s/\left(2\pi f_z\right)}{\left(\frac{2\pi f_L}{s}+1\right)\left(\frac{s}{2\pi f_H}+1\right)}$$

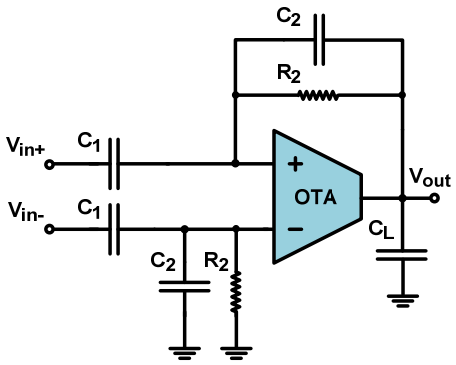

Figure 2. A simple single-stage neural amplifier with RC filter

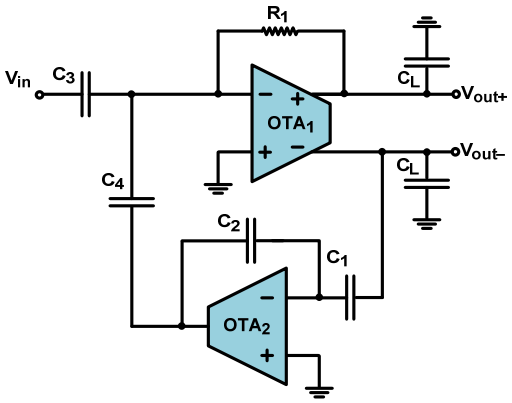

Figure 3. A single-stage neural amplifier with feedback filter

	BW (Hz)	Gain (dB)	NEF	$V_{ni,rms}$ (μV)	Fully Diff.	# of Stages	Supply (V)	Power (μW)	Tech. (μm)
Harrison 2003, [9]	0.025 – 7.2k	39.5	4	2.2	No	1	5	80	1.5
Mohseni 2004, [11]	50 – 9.1k	39.3	19.4	7.8	No	2	3	115	1.5
Heer 2006, [12]	10 – 100k	20	8.1	5.9	Yes	1	5	160	0.6
Wu 2006, [13]	0.003 – 245	40.2	3.8	2.7	No	1	1	2.3	0.35
Denison 2007, [14]	0.5 – 250	45.5	4.9	0.93	No	1	1.8	2.16	0.8
Yin 2007, [15]	0.015 – 4k	42.5	4.9	3.6	Yes	1	3.4	27.2	1.5
Wattanapanitch 2007, [16]	45 – 5.3k	40.9	2.7	3.1	No	2	2.8	7.56	0.5
Lee 2008, [17]	16 – 5.3k	40	NA	5.29	No	1	1.8	9	0.18
Yazicioglu 2008, [A18]	0.5 – 100	48	4.1	0.59	Yes	2	3	6.9	0.5
Mollazadeh 2009, [19]	94 – 8.2k	39.6	2.9	1.94	Yes	2	3.3	79.2	0.5
Yeager 2009, [20]	0.5 – 5.9k	39	4	4.4	No	2	1.8	5.94	0.5
Zhao 2009, [10]	13 – 8.9k	46	3.1	5.7	Yes	1	3	6	0.35
Shahrokhi 2010, [21]	10 – 5k	33	5.55	6.1	Yes	2	3	8.4	0.35
Rezaee-Dehsorkh 2011, [8]	300 – 10k	57.5	2.4	3	No	3	1.8	20.8	0.18

Table 1. Comparison of different neural amplifiers specifications

A sample of this amplifier can be found in [9] with a midband gain of 39.5dB, while occupying 0.16 mm^2 of silicon area in a 1.5-μm CMOS Technology, and consuming 80 μW of power from a 5-V supply. The input referred noise for that amplifier is about 2.2 μV_{rms}.

- Amplifiers with Feedback Filters
  One of the big problems of neural amplifiers with RC filters is the generating a big time constant to achieve sub-Hz lower cut-off frequency. To solve this problem, the lower cut-off frequency can be generated using the upper cut-off frequency of an auxiliary amplifier in the feedback path. One of these types of neural amplifiers has been presented in [10] which can be seen in the Figure 3. This amplifier has a midband gain of 46 dB, and bandwidth of 13 Hz to 8.9 KHz. It consumes about 6 μW of power from a 3-V supply. The input referred noise for this amplifier is about 5.7 μV_{rms}.

At the end, a specifications table of neural amplifiers from literature is presented for the comparison.

2.2. Architectures for multichannel neural recording microsystems

Advances in neuroscience and clinical applications demand for simultaneous recording of neural potentials from a numerous amount of electrodes in the cortex in integrated manner with low power and low noise. According to different neural recording microsystems reported in the literature, the architecture of the systems can be categorized based on several main parameters. The most significant difference between the neural recording microsystems is related to their recording mode. In general, it can be separated in two different categories: the *Monitoring* mode, and the *Scan* mode [22]. In the monitoring mode, the signals sensed from microelectrode array are passed through the neural signal preconditioning part (neural amplifier) and in the same form (or their compressed form) are modulated and prepared to be transmitted to the world of the outside of the implant.

Considering the need to know neural information from numerous channels and also the shortage of telemetry power for microsystems, and since monitoring of the neural signals is a power-and-area-hungry method of recording, so someone can send just the useful neural information to the outside. In contrast to neuroscientific research, where the study of exact wave form of the neural signals is important, in prosthetic applications just knowing of the occurrence rate of the neural spikes is sufficient [22]. In scan mode, just the existence of neural spikes is detected and the addresses of channels with detected spikes on them are sent to the outside of the microsystem.

The type of wireless transmission is depended upon the type of signal processing on the amplified and filtered out neural signals, whether analog or digital. In some of microsystems the signal processing is done in the analog domain to be sent in the same domain using an analog transmitter. The most important advantages of analog transmitter are lower energy consumption and less implementation complexity. The most commonly-used analog modulation scheme to design the *analog transmission* is *Frequency Modulation*

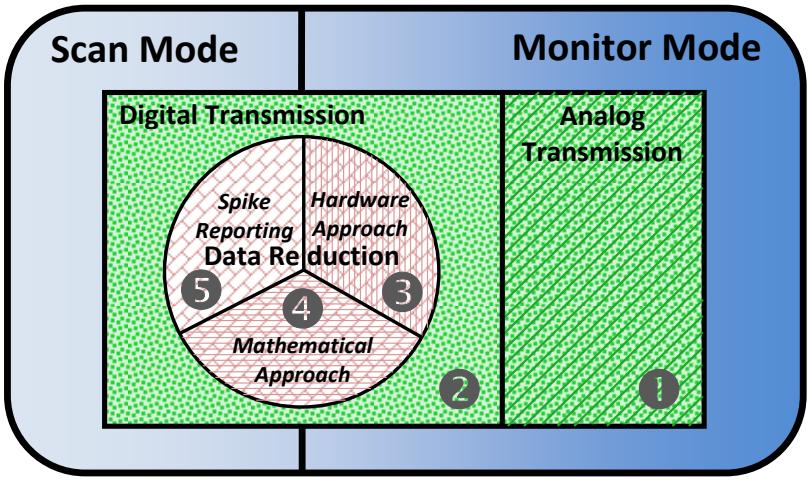

Figure 4. The general scope of architectures for multichannel neural recording microsystems

(FM) that is easily implantable. In contrast, the most important advantages of *digital transmission* are higher noise margin, detection and correction of errors, and easy synchronization between transmitter and receiver [23]. These parameters have returned the choice of designers to digital transceivers.

Ideally, it is desired an infinite accuracy for the recording and transmission implant system. Although this accuracy exists intrinsically in analog transmission systems, but considering the problem of noisy transmission, the equivalent accuracy, from the beginning of the system to the end, is not unlimited. Hence, digital transmission systems with appropriate accuracy are used. But aforementioned simple digital monitoring architectures are not useful when the number of recording channels exceeds. Therefore, according to the literature, three different techniques are introduced as *Data Reduction techniques* for implantable microsystem design: *spike reporting*, *mathematical approaches*, and *hardware approaches*. Hence, one of the other ways of categorizing the architectures for multichannel neural recording microsystems is to use or not to use the data reduction techniques. Figure 4 shows the general scope of categorizing the architectures for multichannel neural recording microsystems. So, there are five different architectures that are discussed in the following. However, it should be noticed that one of the other ways of division of these architectures is the choice of *Time-Domain Multiplexing* (TDM) or *Frequency-Domain Multiplexing* (FDM) to simultaneous recording from all the neural channels.

2.2.1. Monitor mode, analog transmission, without data reduction

In this architecture, after simultaneous per-channel passing of neural signals of all the recording channels from signal preconditioning part, neural samples on parallel channels using either time-domain multiplexing or frequency-domain multiplexing are converted to series samples in analog domain. The prepared analog samples are then transmitted using

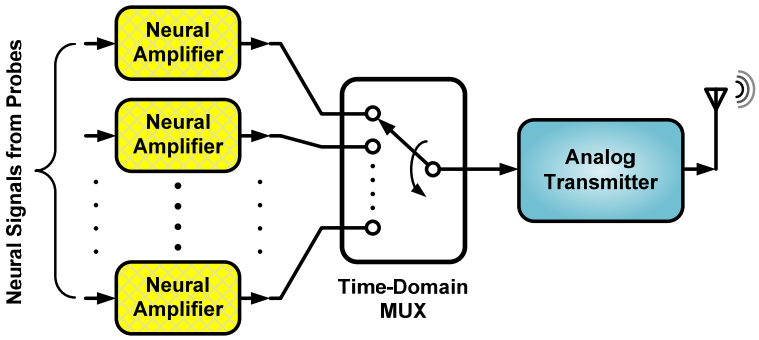

Figure 5. Monitor mode, analog transmission, without data reduction architecture with TDM

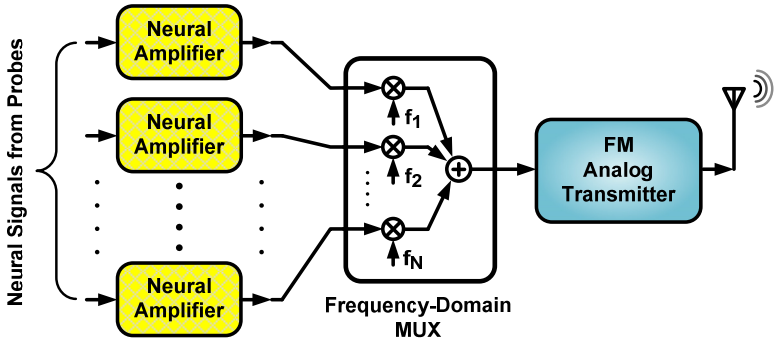

Figure 6. Monitor mode, analog transmission, without data reduction architecture with FDM

an analog transmitter (usually with FM modulation). One of the most important advantages of this kind of transmitters is low power consumption. However, here, the environment noise is very destructive. Figure 5 shows such an architecture using time-domain multiplexing. A sample of such an architecture was presented in 2005 for a 8-channel wireless FM neural recording microsystem [24].

But as previously mentioned, another technique to record all the neural channels simultaneously is frequency-domain multiplexing. For the first time, such a multichannel neural recording system was presented in [25]. Figure 6 depicts the mentioned architecture. The most important advantage of such an architecture over its TDM counterpart is its capability to recording from many more neural channels. But, of course, care should be taken in design and implementation of such architecture to avoid frequency interference.

2.2.2. Monitor mode, digital transmission, without data reduction

The difference between this architecture and the previous one is in the way of transmission, i.e., digital versus analog. Considering the advantages of digital transmission over analog one, after signal preconditioning, multiplexing in analog domain, the prepared samples are

converted to digital words. Then, these words along with parity bits and synchronization pulses are converted from parallel to serial form, and the prepared bit stream is then delivered to a digital transmitter. Figure 7 shows such a digital monitor architecture. The resolution of the quantization in neural recording systems is typically chosen to be 6 – 10 bits, and the sampling rate of the data converter is typically considered to be about production of 20 – 30 kS/s (twice to three times the Nyquist rate of neural signals) by the number of neural channels. A sample of this architecture is presented in [26].

Noting the low accuracy of multiplexing in analog domain, another possible change to the mentioned architecture can be as to use per-channel analog to digital converters for every neural channel before multiplexing and then to multiplex in digital domain. In this way the sampling rate of any ADC can be as low as 20 – 30 kS/s. Such an architecture (Figure 8) with delta-sigma ADCs is presented in [19], in which the ADCs' resolution and sampling rate are 7 bits and 20 KHz, respectively.

If we dedicate one ADC to every neural channel, then a big problem occurs if the number of channels exceeds. This big problem is large amount of power dissipation and great occupied silicon area related to all of the ADCs. To solve this problem, an approach was proposed by the authors in 2009 regarding the use of delta-sigma modulators instead of a complete ADC

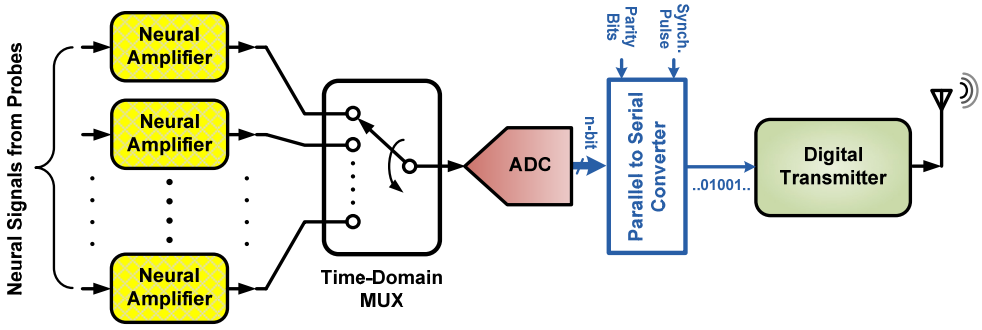

Figure 7. Monitor mode, digital transmission, without data reduction architecture

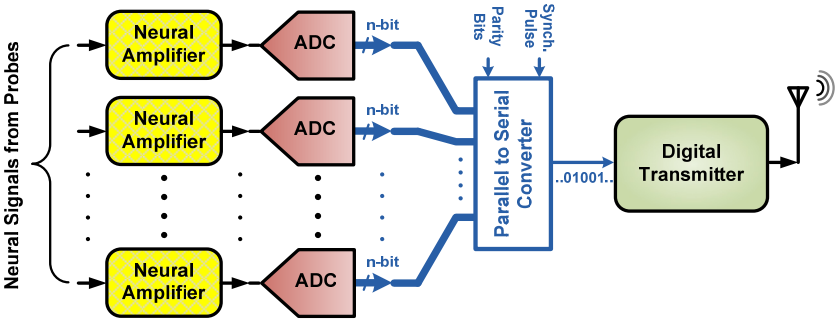

Figure 8. Monitor mode, digital transmission, without data reduction architecture with per-channel ADCs

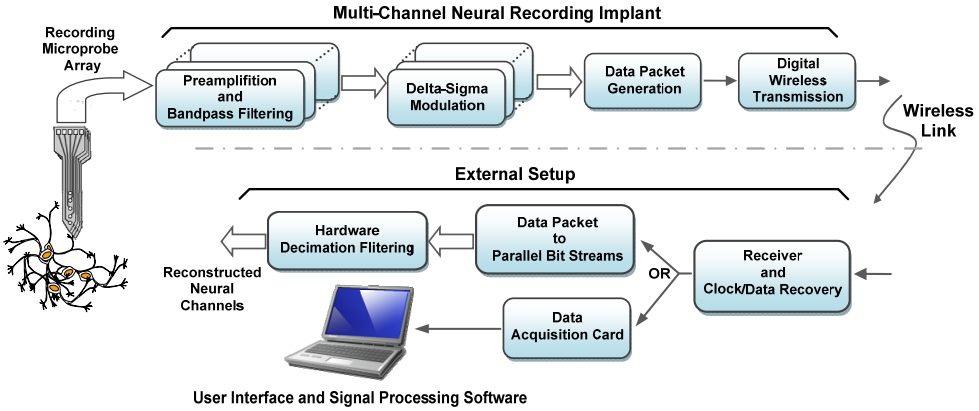

Figure 9. Monitor mode, digital transmission, without data reduction architecture based on delta-sigma modulators

in every channel [27]. In this method, the architecture of the ADC is indeed a delta-sigma one but with the difference that delta-sigma modulators are implemented in implant unit and the remained part of a delta-sigma ADC, i.e. decimation filtering, is implemented in the external unit (Figure 9). In this way, a large amount of power and silicon area is saved in the implant side. An 8-channel system is designed and laid-out in a 0.5-μm CMOS Technology. Post layout simulations showed a power consumption about 16.5 μW for every neural recording channel. The recording bandwidth was set to be 6.25 KHz and quantization resolution was considered to be about 8 bits.

2.2.3. Monitor mode, digital transmission, hardware approach data reduction

One of the other architectures that have been recently published promises the multichannel neural recording using Anti-Logarithmic ADCs [28]. The significant difference between this architecture and the architecture discussed in the previous section is in the type of ADC. It has been showed that, nonlinear (exponential) quantization of neural signals can be very more effective than the linear type and reduces the physical bits of the data converter comparing to its linear counterpart. This architecture is shown in Figure 10.

2.2.4. Monitor mode, digital transmission, mathematical approach data reduction

It can easily extract the useful information from neural signal using a data compressor based on *Wavelet Transform* or other useful discrete transforms. According to Figure 11, another architecture for multichannel neural recording microsystems can be realized. A 64-channel neural data compressor based on *Walsh-Hadamard Transform* is presented in [29] with a compression factor of 72. But a more efficient 64-channel neural data compressor based on *Discrete Haar-Wavelet Transform* is presented in [30] with a compression factor of 112, in which has been claimed that has a more simpler circuit in comparison with the work in [29]. Anyway, data compressor approach is a power-and-area-hungry one.

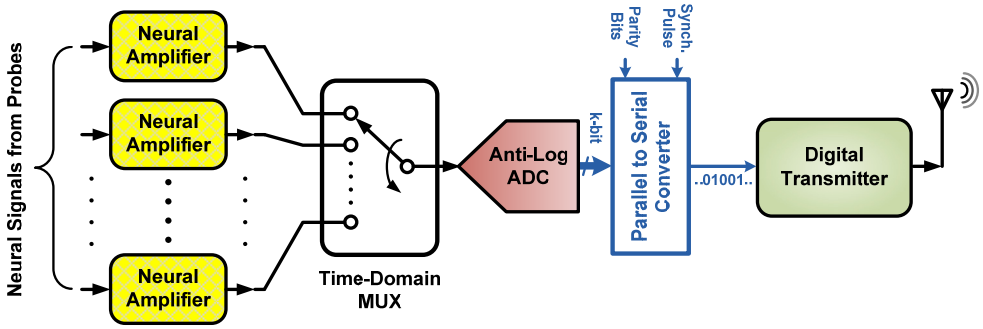

Figure 10. Monitor mode, digital transmission, hardware approach data reduction architecture

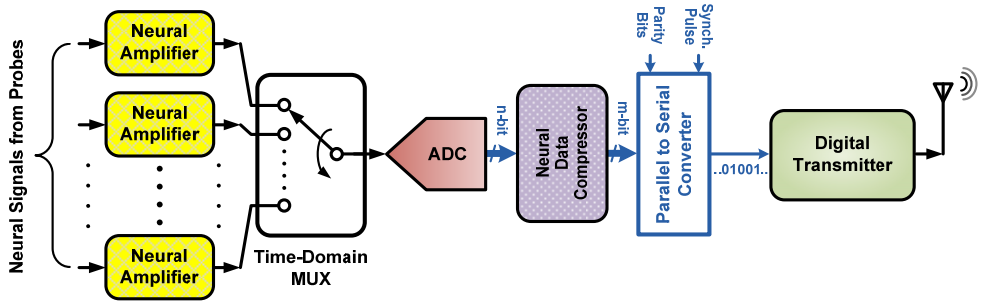

Figure 11. Monitor mode, digital transmission, mathematical approach data reduction architecture

2.2.5. Scan mode, digital transmission, spike reporting data reduction

When the number of neural recording channels exceeds (greater than 16 channels), monitor mode of recording is not very practical. Instead of monitoring of neural signals, the system can easily detect the neural spikes on every channel using per-channel spike detectors and then reports the existence of a spike on a channel. The spike detection can be accomplished using one of the three methods: hard thresholding, detection based on spike's features, or detection based on nonlinear energy operator. Such architecture is shown in Figure 12. In

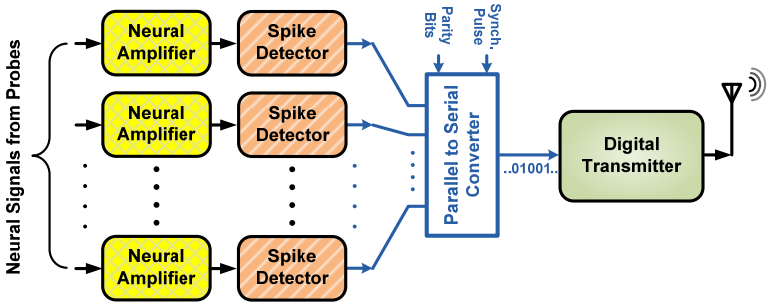

Figure 12. Monitor mode, digital transmission, spike reporting data reduction architecture

this architecture after signal preconditioning and spike detection, all the parallel data is converted to a bit stream along with parity bits and synchronization pulses and is then delivered to the digital transmitter. A sample of this architecture for a 100-channel neural recording microsystem is presented in [31] where the spike detectors are simple comparators with adjustable threshold level.

3. Visual prostheses

Human vision is known to be one of the highly sophisticated sensory systems could be found in the nature. When looking into someone's eyes, several parts of visual system can be easily seen. A black-looking aperture, **the pupil,** that allows light to enter the eye. A colored circular muscle**, the iris,** which controls the size of the pupil so that more or less light is allowed to enter the eye. A transparent external surface**, the cornea,** that covers both the pupil and the iris. The cornea is the first and most powerful lens of the optical system of the eye and allows, together with **the crystalline lens** the production of a sharp image at the back of the eye. The back of the eye is lined with a layer called the retina. The retina is a membrane containing photoreceptor nerve cells. The image information from over 100 million photoreceptor cells is pre-processed in subsequent layers of retinal cells, and then transported to the next parts of the visual system by the optic nerve comprising around 1.2 million fibers [32]. Failure in the operation of any part of the visual system, illustrated in Fig. 13, can potentially cause blindness. Aside from approached such as cell regrowth using stem cells and semiconductor photodetector arrays, implantable visual prostheses have exhibited successful performance through electrical stimulation [33]. The goal of artificial vision systems, also known as visual prostheses, is to artificially produce a visual perception in individuals with profound loss of vision. The visual prosthesis technology relies on patients having a developed visual cortex and they need have been able to see in the past for this device to be of benefit to them.

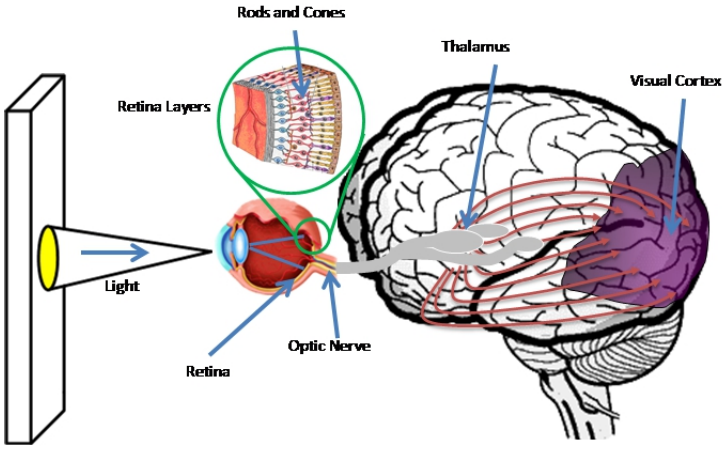

Figure 13. Human Visual Pathway

According to the World Health Organization (WHO), population of the blind is estimated 38 million in 1990 worldwide, extrapolated 45 million in 1996 and projected to be 76 million in 2020. The important fact is that almost 80% of the blind suffer needlessly and their blindness could be prevented or treated [34]. The most common causes of adult visual impairment include Age-related Macular Degeneration (AMD), Retinitis Pigmentosa (RP), and diabetic retinopathy, all occurring in the retina. AMD is caused by a combination of genetics and environmental and other individual factors, and is characterized by progressive loss of central vision. RP affects the rod cells first and then the cone cells. Rod and cone cells are used in night vision and ambient daylight levels, respectively. Early symptoms of this retinal degeneration include night blindness and increasing loss of peripheral vision leading to complete blindness [35]. Existing treatments can perhaps slow the progress of these diseases, and no cure is available. However, recent use of molecular genetic strategies has provided some restoration of vision in dogs and humans with RP [36].

In the following sub-sections, general block diagram of a visual prosthesis will be presented. Main building blocks of a typical visual prosthesis system will then be introduced and some of the associated design aspects and challenges in both circuit and system levels will be studied. Furthermore, latest achievements in the visual prosthesis being developed at the Research Laboratory for Integrated Circuits and Systems (ICAS), K.N. Toosi University of Technology, Tehran, Iran, will be reviewed.

3.1. General design

Depending on the part of the visual system that fails to function, a visual prosthesis is designed to bypass the failing parts and deliver the image information to the rest of the natural visual system that works perfectly. Hence, several approaches are taken to restore vision to the blind, which can be categorized into: retinal (including epi-retinal and sub-retinal) approaches, optic nerve stimulation, and cortical approaches.

In epi-retinal prostheses, the prosthetic device is attached to the inner retinal surface. The sub-retinal approach involves implanting an electrode array between the bipolar and retinal pigment epithelium. In this case, the rest of the system can be placed out of the eyeball. In both epi-retinal and sub-retinal methods, healthy retinal neurons are electrically stimulated, which bypass the damaged photoreceptors thereby creating visual excitation [37,38].

The optic nerve, which is about 1–2 mm in diameter, serves as a compact conduit for all the information in the visual scene. This means that electrical stimulation of a small area of the optic nerve would be expected to activate a large segment of the visual field. To stimulate the optic nerve, a cuff electrode encircles the optic nerve. Since the electrodes are on the outside of a very densely packed nerve (1.2 million fibers within the nerve), focal stimulation and detailed perception are difficult to achieve [39].

Without taking so many technological, surgical, and cognitive challenges into consideration, stimulation of the visual cortex seems to be capable of restoring vision for the blinds of different types, including those suffering from damages to both retina and optic nerve.

However, for those who are eligible to use retinal prostheses or optic nerve stimulation, stimulation of the visual cortex might not be the first preference. The surgical risk to a patient with an otherwise healthy brain may be higher for visual cortex prostheses. Also, bypassing the visual pathway demands more complicated signal processing by the prosthesis to make up for the non-negligible part of the natural image processing that is missed [40].

Figure 14 shows a generalized architecture for the visual prostheses of different kinds being developed by several groups around the globe [37-41]. Despite so many differences between how these systems are implemented, they are all common in the fact that they capture images from the external world and after some processing, deliver the processed image information to the healthy part of the visual system that is still functional. Successful stimulation of the visual system can lead to the perception of spots of light, referred to as *phosphenes*, in the visual field of the patient [42]. Although unlikely to recreate perfect vision, artificial vision systems may evoke enough phosphene perception to perform every-day tasks such as navigation, recognition, and reading.

According to the simplified block diagram shown in Fig. 14, a visual prosthesis system, in general, comprises several blocks: A video camera, which can be worn on eyeglasses, captures images from the vision field of the patient in the external world. After some external video preprocessing, performed to extract the main useful information from the recorded images and hence to reduce the amount of data, the resulting image information is prepared for wireless transmission. Processed image information along with some stimulation specifications are then transmitted to an implantable module. After the retrieval of the received data, an embedded processor sends digital information to a stimulation back-end, which is in charge of generating analog electrical pulses. Usually, a flexible cable conveys these electrical outputs to an electrode array that interfaces to the target tissue.

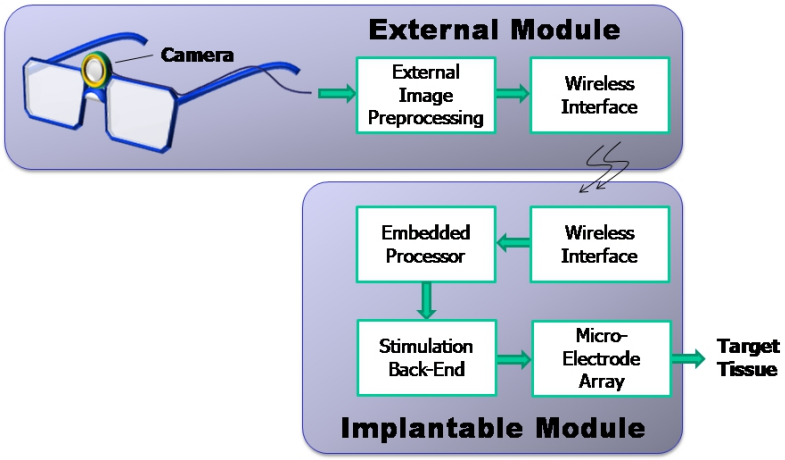

Figure 14. General architecture for a visual prosthesis system

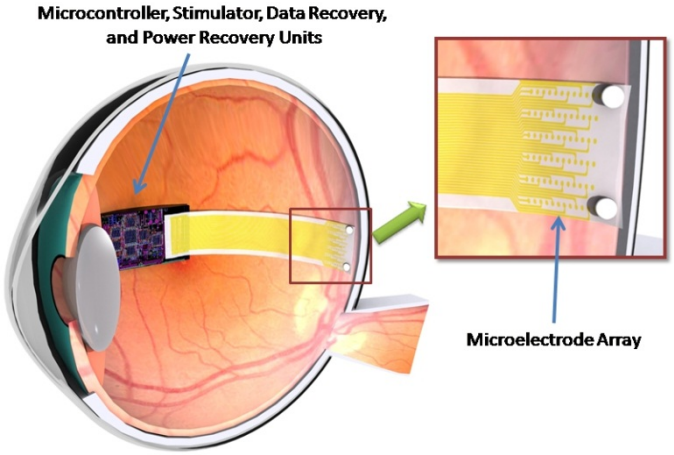

Figure 15. Illustration of the ICAS epi-retinal implant

The external unit is usually powered using batteries, while the implanted electronics receive power wirelessly. In an ideal case, all the electronic circuit blocks are integrated on the same platform. Figure 15 shows an illustration of the visual prosthesis being developed at the ICAS laboratory, in which all the implantable electronics are integrated on a micromachined silicon platform. This platform needs to be packaged and sealed in order to prevent any interaction between the electronic parts and the neighboring living tissues and biological fluids. Moreover, non-electronic parts, such as the coils used for inductive power and data telemetry, the microelectrode array (MEA), and the cable connecting the MEA to the electronics package need to be either made from biocompatible materials or at least encapsulated with biocompatible films.

To develop a fully functional visual prosthesis, in addition to the development of the electronics hardware required for this purpose, engineers need to collaborate with specialists in clinical and surgical issues to form a multidisciplinary team. In addition to making decisions on main issues such as surgical and implantation procedures, the medical research team also works on the selection of appropriate types of lab animals, assess and monitor issues related to the health and normal behavior of the subjects pre- and post-implantation, and on the design and development of clinical tests to assess the efficacy of the operation of the implant. In summary, to develop a visual prosthesis system for chronic operation, close collaboration between specialists in both engineering and medical disciplines is inevitable.

3.2. External video processing unit

Considering the fact that the implantable module is preferred to be realized with small physical size and operate with low power dissipation, any attempt to reduce the complexity and power consumption is welcomed in the design and implementation of the implant. For this reason, complex image processing tasks are usually performed right after capturing

video information on the wearable external module where physical size and supplying electric power are not big concerns.

For video capture, different image-acquisition devices are used in visual prosthesis systems such as charge-coupled devices (CCDs) and complementary metal-oxide semiconductor (CMOS) cameras. Figure 16 shows two CMOS camera modules used as the external video capture device by the ICAS visual prosthesis team [43, 44]. The first generation (Gen.-1) video capture setup, shown in Fig. 16.a, was implemented on the CMUCAM3 module comprising the OV6660 CMOS image sensor. Input and output image sizes are 128 × 128 and 32 × 32 pixels, respectively, and output frame rate is 8.3 images per second. For the second generation (Gen.-2) external video capture device, the MINI2440 board with the OV9660 image sensor was used (Fig. 16.b). For this version, input image size is 256 × 256 pixels, output image size is 32 × 32, and output frame rate is 15 images per second. These are wearable hardware that can be used in dynamic tests to evaluate image processing algorithms used in research prototypes and also in real visual prostheses.

To efficiently utilize the limited bandwidth available for the wireless transfer of the captured images on one hand, and to simplify the tasks the embedded controller is expected to do, some image processing is performed on the external module. Edge detection and image quality enhancement, zoom, contrast and brightness adjustment are considered to be realized on the external side [45-47]. Taking into account limitations in the fabrication of MEAs, two image processing modules were developed in the ICAS visual prosthesis project, each comprising three major tasks: image reduction, extraction of basic features, and result remedy.

In order to assess and evaluate the efficacy of the image processing methods used, a bank of a variety of images, frequently seen in everyday life, was prepared. This includes in-door and out-door images, real pictures taken from the external world and synthesized images such as handwritings and signatures. For the Gen.-1 external module, images were reduced in resolution and color information and processed based on image histogram classification [43]. The proposed algorithm and other well-known approaches such as Canny's method [48], importance map [49] and hard-thresholding [50] were applied to exemplars of the

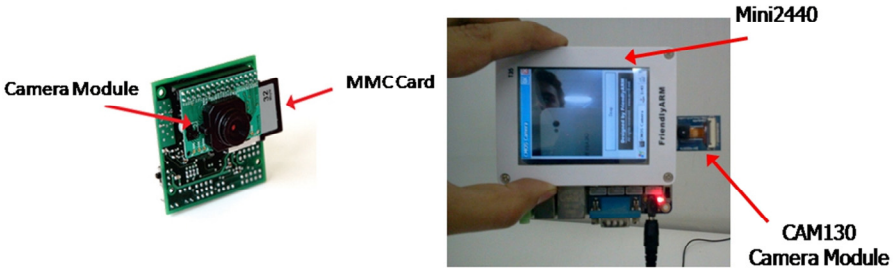

Figure 16. Hardware used by ICAS visual prosthesis team (a) First generation, (b) Second generation

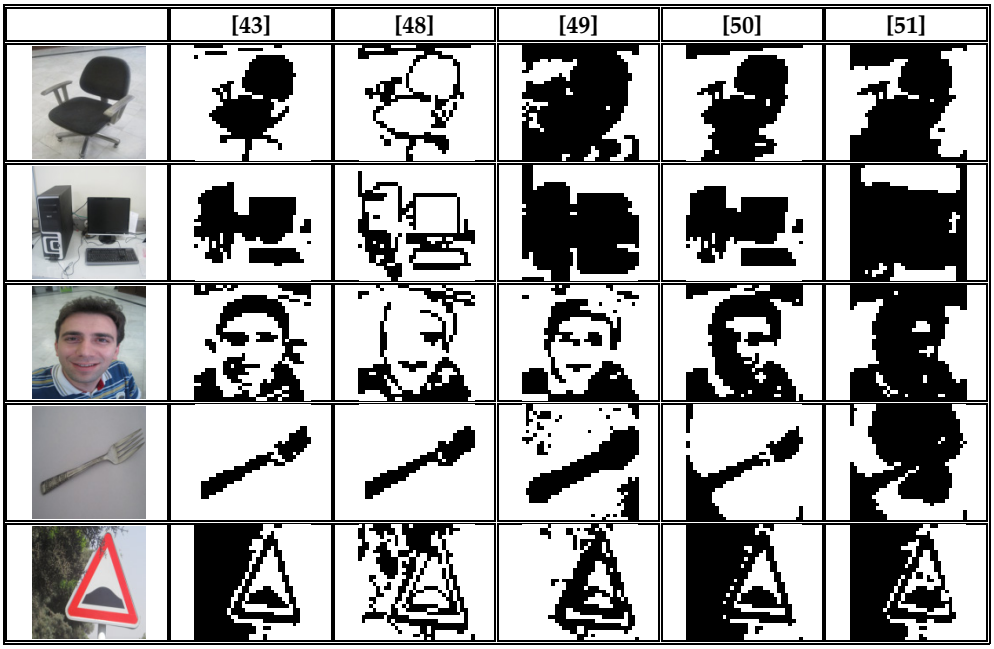

Figure 17. Comparison between the first image processing algorithm proposed by ICAS visual prosthesis team and the output of some well-known approaches [43]

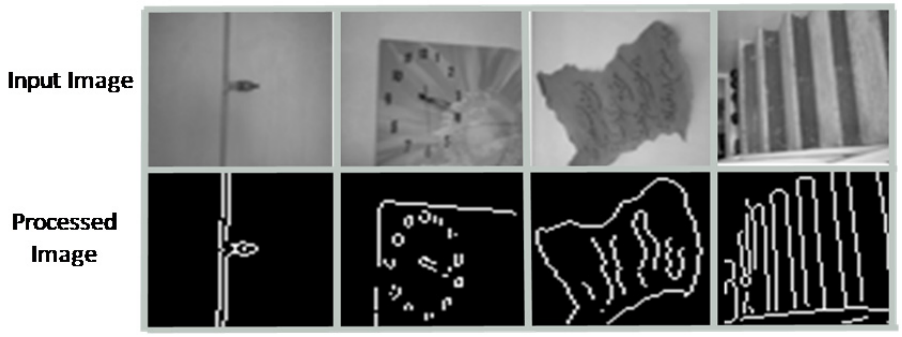

Figure 18. Output results of the developed hardware for the second generation of external module of ICAS visual prosthesis team [44]

picture classes in the bank (Fig. 17). The results were then evaluated using questionnaires filled out by a group of randomly selected people.

The algorithm used for external image preprocessing in the Gen.-2 setup was based on the Discrete Cosine Transform (DCT) [52] and Gabor filter [53]. The DCT determines image frequency and sets the frequency for the Gabor filter. Gabor edge detector is like the natural edge detection that is performed in the human visual system. This algorithm was implemented on the MINI2440 board. Output image dimensions were 32 × 32. Figure 18

shows the output results obtained from the developed hardware for the second generation of ICAS visual prosthesis team.

3.3. Implant modules

3.3.1 Embedded control unit

Similar to almost any other implantable microstimulating systems, a visual prosthesis sends the incoming data from external module to a stimulation back-end to be delivered to the target tissue by a centralized controller embedded in the system. The controller is in charge of both administering the implant operation and generating stimulation commands/data to be converted to analog stimulation pulses in the stimulation back-end. As these controllers are designed to be implanted in the body, they need to be realized with small physical dimensions, have a limited power budget mainly to comply with living tissue safety standards and limited amount of power transferred to the implant part, and can utilize a limited bandwidth for data telemetry according to frequency allocation regulations. This is why all of the research groups including ICAS visual prosthesis team involved in the design of visual prostheses prefer to design their own special-purpose controller [54-56] rather than an off-the-shelf commercially-available general-purpose controller.

From a functional point of view, the entire visual prosthesis system needs to provide high enough image resolution for acceptable visual perception for the patient. The system also needs to operate fast enough to stimulate the visual system with acceptable stimulation rate for a real-time flicker-free video stream. There are other concerns, however, in the system level that contribute in how the system will be integrated. For instance, it is important to have low number of interconnects between the controller and the stimulation back-end, especially when the system is designed with a high-resolution electrode array. This means that the controller needs to interface with the stimulation back-end in a serial fashion rather than in parallel form.

As an example of a special-purpose microcontroller dedicated to visual prosthesis, the following paragraphs reports on the design of ICAS embedded controller. This controller receives three types of data packets carrying a mode packet and the associated data, and is capable of generating a variety of stimulation signals according to the definition of the received data. Figure 19 shows the block diagram of the ICAS controller designed with a hardwired architecture for small silicon area and power consumption, and fast operation [56]. The data exchange block receives the incoming information in the form of serial data packets along with a synchronized clock signal from the wireless interface block. This block checks the format and contents of the data packets and returns an error message to the extra-ocular module as required. The received data packets may convey either configuration or image information. Configuration parameters are stored in the config. register bank. The image memory is considered to temporarily store the pixelized image information. Corresponding stimulation details for each pixel of the image are then generated in the stimulation generation engine. Stimulation details in the form of packaged commands and data (stimulation packets) are finally framed in the outgoing packet generator in order to be sent to the stimulation back-end.

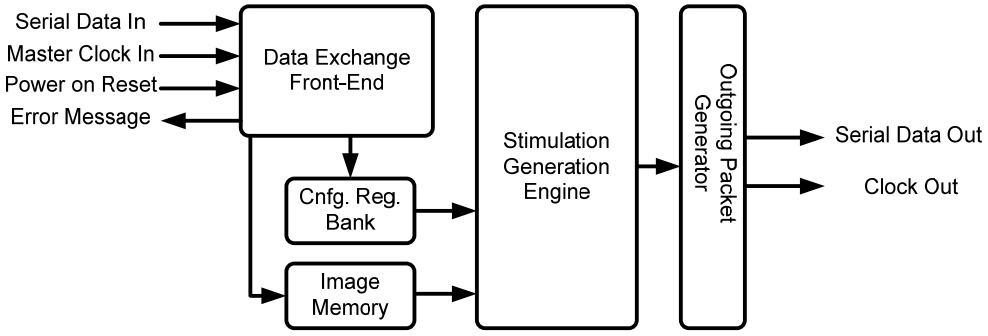

Figure 19. Block diagram of the controller designed by ICAS visual prosthesis team

The controller designed by ICAS visual prosthesis team supports the generation of biphasic stimulation pulses (refer to section 3.3.2) in the form of both single pulses and pulse trains. Stimulation packets, sent from the controller to the stimulation back-end, define stimulation pulse amplitudes and timings. This includes amplitudes and pulse widths for both anodic and cathodic phases, an inter-phase delay, and an inter-pulse delay for the pulse train stimulation. The controller returns a data packet containing an error message to the external setup in the case of detecting error in the incoming data packets. The pixelized image sent to the controller are in the form of black and white, number of pixels are 16×16 and input frame rate is 15 frames per second.

The designed controller can be programmed to operate in one of the following three possible operating modes:

- Setup mode, in which the parameters required for the main operation of the system (e.g., stimulation pulse profile) are transferred from the external setup to the controller.
- Image mode, considered for receiving information associated with the image captured externally.
- Site discharge mode, envisioned for connecting the electrodes to the ground. This is to discharge the tissue being stimulated every once in a while in order to prevent tissue damage caused by charge accumulation.

For the controller to operate in either one of the three operating modes introduced above, a set of 10-bit packets is sent from the external setup to the controller. Each 'packet set' starts with a 'START' packet, which is a predefined combination of 0's and 1's (1010101010). A 'MODE' packet (MP) then follows to indicate in what operating mode the controller is to be put. Depending on the type of the packet set received, the next packets are accordingly determined, as shown in Figure 20. A packet set is finally terminated with an 'END' packet. In the case of detecting errors in the incoming packets, the controller generates an error message and sends it to the external setup. To comply with the interconnect challenge, pointed out in the previous section, data communication between the controller and both the external setup and the stimulation back-end is performed in a serial fashion.

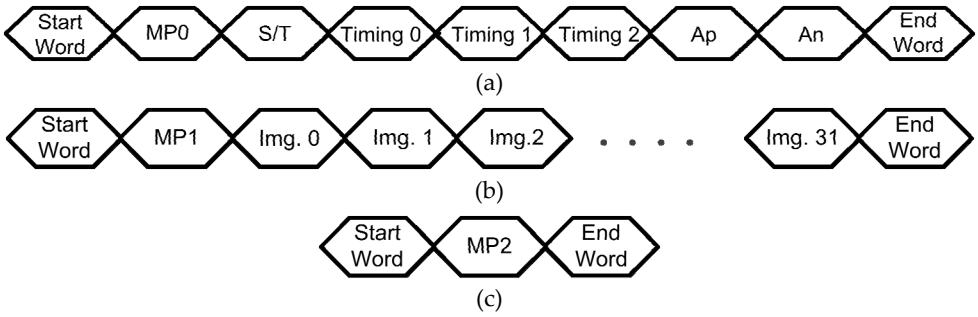

Figure 20. Format of the data packets (a) Configuration data packets, (b) Image data packets, and (c) Discharge data packets

Parameters	Specifications/Values	Parameters	Specifications/Values
Master clock freq.	1 MHz	No. of pulse repetition (pulse train)	31 times per stimulation
No. of pins	5 input pins, 3 output pins	Pulse repetition freq.	0.14 - 9.8 KHz
Incoming bit rate	10.5 Kbps @ 30 fps	Stim. phases width	Anodic 34 – 2018 μs Cathodic 34 - 2018 μs Interphase delay 0 - 994 μs
Outgoing bit rate	65.2 × n* Kbps @ 30 fps	Stim. Phases resolution	34 μs
No. of stim channels	16 × 16	Anodic and Cathodic amplitude resolution	8 bit

*n = number of pulse repetition in train strategy

Table 2. Designed Controller Specifications

To verify the functionality of the controller, it was implemented on XC2S200. The controller was tested in different operating conditions, including Setup, Image, and Site discharge modes. Serial incoming packet sets were sent to the controller to either program or operate the controller. Functional specifications of the controller are summarized in Table 2. It is worth noting that, at a master clock frequency of 1MHz, the controller is fast enough to support stimulation rate of as high as 30 fps for 256 stimulation sites with a time resolution of 34 μs for biphasic stimulation pulse generation.

3.3.2. Stimulation circuitry

Stimulation circuitry also known as microstimulator is another implant module in visual prosthesis and is in charge of generating and delivering electrical stimulation pulses to the target tissue. Figure 21 shows a generic block level diagram of the components of a

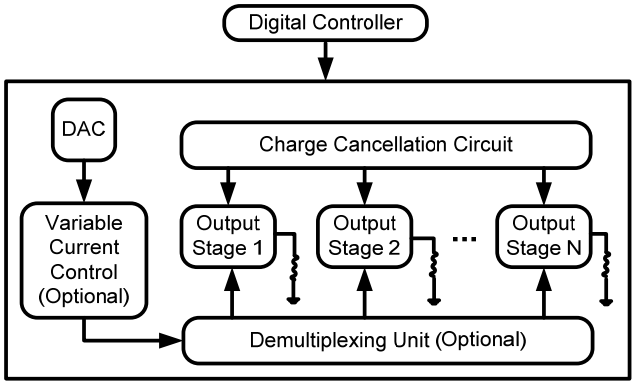

Figure 21. A generic block diagram of a microstimulator

microstimulator. The serial data which is wirelessly received and recovered by the data telemetry system, and the clock required for synchronization serve as inputs for the system. A digital controller controls the various blocks of the microstimulator to avoid any conflicts such as discharging while stimulating.

The amplitude of the current generators is controlled by an array of digital-to-analog converters (DAC) allowing digital control of the amplitude of current pulses. The pulse width of each stimulus is controlled by the stimulation sequencer according to the data received. Other parameters such as interphase interval, and stimulation period are also controlled by this block. Along with providing stimulation parameters for an individual stimulus generator, the stimulation sequencer also controls the order of stimulation between different electrodes.

The outputs of the stimulus generators can be designed to pass through a demultiplexer which connects to the electrode array. In this case, the demultiplexer allows one output of the stimulus generator to serve more than one electrode by connecting the output to one of the many electrodes which form a demultiplexed group. This method allows only one electrode in demultiplexed group to stimulate the tissue and thus reduce the flexibility of any-time-any-electrode stimulation but reduces the number of current generators. The stimulus gain controller which is also optional in designing a microstimulator adjusts the gain of the stimulus generator thereby adjusting the full scale (maximum) current generated for each demultiplexed group [57].

Electrical stimulation of excitable cells is generally performed in three forms: 1) voltage-controlled stimulation (VCS), 2) current-controlled stimulation (ICS), and 3) charge-controlled stimulation (QCS), in which voltage, current and electrical charge controlled by switched-capacitor array is applied to the target tissue, respectively. A main drawback of VCS approach is that the current passing through the tissue is highly dependent on the electrode or tissue impedance. Therefore, the charge delivered to the tissue is not well controlled. The VCS form is suitable for power-efficient circuits. The disadvantage of QCS method is large chip-area occupied due to many used capacitors. In ICS form of electrical

stimulation, the desired stimulus current passes through the tissue regardless of the tissue impedance. Using this approach with a high-output-impedance output stage for a microstimulator results in better control over the stimulus current and also safer stimulation [58, 59].

There are two general stimulus current waveforms used in neural stimulation: 1) monophasic pulse and 2) biphasic pulse. Monophasic stimulation causes charge accumulation at the electrode-tissue interface and leads to tissue damages. In charge balanced biphasic stimulation, each pulse is followed by a pulse of reverse polarity and results in no residual charge on the electrode and prevents tissue damages. Thus, it is safer and is preferred to monophasic stimulation. Biphasic stimulation is widely used in the neural stimulators and is shown in Fig. 22(a) in the case of rectangular stimulation waveform. The interphase delay T_d separates the opposite phases and thus, they don't reverse the physiological effects of each other. While the circuit is designed to produce charge balanced biphasic pulses, systematic mismatches in circuit design which cannot be avoided, and mismatch between anodic and cathodic current pulses due to manufacturing deviations, would most certainly be present and cause a small but finite charge storage at stimulation sites. Also other unintended sources such as leakage from an adjacent stimulation sites over a period of time may result in buildup of electric charge. The charge cancellation circuitry is activated periodically to perform this discharging process by connecting the electrodes to the common ground potential.

Historically the rectangular waveform has been the choice for the current or voltage pulses employed in neural stimulators [33-40, 57]. But, stimulation efficiency is an important consideration in the stimulation parameters of implantable neural stimulators. There exist some nonrectangular pulse shapes which can results more charge per unit transformed from surface area of the electrode to the target tissue. Some waveform shapes including rectangular, rising exponential, decaying exponential, and rising ramp are shown in Fig. 22(b). Some studies exist in the literature, analyzing the effects of waveform shape and duration on the charge, power, and energy efficiency of neural stimulation [60, 61]. As it proved by the researchers, no waveform was simultaneously energy-, charge-, and power-optimal, and differences in efficiency among waveform shapes varied with pulse width [61].

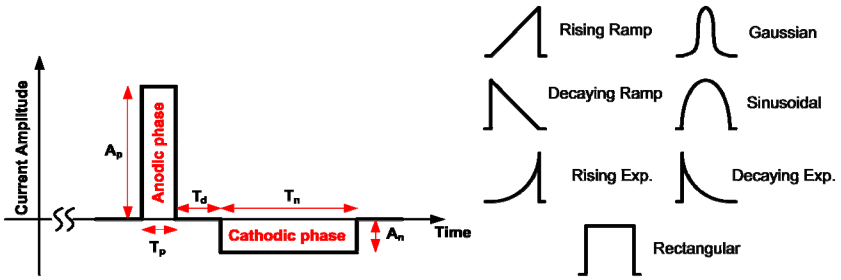

Figure 22. (a) Diagram of biphasic current pulse, (b) Different types of stimulating pulses

So, an important factor in designing a microstimulator is related to the application and signal pulse widths. Some researchers have developed appropriate circuits to generate nonrectangular waveforms according to their applications [62].

3.3.3. Microelectrode arrays (MEAs)

The advent of MEAs more than twenty years ago led to a steady advancement in the development of neural interfaces and neuroscience research. Today advanced microsystems are available for implantation into different organs of body that have multiple electrode sites and are chronically implantable [24, 31]. The packaged electronic circuits containing current drivers in implanted microsystem are connected with enough vias to recording/stimulating MEAs. Typically, a ribbon cable is used with conducting lines for an interconnect from package to electrodes and the flexible cable and MEA are formed in a single process.

The electrode sites are typically made of a conducting metal deposited on a silicon-based substrate. MEAs are usually insulated by a passivation layer, leaving the electrode sites and bonding pads exposed to the target tissue and remaining electronics, respectively [63]. Silicon microelectrodes show good biocompatibility and have the advantage of being compatible with CMOS-based on-chip signal conditioning circuitry [64]. The main problem in silicon-based microelectrodes is that the silicon substrate is mechanically rigid and brittle; therefore if the electrode moves spontaneously, it may cause severe damage in tissue. Therefore, for accommodation for movement, a flexible electrode is highly operational in implantable MEAs.

The main approach for flexible electrodes is polyimide based electrode which has drawn widespread attention [65]. In 1992, Boppart presented a first flexible electrode and used it to measure evoked potentials in brain slices [66]. The research in this field then followed in more advanced designs by Humayun and Weiland's visual prosthesis team in dual-metal-layer processes [67, 68]. Recently, another approach for flexible implantable electrode has been presented using ITO/PET (Indium Tin Oxide/PolyEthylene Terephthalate) by ICAS visual prosthesis group [69]. Among the flexible electrodes, ITO/PET electrode combines good biocompatibility, proper mechanical characteristics, high dielectric strength and is appropriate for microfabrication. The transparency of ITO/PET sheets is in the range of 75 – 80% and they have a measured sheet resistance of about 45 Ω/square. The electrodes can recover to their original shape after rolling or folding as shown in Fig. 23(a). A retinal implantable stimulation electrode has been fabricated with ITO on PET substrate in [69]. Although ITO is very biocompatible, it has relatively high impedance in contrast with other conductors like gold, therefore a layer of gold was evaporated on electrode sites for reducing electrode tissue interface impedance [69]. To passivate the electrode array and ensuring biocompatibility, the electrodes were coated by an insulating polymer, SU-8. This polymer was chosen in this work because of its excellent lithographic properties and also being biocompatible and flexible.

ICAS retinal prosthesis stimulation electrodes, microfabricated on the ITO substrate, consist of 72 (12 × 6) stimulation sites with 100 μm diameter both with circular and rectangular

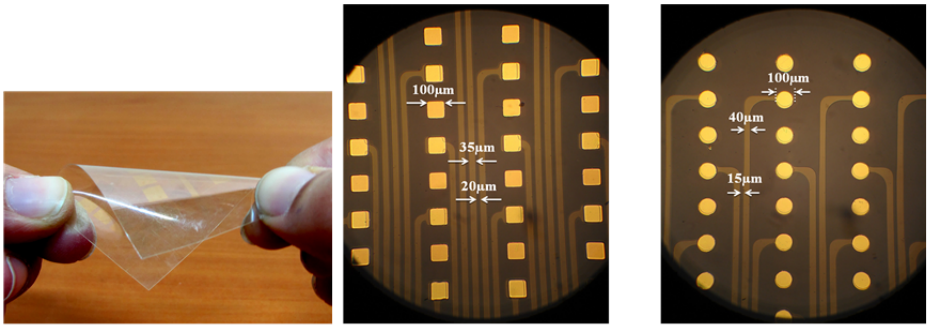

Figure 23. (a) The electrode can be folded and rolled and still maintains the original shape, (b) Stimulation sites of visual prosthesis electrode array taken by electron microscope

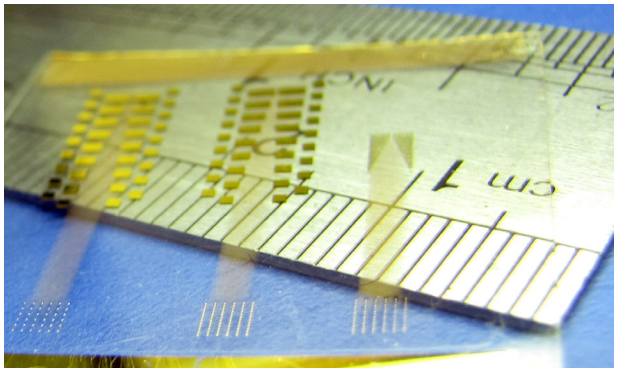

Figure 24. Fabricated biomimetic electrodes array contains of 72 sites with 100-μm diameter. The stimulation sites and bonding pads have been coated with gold. (2.47 mm × 2.8 mm)

exposing sites as shown in Fig. 23(b). The fabricated microelectrode arrays are shown in Fig. 24. Stimulation sites and bonding pads were coated with gold and other areas were covered by SU-8 polymer. The whole exposing area of the fabricated microelectrode is 2.47 mm × 2.8 mm, appropriate to be implanted in human eye.

4. Wireless telemetry

Wireless telemetry has become an inseparable part of high-performance implantable biomedical devices especially neural recording microsystems and visual prostheses. This is mainly due to the fact that use of wires increases the risk of infection, and also in most applications it is desirable to minimize the size of the implant. In order to benefit from a completely wireless system, the designed wireless interface should be capable of both receiving data from the implant, and sending power and data to the implant. Therefore, on the implant side, the wireless interface is typically consisted of a rectifier and voltage regulator (*power telemetry*), data receiver (*forward telemetry*), and data transmitter (*reverse*

telemetry). In depth discussions of wireless telemetry are presented in [70] by the authors. Hence, in this section we briefly review some of the important principles and methods in this field.

Requirements and design constrains for both power and data telemetry are dependent to the application. For example, a multi-channel neural recording system can be designed with around 10-mW power consumption, while a retinal implant may consumes more than 100 mW. Furthermore, position of the implant in body determines the maximum size of the wireless interface. In data transfer, speed of forward telemetry is of great importance in applications where large amount of stimulation data is transmitted continuously to the implant, e.g., visual prostheses and cochlear implants. On the other hand, a high-data-rate reverse telemetry is needed in neural recording microsystems and *brain machine interfaces* (BMIs) for sending recorded signals to external host with minimum delay.

Traditionally, wireless interfaces are based on inductive links, which are composed of two closely-coupled coils with a few millimeters of living tissue in between. These coils are usually tuned to the same resonant frequency to maximize the power transfer efficiency. Wire wound coils and *printed spiral coils* (PSC) are two common types of coils used in biomedical implants. Generally, there are two approaches for implementing a completely wireless microsystem. In the classical approach, only one wireless link is used for power and data telemetry, and data is modulated on the power carrier. Efficient power transfer needs high-Q coils, while for high-speed data transfer low-Q coils are mostly favored. Due to these conflicting requirements, there is a trend towards multiple carrier (multiband) links, where separate links are considered for power and data. The main advantage of this approach is that each link can be optimized individually. However, it should be mentioned that in multiband links there are notable interferences between different carrier signals, which should be reduced by using appropriate techniques such as various geometries and orientations of data coils presented in [71].

In order to optimize the power transfer efficiency and power delivered to the load, a 3-coil power link (with one additional coil on the implant side) has been proposed in [72]. The main idea behind this method is transforming the load impedance to the optimal impedance needed at the primary coil [72]. In forward data telemetry, by designing the link specifically for *binary phase-shift keying* (BPSK) modulation [73], and selecting one of the BPSK demodulators reported in [74-77], data rates as high as the carrier frequency can be achieved. For reverse telemetry, *pulse harmonic modulation* (PHM) [78], or low-power *ultra wide band* (UWB) transmitters [79] can be used to provide data rates in the range of a few Mbps.

Recently, employing capacitive links for implantable biomedical applications was studied in [80, 81]. The idea of capacitive coupling has been already used for inter-chip data communication [82] and power transfer [83], and also for sensing biomedical signals [84, 85]. In this approach a capacitor is formed between two parallel plates, one implanted and the other one attached to the outer part of the skin. The dielectric of this capacitor is mostly the body tissue between the plates. A detailed model of this type of capacitance and the

complete capacitive link can be found in [81]. One of the most important advantages of the capacitive coupling over its inductive counterparts is the high-pass nature of the link. As a result, high voltage transfer ratios can be achieved even when the transmitted signal contains wide range of harmonics, like digital data and BPSK signals [81].

Besides size constrains, number/type of wireless links, power transfer efficiencies, and high data rates, one of the most important issues in wireless telemetry is power dissipation in human body. These power dissipations may result in excessive temperature rise in biological tissues, which can even lead to tissue damages. Therefore, in designing all wireless interfaces, the amount of absorbed *radio frequency* (RF) energy has to be evaluated and compared with the human safety levels, which are usually expressed in terms of *specific absorption rate* (SAR) in the standard [86]. Nowadays, SAR calculations can be performed by most of electromagnetic simulators (e.g., SEMCAD X by SPEAG and CST Microwave Studio), and using high-resolution *three-dimensional* (3-D) human body models [87, 88].

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