
Conductance Deep-Level Transient Spectroscopic Study of 4H-SiC MESFET and Traps

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1. Introduction

Silicon carbide (SiC) is an important material for fabricating high-power, high-temperature and high frequency devices [1]. The semi-insulating (SI) form of 4H-SiC is useful for making microwave devices [2] because it helps in lowering the stray device capacitances, thereby increasing the maximum operating frequency of the device. Selective area ion implantation is regarded as an attractive doping method for fabricating MESFETs in bulk SI 4H-SiC [3–5] due to the ease of inter-device isolation without the loss of planarity.

The silicon carbide (SiC) MESFET becomes very promising candidate for high power microwave applications in commercial and military communications.

However, SiC MESFETs are not without trapping problems associated with both the surface and with the layers underlying the active channel, which influence power performance through the formation of quasistatic charge distributions. This parasitic charge acts to restrict the drain current and voltage excursions, thereby limiting the high-frequency power output [6, 7].

Over the past few years, the vanadium-doped semi-insulating SiC substrate has attracted much attention in explaining the deterioration of the SiC MESFET microwave performance. Recently, the concern has shifted more towards surface traps due to the introduction of high-purity semi-insulating substrates, which have eliminated the larger part of the problems associated with the substrate [8,9]. The presence of surface states in the ungated channel regions between drain and source terminals has modulated the depletion of the channel under the device surface, and has resulted in the frequency dispersion of the transconductance (gm) and gate lag transient [10, 12]. These anomalies make the device characteristics much more complicated, and make some troubles in circuit design.

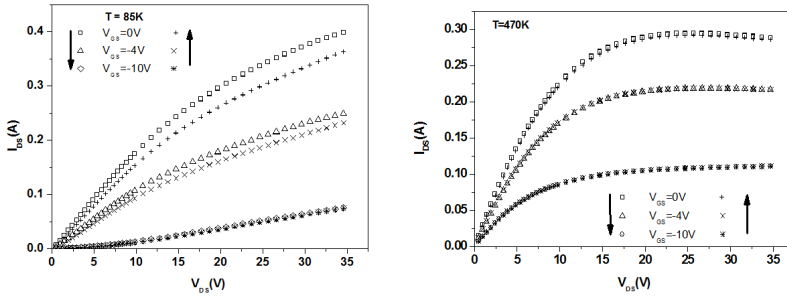


Figure 1. a: Static output characteristics (IDS-VDS-VGS) at T=85K. The gate voltage is first increased from 0 to -10 V (open symbols) and next decreased from -10V to 0V (cross symbols), b: Same as figure 1.a for T=475K. The drain current decrease is no present for the second set of curves

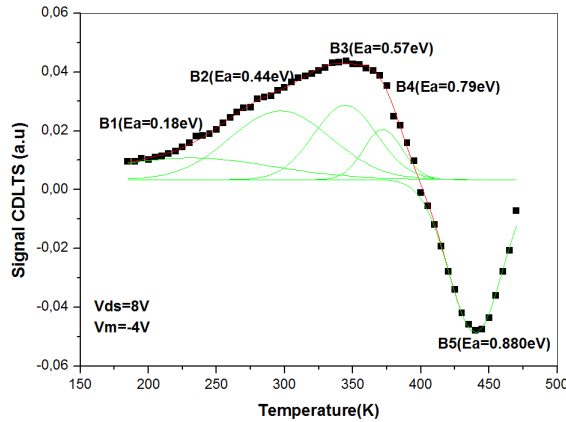


Figure 2. Conductance DLTS spectra for a 4H-SiC MESFET.

Then trapping effects due to the substrate deep levels can occur. On the other hand, it is well known that SiC / insulator interface presents high density of surface states. As an example, when using a SiO₂ passivation, a high interface state density (in the 10¹¹ to 10¹² cm⁻² range) between SiO₂ and SiC is still present. Consequently, the second hypothesis is consistent with the well known remaining passivation problem for SiC devices. Understanding the nature of the surface states in MESFETs could be a key to solve the problems. However, only a few works were reported on this topic. Conductance Deep Level Transient Spectroscopy (CDLTS), as capacitance DLTS, is an efficient tool to obtain information about traps in semiconductors, such as the activation energy, the capture cross section and the density of traps (in the case of Capacitance DLTS). The advantage of CDLTS over DLTS is the possibility to

perform the measurements on a device with a small gate area and in operating conditions. However, to the best of our knowledge, no work has been conducted using this technique for 4H-SiC MESFETs. Subsequently, in this study we have investigated the origin of parasitic effect in DC characteristics of 4H-SiC MESFETs with a gate length of 1 μ m by CDLTS.

In this study, we have used an old but not yet reported technique to investigate the origin of non stationarity in 4H-SiC MESFETs. This technique is called Current (or Conductance) Deep Level Transient Spectroscopy (CDLTS). Indeed this technique is more suitable for the study of transistors than the classical capacitance DLTS for two main reasons.

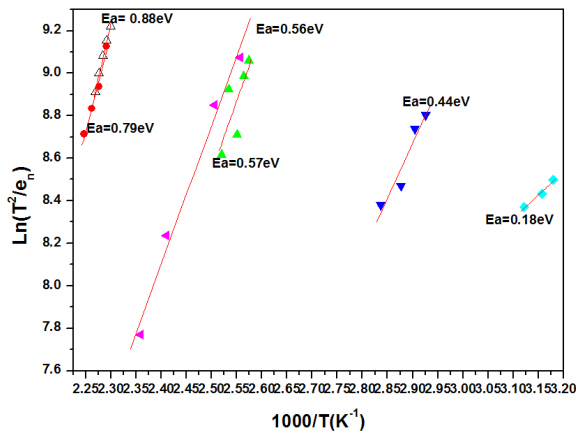


Figure 3. Arrhenius plot for the deep levels observed in the 4H-SiC MESFET.

2. Experimental procedure

The 4H-SiC MESFETs studied in this work were realized at THALES Research and Technology (TRT) in Orsay (France) using the same fabrication process for all the transistors. The epitaxial layer structures were prepared by CVD on semi-insulating substrates supplied by CREE. The layer stack consists of three layers: a P-type buffer layer with a thickness of 0.3 μ m and a doping level of 1.10^{16} cm^{-3} , an N-type active layer with 0.3-0.4 μ m thickness and doping level $N_d = 1-2.10^{17}$ cm^{-3} , and an N⁺ contact layer with a thickness and doping of 0.2 μ m and $N_d = 10^{19}$ cm^{-3} . The lift-off process for the fabrication of the device has already been described elsewhere [5]. The first step consists in reactive ion etching for the channel recess. An evaporation of Ti/Pt/Au stack is realized for the gate contact. The surface is passivated by a deposited oxide layer. The measurements presented in this work have been realized on short test transistors with a gate of 1 μ m and a gate width of 100 μ m. For all the transistors the source gate distance is 0.5 μ m and the gate drain distance is 2 μ m.

The current (or conductance) deep level transient spectroscopy (CDLTS) measurements were performed by applying both a drain to source voltage of 8 V, in the linear regime, and a drain to source voltage of 18V in the saturation region. The steady-state reverse bias and filling pulse voltages applied to the gate were -10V and 0V. The drain source current transient were recorded using a numerical multimeter (HP 34401 A). The transient were treated numerically using the Lang method as in classical capacitance DLTS. The measurements were carried out between 80K and 600K in a nitrogen cooled cryostat.

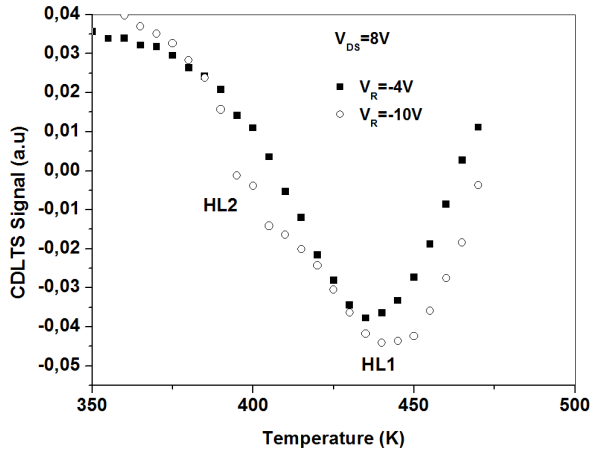


Figure 4. Conductance DLTS under gate pulse spectrum with $V_{gs} = -4V$ and $-10V$.

3. Results and discussion

3.1. Output Characteristics

Drain-source current voltage ($I_{DS}-V_{DS}$) measurements as a function of gate voltage and temperature have been performed. Output characteristics registered at different temperatures show several parasitic effects. The first anomaly observed on $I_{DS}-V_{DS}$ characteristics consist in decreasing of the current when we perform the V_{GS} sweep consecutively increasing the negative gate voltage (i.e pinching the channel) and next decreasing V_{GS} to zero (i.e opening the channel). This effect observed at 85K becomes more and more important for low gate voltages (Fig. 1a), i.e. when the current flows in the physical channel near the surface. This degradation in current vanishes progressively when the temperature is raised and totally disappears above 470K (Fig. 2b). Obviously, this behavior is due to a thermally activated effect. In a previous work [17] we observed also an effect of current collapse, but more pronounced for high gate voltage, when the current flows near the substrate. We attributed this to the presence of deep center located in the SI substrate. Basically, the explanation here can

be the same, but the trap location is different. Indeed, the degradation in current can be due to the presence of deep centers located in the vicinity of the channel surface. Trapping/detrapping phenomena on these centers change the charge density near the surface. When we apply V_{DS} for the first measurement we force these traps to be charged. In the case of electron traps, for instance, this charge is negative and a parasitic depletion at the channel surface reduces the drain current. At low temperature the emission kinetic of the traps is very slow. Consequently, when the second measurement is performed, the parasitic depletion region is still present and the current is reduced. When the temperature is increased, the traps are thermally activated and the phenomenon disappears. The same effect of gate lag has been observed recently and was undoubtedly attributed to surface trapping phenomena by an other group. Indeed, in their work, Cha et al [18] noticed that the phenomenon depends strongly on the channel surface: current lag is lower for recessed gate and buried gate geometry than for unrecessed and channel recessed ones. Another parasitic effect observed on some of our transistors consists in an important leakage current increasing with the temperature as can be seen for $V_{GS} = -10$ V in Fig. 1 a and 1b. We will focus in the following on the transistors showing these parasitic effects in output characteristics.

I-V-T measurements have been performed on the Schottky gate of defective MESFETs in the temperature range 100K-460K. On these diodes we have not observed any anomalous behavior like multi barrier height in direct characteristics. The ideality factor for all transistors ranges from 2 at 300K to 1.3 at 400K. These values show that the dominant mechanism of transport in our case is the generation recombination (G-R) mechanism. This result confirms the presence of (G-R) centers in the structure.

3.2. Part A

The current DLTS measurements were performed on the MESFET by applying a small drain to source voltage, V_{ds} of 8V while keeping the source grounded. This low V_{ds} was used to ensure that the MESFET operates within the linear region of the current-voltage characteristics.

With a gate bias of 4V in the neighbourhood of the threshold voltage, the drain current DLTS is sensitive to traps in the channel.

Figure 2 gives current DLTS spectrum under a gate pulse, showing five traps called (B1, B2, B3, B4 and B5). The apparent activation energies and capture cross-sections are deduced from the Arrhenius plot of $\ln(T^2/e_n)$ versus $1000/T$ (Figure 3) of all observed traps. The nature and localization of traps B₁ to B₄ has been discussed in a previous publication [6]. On the other hand, with a gate bias of -10V the device is biased closer to the threshold voltage, the drain-current DLTS is sensitive to traps in the channel and at the buffer-channel interface. A current DLTS spectrum under a gate pulse (V_{gs} switching from 0-4V and 0-10V) is depicted in Figure 4. The peak amplitude of the B1 (0.18eV), B2 (0.44eV) B3 (0.57eV) and B4 (0.79) traps is invariant with the change of the gate bias which improves their localisation at the channel surface [13].

The anomalous hole trap like peaks observed in current DLTS spectra of GaAs MESFET have been previously studied and have been associated with surface states present in the ungated regions between the gate and the source-drain electrode, acting as trapping sites for electrons emitted from the gate edge during the reverse bias. Such an explanation is supported by the fact that the temperature dependence of the thermal emission current from the gate edge to the ungated region observed in the DLTS measurements induces the change of the DLTS peak height of the hole-like trap when the value of t_2 was $4t_1$ at the constant value of V_p and V_m (Figure 5).

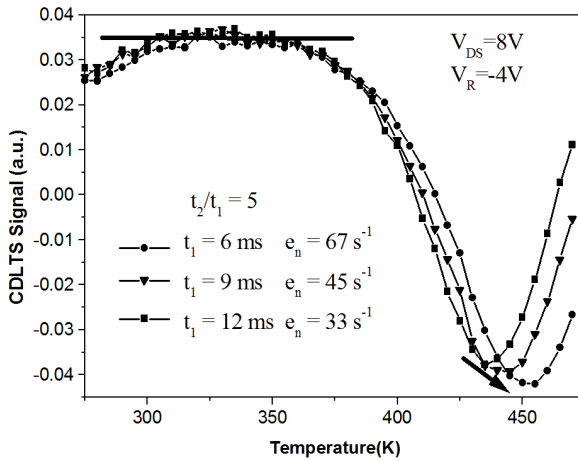


Figure 5. Conductance DLTS spectra in the linear regime ($V_{DS} = 8\text{ V}$) at $V_R = -4\text{ V}$ and for different emission rates

Thermal emission from the bulk electron traps, if present, in the active channel region below the gate would reduce the depletion width under the gate, this would in turn cause an increase in the measured source to drain current I_{ds} . However, the emission of electrons from the interface electron traps into the surface conduction channel would increase I_s . As the surface channel forms an additional conduction path between the gate and the drain (source), the interface trap emission would thus decrease I_{ds} . This is because the change in the surface current I_s and the change in the bulk channel flow in opposite directions.

The appearance of the hole-like trap signal B4 ($E_a=0.78\text{ eV}$) only for V_m lower than -10 V near the pinch-off voltage leads us to conclude that the hole-like trap is not related to the surface states at the ungated regions, but is related to channel-buffer interface.

The independence of the CDLTS signal associated to all the traps with t_p lead us to conclude the absence of all types of micropipes which can be responsible for the high power device deficiencies [13].

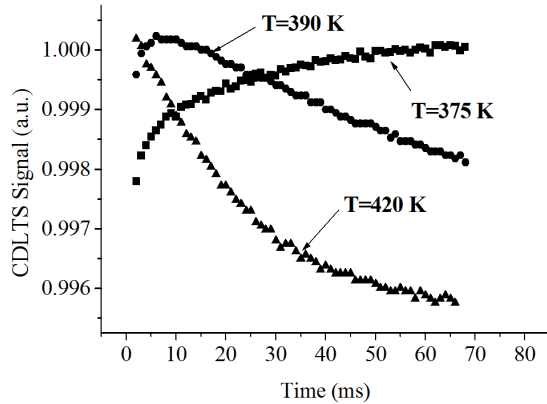


Figure 6. I_{ds} transient showing the progressive change from emission (375 K) to capture (420 K).

3.3. Part B: Surface Traps in 4H-SiC MESFET

In this part we can study the surface traps in MESFET 4H-SiC we can use CDLTS. Therefore, in our samples, we expect to observe emission from the channel (or buffer/channel interface) electron traps. In this case, the depletion width under the gate (or at the buffer/channel interface) is reduced and then an increase in I_{ds} is observed. The corresponding C-DLTS signal is positive. Nevertheless, a progressive change from emission to capture was observed in the I_{ds} transient measurement between 375 K and 420 K (Fig. 6). The corresponding C-DLTS is shown on Fig. 6. A broad positive peak due to electron emission by at four different levels is observed. The signatures of these traps have been reported in a previous work [15]. The interesting point comes from the negative peak which is clearly observed. We will focus here, on this level.

Different mechanisms can explain the presence of a negative peak:

- In capacitance DLTS they can be due to a measurement artifact when a high frequency modulation is used for the differential capacitance measurement ($R^2C^2\omega^2 \gg 1$). This obviously cannot be the case in C-DLTS measurement.
- Even if this kind of behavior is frequently called “hole like”, a hole emission process is not possible in our samples. Where do these holes could come from?
- A mid-gap amphoteric level can exchange with both bands. The activation energy of 0.9 eV for level B5 rules out this explanation.
- The last explanation is the presence of a conductive layer at the channel/passivating layer interface in the ungated regions. This conductive layer constitutes a tank for electrons which can be captured by a trap located close to the interface.

This phenomenon has been previously observed and is well-known in the case of GaAlAs/Si₃N₄ interface for GaAs MESFETs [16]. The presence of a large amount of interfacial traps (in the 10¹² cm⁻² range) at the SiC/SiO₂ interface is consistent with this explanation. These defects acting as a conductive layer at the channel surface can also explain the leakage current observed on DC characteristics (surface current flowing from the gate to the drain). To strengthen the hypothesis of a capture process on surface states, an additional C-DLTS measurement in the saturation regime (V_d=18V) has been performed. From The result displayed on Fig. 7 we clearly observe the absence of the negative peak. Indeed, in these polarization conditions the channel between the gate and the drain is almost fully deserted even for V_g = 0 V and then, it is no more modulated by the gate pulses. As the gate-drain distance is 4 times higher than the source gate one (respectively 2 μm and 0.5 μm), the response in C-DLTS measurement is almost insensitive to the channel/SiO₂ interface. This is why peak B₅ is no more observed.

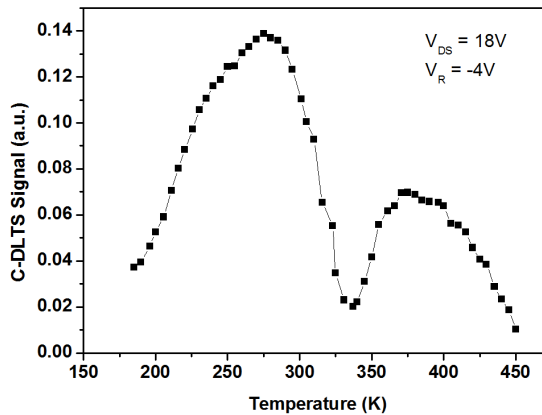


Figure 7. Current DLTS spectra in the saturation regime (V_{DS} = 15V). Only positive peaks, corresponding to electron emission are observed in this case.

4. Conclusion

In summary, deep levels in 4H-SiC MESFET were directly measured by means of the drain-current DLTS technique. Three kinds of electron traps called B1, B2, and B3 with the activation energies of 0.18eV, 0.44eV and 0.57eV respectively. These traps are located in the channel surface.

In part B we have been used Conductance DLTS for 4H-SiC MESFETs characterization and revealed capture phenomenon of electrons present at the channel/passivating layer (SiC/SiO₂) interface or at the channel/buffer or buffer/substrate interface. One kind of hole-like trap signal with activation energy of 0.90 eV is observed in conductance DLTS measure-

ments on 4H-SiC MESFETs when the device is biased in the linear regime with a gate reverse pulse in the neighbourhood of the threshold voltage. This result shows the interest of this technique for the analysis of trapping phenomena due to SiC/SiO₂ interfacial defects. The conductance DLTS using a gate pulse closer to the pinch-off voltage shows one additional hole trap HL2 with activation energies of 0.56eV located at the channel/buffer or buffer/SI substrate interface.

The understanding of trapping phenomena due to surface and interface states and the surface passivation breakout is of main interest for the future industrial development of high power RF transistors on wide band gap materials (SiC MESFETs and AlGaN/GaN HEMTs).

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References

- [1] Chow, T. P., & Ghezzi, M. (1996). *Mater. Res. Soc. Symp. Proc.*
- [2] Allen, S. T., Palmour, J.W., Tsvetkov, V.F., Macko, S.J., Carter Jr, C.H., Weitzel, C.E., Moore, K.E., Nordquist, K.J., & Pond, L.L. (1995). *3rd Annual Dev Res Conf Digest 102.*
- [3] Tucker, J.B., Papanicolaou, N., Rao, M.V., & Holland, O.W. (2002). *Diamond Relat Mater.*
- [4] Kimoto, T., Itoh, A., Inoue, N., Takemura, O., Yamamoto, T., Nakajima, T., & Matsunami, H. (1998). *Int Conf Silicon Carbide, III Nitrides and Related Materials 97, Mater Sci Forum.*
- [5] Tucker, J.B., Mitra, S., Papanicolaou, N., Siripuram, A., Rao, M.V., & Holland, O.W. (2002). *Diamond Relat Mater.*
- [6] Sghier, N., Bluet, J.M., Souifi, A., Guillot, G., Morvan, E., & Brylinski, C. (2003). *IEEE Trans. Electron Dev.*, 50-297.

- [7] Steven, C., Klein, P.B., & Kazior, E.T. (2002). *Proc. of the IEEE*, 90-1048.
- [8] Fang, Z.Q., Claflin, B., Look, B. C., Polenta, L., & Mitchel, W. C. (2005). *J. Electron. Mater.*, 34-336.
- [9] Sriram, S., Ward, A., Janke, C., Alcorn, T., et al. (2003). *Mater. Sci. Forum*, 457-460, 1205-1208.
- [10] Ho-Young, C., Thomas, C.I., Koley, G., Lester, F., Eastman, M., & Spencer, G. (2003). *IEEE Trans. Electron Dev.*, 50-1569.
- [11] Andersson, K., Sudow, M., Nilsson, P.A., & Sveinbjornsson, E. (2006). *IEEE Trans. Electron Dev. Lett.*, 27-573.
- [12] Sankha, S.M., Syed, S.I., & Robert, J.B. (2004). *Solid-State Electron*, 48-1709.
- [13] Gassoumi, M., Bluet, J. M., Dermoul, I., Maaref, H., Guillot, G., Morvan, E., Dua, C., & Brylinski, C. (2006). *Solid-State Electronics*, 50.
- [14] Gassoumi, M., et al. (2005). *Materials Science Forum Vols.*, 483-485, 865-868.
- [15] Gassoumi, M., Dermoul, I., Chekir, F., Sghaier, N., Maaref, H., Bluet, J. M., Guillot, G., Morvan, E., Noblanc, O., Dua, C., & Brylinski, C. (2004). *Proc. 24th MIEL Conference (Nis, Serbia and Montenegro, 16-19 May, 2, 417.*
- [16] Balakrishnan, V.R., Kumar, V., & Gosh, S. (1998). *Semicond. Sci. Technol.*, 13, 1094.
- [17] Sghaier, N., Bluet, J.M., Souifi, A., Guillot, G., Morvan, E., & Brylinski, C. (2003). Study of trapping phenomenon in 4H-SiC MESFETs : Dependence on substrate purity. *IEEE Trans. Electron Devices*, 50(2), 297-302.
- [18] Cha, H., Thomas, C., Koley, G., Eastman, L.F., & Spencer, M.G. (2003). Reduced trapping effect and improved electrical performance in buried-gate 4H-SiC MESFETs. *IEEE Trans. Electron Devices*, 50(7), 1569-74.