

# Character Projection Lithography for Application-Specific Integrated Circuits

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## 1. Introduction

In the recent fabrication of semiconductor devices, quite various devices are produced while most of them result in small production volumes. A small production volume of ICs leads to a rise of the price of an IC because the expensive investment made in its photomask set must be redeemed by passing on the price. The price of photomasks increases rapidly as the transistor integration advances. The price of photomasks has a great impact on the price of semiconductor devices.

Electron beam direct writing (EBDW) is a solution to fabricating small-lot ICs at a cheap cost. The EBDW can draw patterns onto silicon wafers masklessly or quasi-masklessly (Inanami, 2000; Pfeiffer, 1979). The throughput of the conventional EBDW equipment which adopts the variable shaped beam (VSB) method (Pfeiffer, 1978) is, however, extremely low. In the VSB method, exposed patterns are divided into a large number of small rectangular and triangular shapes to draw them as shown in the left of Fig. 1. In this figure Letter "E" is divided into four rectangles and consequently needs four "EB shots" to be drawn. The conventional VSB equipment *shoots* rectangular and triangular shapes onto silicon wafers and results in a lot of EB shots, which deteriorate the throughput of the equipment.

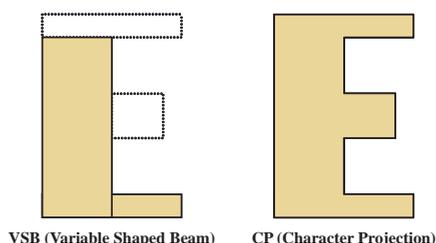


Fig. 1. VSB and CP lithographies

Character projection (CP) lithography is a promising one in which a pattern more complex than a triangle or a rectangle, called a character, is projected onto a silicon wafer with an EB shot as shown in the right of Fig. 1 (Sakitani et al., 1992; Hattori et al., 1993; Hirumi et al., 2003; Inanami et al., 2000; Inanami et al., 2003; Nakamura et al., 2006; Nakasugi et al., 2003). The e-BEAM Corporation developed a low-energy electron beam direct writing (LEEBDW) system, which was named "EBIS" (Electron Beam Integrated System) (Inanami et al., 2000;

Inanami et al., 2003; Nakamura et al., 2006; Nakasugi et al., 2003). The system can accommodate 400 characters on a CP aperture mask and any character can be chosen at every EB shot, so that the throughput of the system can be enhanced quite effectively with the CP lithography. The projection system can also project rectangular and triangular shapes with the VSB lithography. Their system is capable of projecting patterns with both the VSB and CP lithographies.

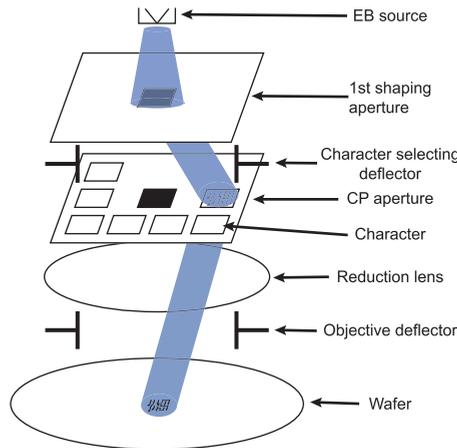


Fig. 2. Single-column-cell character projection equipment

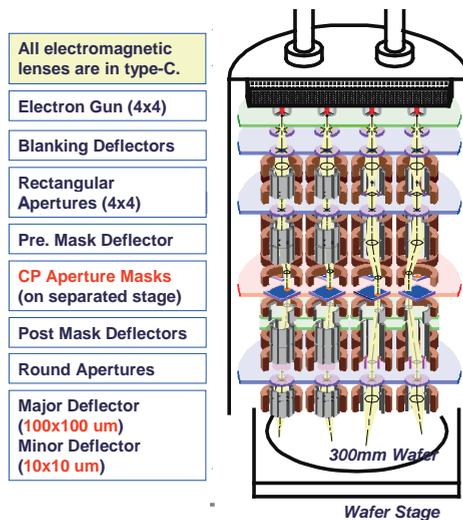


Fig. 3. An Advantest multi-column-cell character projection equipment

Yasuda et al. proposed a multi-column-cell (MCC) system, which can project multiple characters in parallel by equipping it with multiple projection mechanisms called column-cells (Yasuda et al., 2004). The motivation to develop the MCC system is to achieve higher

throughput to produce ICs than sequential projection systems by parallelizing projection operations. Several ASIC design techniques were discussed (Sugihara, 2008, 2010). This chapter focuses on design techniques for single-column-cell projection equipment.

## 2. Cell library development for character projection equipment

Standard cell methodology is a quite popular design method to design an ASIC. The standard cell methodology exploits a cell library which is a collection of low-level logic functions, called cells, such as NAND gates, NOR gates, flip-flops, latches and buffers. From a viewpoint of character projection lithography, it is important to project as many cells as possible with character projection lithography.

Cell library development methodologies were studied for character projection lithography (Sugihara et al., 2005, 2006a, 2006c, 2007b, 2008, 2010, Inanami et al., 2000). In this section, we focus on a cell library development methodology for a single-column-cell system (Sugihara et al., 2005, 2006a, 2006c, 2007b).

*Cells*, which are components for IC designs, are ordinarily utilized as the basis of characters. The characters are placed in an array on a CP aperture mask as shown in Fig. 4. It accommodates several hundred characters, which are several- $\mu\text{m}$  squares. The number of characters available on a single CP aperture mask is limited to a small one and not all cells in a cell library can be realized on it. For example, if there are four variations for every cell function as shown in Fig. 5, a CP aperture mask accommodates about 100 or less of cell functions at the 90 nm technology. Even if multiple CP aperture masks are utilized for placing all the cells on them, it takes forbiddingly long time to switch CP aperture masks for setting and adjusting. This chapter assumes that a single CP aperture mask is allowed to use for each layer and that the cells off the CP aperture mask are projected with the VSB lithography. It is quite important to select frequently-utilized cells to put on a CP aperture mask because a CP aperture mask is a precious resource to increase the throughput of the system.

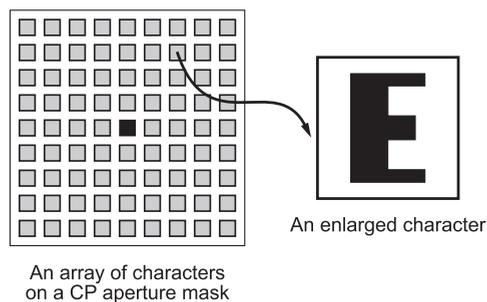


Fig. 4. A CP mask

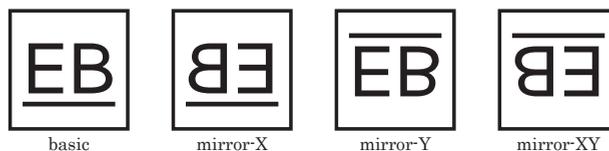


Fig. 5. Cell directions

## 2.1 Cell selection for CP aperture masks

In this section, a mathematical programming model is shown to select an optimal set of cells which are placed on a CP aperture mask so that the number of EB shots to draw an entire chip is minimized.

Before we describe the mathematical programming model, we briefly describe the ILP (Integer Linear Programming) to review. The ILP is a well-known way to minimize loss or maximize benefit in logistics, transportation, manufacturing and so forth (Williams, 1999). The goal of the ILP is to minimize (or maximize) a linear objective function on a set of integer variables, while satisfying a set of linear constraints. A typical ILP model can be described as follows:

$$\text{minimize: } \mathbf{Ax} \tag{1}$$

$$\text{subject to: } \mathbf{Bx} \leq \mathbf{C}, \text{ such that } \mathbf{x} \geq \mathbf{0}$$

where  $\mathbf{Ax}$  is an objective function to minimize,  $\mathbf{A}$  is an objective vector,  $\mathbf{B}$  is a constraint matrix,  $\mathbf{C}$  is a column vector of constants, and  $\mathbf{x}$  is a vector of integer variables. Efficient ILP solvers are now readily available (ILOG, 2003).

A mathematical formulation is shown to select an optimal set of the cells which are placed on a CP aperture mask so that the number of EB shots to draw an entire chip is minimized. We name this mathematical problem  $P_A$  ("A" stands for assignment). The problem  $P_A$  can be stated as follows:

For given  $C$  kinds of cell objects, their reference counts  $r_1, r_2, \dots, r_C$ , their EB shots by the CP method,  $S_{CP_1}, S_{CP_2}, \dots, S_{CP_C}$ , their EB shots by VSB method,  $S_{VSB_1}, S_{VSB_2}, \dots, S_{VSB_C}$ , and a CP aperture mask capable of loading  $N_{\text{char}}$  characters, determine each cell's drawing method, the CP or VSB method, such that the total EB shots to draw the entire chip are minimized.

This problem is a typical combinatorial optimization problem and can be shown to be NP-hard. However, for realistic cell libraries, the sizes of the problem instances are small. The problem instances can be solved exactly using an ILP solver within short computation time.

To model this problem, consider a chip for which  $C$  kinds of cell objects are employed. Cell  $i$  appears  $r_i$  times in the chip and is drawn with either the CP or VSB methods. If Cell  $i$  is drawn with the VSB method, let the number of EB shots to draw a cell instance of Cell  $i$  be  $S_{VSB_i}$ . Likewise, If Cell  $i$  is drawn with the CP method, let the number of EB shots to draw a cell instance of Cell  $i$  be  $S_{CP_i}$ . We introduce binary variables  $x_i$  (where  $1 \leq i \leq C$ ), which are used to determine a projection method of cells, that is the CP or VSB method. Let  $x_i$  be a binary variable defined as follows:

$$x_i = \begin{cases} 1 & \text{if cell object } i \text{ is drawn with the CP,} \\ 0 & \text{if cell object } i \text{ is drawn with the VSB.} \end{cases} \tag{2}$$

The total number of EB shots  $S_A$  is to draw the entire chip is given by

$$\begin{aligned} S_A(\mathbf{x}) &= \text{EB shots with the CP} + \text{EB shots with the VSB} \\ &= \sum_{i=1}^C S_{CP_i} r_i x_i + \sum_{i=1}^C S_{VSB_i} r_i (1 - x_i) \\ &= \sum_{i=1}^C (S_{CP_i} - S_{VSB_i}) r_i x_i + \sum_{i=1}^C S_{VSB_i} r_i. \end{aligned} \tag{3}$$

The second summation in the above equation does not include any variables so only the first summation is considered in the objective function of Eq. (1).

Depending on the size of a cell object, the number of characters to draw a cell instance of the cell object may differ from that of another. Cell  $i$  occupies  $c_i$  characters on a CP aperture mask. The area of the CP aperture makes a constraint on the number of characters. The following constraint, therefore, is introduced.

$$\sum_{i=1}^C c_i x_i \leq N_{\text{char}}, \quad (4)$$

where  $N_{\text{char}}$  is the maximum number of characters available on the CP aperture mask,  $c_i$  is the number of characters necessary to draw an instance of Cell  $i$  and is equivalent to  $S_{\text{CP}_i}$ .

From Eqs. (1), (2) and (3), a mathematical programming model for this problem can be formulated as follows.

*Objective:* Minimize  $S_A' = \sum_{i=1}^C (S_{\text{CP}_i} - S_{\text{VSB}_i}) r_i x_i$ , subject to  $\sum_{i=1}^C c_i x_i \leq N_{\text{char}}$ , i.e. every cell adopts one drawing method, the CP or VSB in conformity with the restriction of the area of the CP aperture. The total number of EB shots is given by  $S_A' + \sum_{i=1}^C S_{\text{VSB}_i} r_i$ .

The above model mainly aims to develop an optimal cell library set dedicated to a product but can be applied to developing a general cell library to various products. In order to make a cell library more general among multiple products, the reference counts of cells defined as  $r_i$  ( $1 \leq i \leq C$ ) should be set as the reference counts of cells through the total production of the multiple products. Both dedicated and general cell libraries can be easily obtained by our proposal once the reference counts of cells  $r_i$  ( $1 \leq i \leq C$ ) are given. The decision to make a cell library of a product dedicated or general is made by the following two factors.

The cost reduction by reducing the number of EB shots with a newly developed set of CP aperture masks.

The cost increase to newly develop the set of CP aperture masks dedicated to a product.

Even if CP aperture masks are made to dedicate to a product, the total cost for the CP aperture masks is much cheaper than that for the photomask costs of the other lithography. The total amount of data to draw patterns on masks is a dominant factor in the costs of the both kinds of masks. The amount of data for photomasks is linear to the number of transistors while that for CP aperture masks to the number of cell objects on them. The developing cost of CP aperture masks is, therefore, much cheaper than that of photomasks. The CP lithography with a set of CP aperture masks is still *quasi-maskless* in terms of cost.

## 2.2 The impact of cell directions on area and delay

There are basically four directions of cells as cell instances are physically placed as shown in Fig. 5. A *basic* direction is literally a basis of the other directions. *Mirror-X*, *mirror-Y* and *mirror-XY* directions are horizontally-flipped, vertically-flipped and horizontally-and-vertically-flipped ones respectively. The patterns of these directions of a cell function must be distinguished from the other as different patterns on CP aperture masks.

In this section, we examine the influence of the existence of the cell directions on both area and delay time of a chip. We used a logic-synthesizable benchmark circuit which was a Z80-compatible microprocessor. We used a cell library whose feature size was 0.35  $\mu\text{m}$ . The logic synthesis for the circuit was done with Synopsys Design Compiler (Synopsys, 2005). Place-and-route was done with Avant! Apollo (Avanti, 1998). Delay times for four cell directional variations are shown in Table 1. In the table, the four-bit vectors which follow "Conf. X" denote the existence of the four cell directions in the processes of place-and-route. The first bit of the vectors denotes the existence of the basic direction. If the direction is taken into

account, the number is 1, otherwise 0. Likewise, the second, third and fourth bits denote the existences of the mirror-X, mirror-Y and mirror-XY directions respectively.

Chip area	Delay times for four cell directional variations [ns], (basic, mirror-X, mirror-Y, mirror-XY)			
	Conf. 1 (1,1,1,1)	Conf. 2 (1,0,1,0)	Conf. 3 (1,1,0,0)	Conf. 4 (1,0,0,0)
799.5 × 792	N/A	N/A	N/A	N/A
810 × 808.5	7.09	6.97	N/A	N/A
819 × 808.5	7.37	7.43	N/A	N/A
829.5 × 825	7.52	-	N/A	N/A
840 × 825	7.16	-	N/A	N/A
849 × 841.5	7.24	-	N/A	N/A
859.5 × 858	7.11	-	N/A	N/A
870 × 858	-	-	7.15	N/A
879 × 874.5	-	-	7.23	7.15

Table 1. Delay times for four cell directional variations

A number in each column denotes the delay time with the least area “N/A” means that the given areas were infeasible to place and route the circuit with the place-and-route tool. For example, the least area and the delay time for the area were obtained as 810 × 808.5 and 7.09 ns respectively in Conf. 1. The least areas in Confs. 1, 2, 3, and 4 were 810 × 808.5, 810 × 808.5, 870 × 858, and 879 × 874.5 respectively. About 14% area increased when the mirror-Y and the mirror-XY were forbidden. Theoretically speaking, delay time decreases under a case in which one can use a larger place-and-route area. Delay time in a column of the table is expected to decrease downward but it did not. This is because the CAD tool is based on approximate algorithm. Comparing the two values of Conf. 2, 6.6% delay time increased while place-and-route area increased.

Conf. 1 is the configuration in which all the four cell directions are available and is supposed to be best with regard to area and delay time among the configurations because its design space includes design space of the other configurations. In other words, any layout based on Confs. 2, 3 or 4 can be realized by Conf. 1. The results which the CAD tool reported does not straightforwardly reflect this supposition because the layouts obtained by the CAD tool are approximate solutions, e.g. the delay time of Conf. 2 (6.97 ns) was shorter than that of Conf. 1 (7.09 ns) as the place-and-route area was 810 × 808.5!

Conf. 2 is the configuration in which the horizontal flippings are removed from Conf. 1. In other words, the mirror-X and mirror-XY directions are not taken into account in Conf. 2. There was no great difference of delay times among Confs. 1 and 2. Horizontal flipping seems not to be so effective to reduce delay time and area.

Conf. 3 is the configuration in which the vertical flippings (mirror-Y and mirror-XY) are removed from Conf. 1. Experimental results show that the vertical flipping of cells had little influence on delay time of the chip and it had some influence on the area. Comparing Conf. 3 with Conf. 1, about 14% area increased. This is because the gaps between cell areas were added by eliminating vertical flipping of cells and each cell area got to own its own power and ground lines.

Conf. 4 is the configuration in which any flipping cells are forbidden and only a basic direction of cells is available. Comparing Conf. 4 with Conf. 1, the differences of the delay

times were insignificant while those of the areas were noticeable, that is about 14% area increase. This is because of the same reasons that the area of Conf. 3 increased. Comparing Conf. 4 with Conf. 3, the differences of their best delay times were insignificant while those of their areas were about 4.2%. Horizontal flipping had some influence on the area increase as vertical flipping was completely forbidden.

There was no great difference among delay times between the four configurations. It was experimentally confirmed that cell directions were not strongly relevant to the increase of delay time. The existence of vertical flipping of cells was relevant to increase of area. This was because gaps between cell areas come to arise and each cell area got to own its own power and ground lines.

### 2.3 Case study

In this section, a case study is shown for five cases to examine the relation between the number of EB shots and how to select cell objects to place on characters. The five cases are described in Table 2. We developed the cell selection software described in Section 2.1.1 with a commercial mathematical optimization engine, ILOG CPLEX 9.0 (ILOG, 2003). Every optimization process finished within a second.

	Description
Case 1	Only a basic cell direction is available. The optimal set of cells is exactly searched out by solving an ILP problem instance.
Case 2	The basic and Mirror-Y directions are available. It is assumed that the reference count of a direction of a cell function is equal to that of the other direction of the cell function. Each direction is assigned 1/2 of available characters to. This is after the fashion of Inanami's (Inanami, 2000).
Case 3	The basic and Mirror-Y directions are available. Cell objects to be placed on a CP aperture mask are exactly searched with our cell selection method.
Case 4	The four cell directions are available. It is assumed that the reference count of a direction of a cell function is equal to that of the other directions. Each direction is assigned 1/4 of available characters to. This is also after the fashion of Inanami's (Inanami, 2000)
Case 5	The four cell directions are available. Cell objects to be placed on a CP aperture mask are exactly searched with our cell selection method.

Table 2. Cell directional variations for experiments

The specification of the CP equipment for which we assumed is shown in Table 3. Two benchmark circuits were used to examine their numbers of EB shots under the five cases. The description for the benchmark circuits is shown in Table 4. Note that the cell library is from academia and comprises fewer kinds of cells than that from industry.

The maximum width and length of rectangles for VSB	3.5 $\mu\text{m}$
The width and length of characters for CP	5 $\mu\text{m}$
The number of characters on a CP aperture mask	400

Table 3. Specification of CP/VSB equipment

	Circuit 1	Circuit 2
Feature size [ $\mu\text{m}$ ]	0.25	0.35
# cell objects in the cell library (mirroring ignored)	395	395
# mapped cell objects (mirroring ignored, one direction)	74	111
# mapped cell objects (mirroring considered, two directions)	128	191
# mapped cell objects (mirroring considered, four directions)	211	303
# cell instances	2311	3165

Table 4. Benchmark circuits

The EB shots under the five cases were sought out by solving mathematical problem instances and are shown in Table 5. In the table, the parenthesized values show the numbers of cell objects. The areas and delay times of Circuit 2 are shown in Table 6. In our experiment, areas and delay times of Circuit 1 were not examined because the benchmark circuit was not logic-synthesizable.

	Case 1	Case 2	Case 3	Case 4	Case 5
	# dirs: 1	# dirs: 2		# dirs: 4	
Circuit 1	15268 (74)	17300	16915 (128)	30925	29733 (211)
Circuit 2	51055 (111)	69760	69589 (191)	93774	91187 (303)

Table 5. EB shots and cell objects

	Case 1	Cases 2 and 3	Cases 4 and 5
Area [ $\text{mm}^2$ ]	768,685.5	654,885.0	654,885.0
Delay time [ns]	7.15	6.97	7.09

Table 6. Area and delay time of Circuit 2

According to Table 5, as the number of cell objects increases, in other words, the number of cell directions increases, the number of EB shots increases. This is because the reduction of cell directions enables more cell functions to be on a CP aperture mask and to be projected with the CP. The area of Circuit 2 under Case 1 was largest among the five cases as shown in Table 6 because only a single direction, that is a basic direction, was adopted for place-and-route. This was because the gaps between cell areas came to arise and each cell area got to own its own power and ground lines. Theoretically speaking, the design with the four cell directions should be best among the five cases with regard to area and delay time. Similarly, the design with the two cell directions should be intermediate. The experimentally obtained values of areas do not reflect this supposition. The delay time of Circuit 2 under Cases 2 and 3 was found best. This is because the CAD tool returned approximate solutions of layout and happened to result against the supposition. Note that the values shown in Table 1 and Table 6 are nothing more than the ones the CAD tool reported. If a design obtained with the two cell directions is better than a design obtained with the four cell directions, the design of two-cell direction may be adopted as a design of four-cell direction.

Comparing the number of EB shots of Circuit 1 under Case 4 with that under Case 5, 3.85% reduction of the number of EB shots was achieved. The difference in the numbers of EB shots was caused by solving the problem instances exactly or approximately. The optimal sets of cells was selected exactly under Cases 3 and 5 while sets of cells was selected

approximately under Cases 2 and 4 by assigning the equal number of characters to each directions of cells.

Comparing the number of EB shots of Circuit 1 under Case 2 with that under Case 4, 44% reduction of EB shots was achieved. Likewise, comparing the number of EB shots of Circuit 2 under Case 2 with that under Case 4, about 26% reduction of EB shots was achieved. It was experimentally found that the elimination of cell directions is quite effective to reduce EB shots. It was experimentally found that the elimination of horizontal flipping reduced the much number of EB shots effectively while it has small impact on area and delay time of chips.

## 2.4 Conclusion

In this section, we proposed an ILP-based cell library development methodology to reduce the number of EB shots. All optimization processes finished within a second. More than 3.85% reduction of EB shots was achieved only by distinguishing between the differently mirrored cells whose functions are identical.

We examined the influence of cell directions on both area and delay time of the circuit. It was experimentally confirmed that both of the horizontal and vertical flipping of cells had little influence on delay time of chips. The horizontal flipping had little influence on area while the vertical flipping had some influence on area. This examination helps which cell direction should be implemented on CP aperture masks.

The forbiddance of horizontal flipping caused little deterioration of area while 25.6% reduction of EB shots. It was found that the forbiddance of horizontal flipping was effective to reduce the number of EB shots while it deteriorated little area and delay time of chips. The forbiddance of vertical flipping caused 13.9% increase of area while it caused less than 1% increase of delay time. The forbiddance of vertical flipping should be determined with taking a tradeoff between area and EB shots into account. For many chips of the state of the art, cells are placed so "loosely" that the deterioration of area caused by forbiddance of multi directions of cells might have less impact on area. The relation between cell directions and EB shots in design of such chips should be further examined as future work.

## 3. Character size optimization for higher projection throughput

Character size optimization techniques were studied for character projection (Sugihara, 2006c, 2007b, 2010). We first presented an idea to optimize a character size for higher projection throughput (Sugihara et al., 2006c). We presented a character size optimization by enumerating all possible character sizes and generating a cell library for every given character size (Sugihara et al., 2006c). Next we presented a cell library development methodology in which a character size and a set of cells were optimized at the same time (Sugihara et al., 2007b). We also presented a character size optimization technique for multi-column-cell projection equipment. In this section, we focus on the first work (Sugihara et al., 2006c) for a simple explanation.

### 3.1 Character size optimization problem

In Section 2, the size of characters on CP masks was given and treated as a constant because of the restriction which attributes to character projection equipment. Cells used in a design were, consequently, partitioned to fit the constant size of characters by intuition. In this

section, we present a character size optimization problem  $P_S$  to minimize the number of EB shots, which affect the throughput of the CP equipment ("S" stands for size). The mathematical problem  $P_S$  can be stated as follows.

For given  $C$  kinds of cell objects, their reference counts  $r_1, r_2, \dots, r_C$ , the numbers of their EB shots by the CP method,  $S_{CP_i}(l_{char}, w_{char})$ , the numbers of their EB shots with the VSB method,  $S_{VSB_1}, S_{VSB_2}, \dots, S_{VSB_C}$ , the width and length of a CP mask,  $l_{CP}$  and  $w_{CP}$ , and the gap between neighboring characters,  $G$ , determine the length and width of characters,  $l_{char}$  and  $w_{char}$ , and each cell's drawing method  $x_i$ , that is the CP or the VSB method, such that the number of the total EB shots to draw the entire chip is minimized.

The number of EB shots of each cell with the CP method depends on both the size of characters and a pattern of a target layer. After the fashion of Equation (3), the total number of EB shots  $S_S(\mathbf{x}, l_{char}, w_{char})$  to draw the entire chip is given by

$$\begin{aligned} S_S(\mathbf{x}, l_{char}, w_{char}) &= \text{EB shots with CP} + \text{EB shots with VSB} \\ &= \sum_{i=1}^C S_{CP_i}(l_{char}, w_{char}) r_i x_i + \sum_{i=1}^C S_{VSB_i} r_i (1 - x_i) \\ &= \sum_{i=1}^C \{S_{CP_i}(l_{char}, w_{char}) - S_{VSB_i}\} r_i x_i + \sum_{i=1}^C S_{VSB_i} r_i. \end{aligned} \quad (5)$$

Depending on the size of a cell, the number of characters to draw a cell instance varies from cell to cell. The area of the CP mask makes a constraint on the number of characters. The following constraint, therefore, is introduced.

$$\sum_{i=1}^C c_i(l_{char}, w_{char}) x_i \leq N_{char}(l_{char}, w_{char}, l_{CP}, w_{CP}, G), \quad (6)$$

where  $c_i(l_{char}, w_{char})$  is the number of characters on the CP mask for Cell  $i$  and is equal to the number of its EB shots  $S_{CP_i}(l_{char}, w_{char})$  with the CP method,  $N_{char}(l_{char}, w_{char}, l_{CP}, w_{CP}, G)$  is the maximum number of characters available on the CP mask when the length and width of characters are  $l_{char}$  and  $w_{char}$  respectively, the length and width of a CP mask are  $l_{CP}$  and  $w_{CP}$  respectively, and the gap between characters is  $G$ .

Equations (5) and (6) include nonlinear terms and need to be linearized if we solve this problem as an ILP problem. We did not linearize this problem but enumerate problem instances by varying both  $l_{char}$  and  $w_{char}$ . Both  $l_{char}$  and  $w_{char}$  are discrete with a narrow range. The character size enumeration results in a small number even if all problem instances are enumerated. Problem  $P_S$  can be easily solved by enumeration of Problem  $P_A$ .

### 3.2 Case study

We developed software to optimize the character size and select an optimal projection method for every cell so that the number of EB shots to draw an entire chip is minimized. In this development, a commercial mathematical optimization engine, ILOG CPLEX 9.0 (ILOG, 2003), was utilized. We examined the numbers of EB shots for four benchmark circuits described in Table 7. All cell libraries adopted for the four circuits include more than 300 cell functions while each circuit consists of less than 100 cell functions as a result of logic synthesis. Cells which are logically identical but are differently mirrored must be distinguished from one another on CP masks. The numbers of cell objects with or without mirroring considered are shown in the table. The numbers of cell instances are also shown in the table. Note that the size of Problems  $P_A$  and  $P_S$  are not affected by the number of cell instances but by that of cell objects. The number of cell instances affects the reference counts of cells, which are constants in the ILP model. It is the number of cell objects that is equal to the number of variables in Problem  $P_A$  and affects the size of problem instances. The

experiments were based on the CP equipment which was described in Table 8. In the equipment, patterns on CP masks are demagnified to 1/5 on a wafer and all the values on the table are demagnified to 1/5 on silicon wafer. This means that a CP mask is capable of 441 characters of a 5.0  $\mu\text{m}$ -square which occupies a 25.0  $\mu\text{m}$ -square on CP masks. We assumed that the maximum size of an electron beam for the CP is a 10  $\mu\text{m}$ -square on silicon wafers with the state-of-the-art electron beam technology.

	Circuit 1	Circuit 2	Circuit 3	Circuit 4
# mapped cell objects (mirror ignored)	39	55	74	76
# mapped cell objects (mirror considered)	118	164	211	132
# cells in the library (mirror ignored)	310	310	395	395
# cell instances	3,875	3,943	2,311	35,683
Mirror-X	Yes	Yes	Yes	Yes
Mirror-Y	Yes	Yes	Yes	No
Mirror-XY	Yes	Yes	Yes	No
# variables in subproblems	118	164	211	132
Feature size [ $\mu\text{m}$ ]	0.35	0.35	0.25	0.25

Table 7. Benchmark circuits description

	Size [ $\mu\text{m}$ ]
The length and width of CP masks	650
Gap between neighboring characters	5
The maximum length of characters	50

Table 8. Description for CP equipment

We examined the numbers of EB shots to draw a polysilicon gate layer of the devices under three cases shown in Table 9. In Case 1, we assumed that characters were 5.0  $\mu\text{m}$ -squares. These values were given in Inanami's work (Inanami, 2000) and this size was based on the specification of the CP equipment. In Case 2, it was assumed that the size of electron beams was smaller than a 10  $\mu\text{m}$ -square and the character size was optimized under the character size constraint. In Case 3, we assumed that any size of an EB was available and the character size was optimized under the character size constraint.

	Length	Width	Remarks
Case 1	5.0 [ $\mu\text{m}$ ]	5.0 [ $\mu\text{m}$ ]	Conventional square. This value is given from the equipment specification.
Case 2	Searched	Searched within feasible beam-size	Optimal rectangle with feasible beam-size.
Case 3	Searched	Searched within any beam-size	Optimal rectangle with ideal beam-size.

Table 9. Length and width of characters on wafer for three cases

The numbers of EB shots obtained by our experiments are shown in Table 10. Comparing Case 1 with Case 2, 72.0% of EB shots was reduced in the best. The feasible EB size was utilized in both Cases 1 and 2 and the difference between them was whether or not the character size was optimized. The gap between Cases 1 and 2 implies that the beam size of the CP equipment should be configurable for users so that the throughput of their equipment can be increased. Supposing any size of EBs can be utilized, more reduction of EB shots can be achieved as the numbers in Case 3 in Table 10 show. Comparing Case 1 with Case 3, 75.9% of EB shots was reduced in the best. Comparing Case 2 with Case 3, 39.5% of EB shots were reduced in the best. The gap between Cases 2 and 3 implies that the development effort to seek for a larger size of EBs is capable of reducing 39.5% of EB shots. The gap between Cases 2 and 3 is directive for equipment developers to determine the EB size of their equipment.

	Circuit 1	Circuit 2	Circuit 3	Circuit 4
Case 1	52,117	41,469	26,913	164,316
Case 2	23,785	21,122	7,710	46,050
Case 3	14,379	15,120	7,710	39,546

Table 10. EB shots for the four benchmark circuits under three cases

The computing platform for experiment was an Intel Pentium 4 2.4 GHz with 1 GB of main memory. Computation times to obtain the optimal character sizes under the three cases were shown in Table 11. All character size optimization processes were finished within less than two minutes. Note that computation time was not affected by the number of cell instances but by the number of cell objects. All character size optimization processes were done within practical computation time.

	Circuit 1	Circuit 2	Circuit 3	Circuit 4
Case 1	0.00	0.00	0.00	0.00
Case 2	11.86	14.29	60.55	56.28
Case 3	27.05	32.81	96.04	86.12

Table 11. Computation time to optimize a character size [s]

Fig. 6 shows the numbers of EB shots with various character sizes for Circuit 3. The figure shows that there exists a minimal point of EB shots. The number of EB shots increases rapidly from the minimal point to the point where the size of characters is smaller while it increases gradually from the minimal point to the point where the size of characters is larger. The number of EB shots rises and falls sharply in the neighborhood of the minimal point. The experimental results show that the character size optimization was quite effective to reduce the number of EB shots and to enhance the throughput of the CP equipment.

### 3.3 Conclusion

We proposed the character size optimization technique for improving the throughput of the CP equipment by defining a mathematical problem as an ILP problem. We also showed some experimental results by solving mathematical program instances for several benchmark circuits. According to our experiment, 72.0% reduction of EB shots was achieved with a feasible EB size in the best, comparing with the conventional and intuitional character sizing. It was experimentally found that our character size optimization technique was so

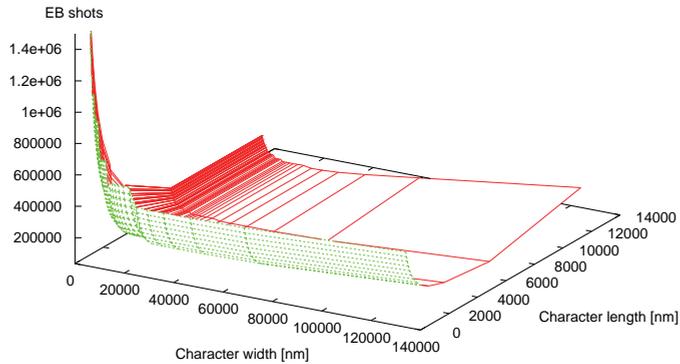


Fig. 6. The number of EB shots for Circuit 3

effective to reduce the number of EB shots. The experimental results imply that the CP equipment should be capable of modifying the size of characters by customers' demands after it is shipped out to them.

Our systematic character size optimization scheme can achieve the lower number of EB shots and can enhance the throughput of the CP equipment. The throughput enhancement of the CP equipment causes the higher production volume of semiconductor devices at a lower cost. It consequently accelerates the application of semiconductor devices to various industrial fields even if their production volumes are small. Likewise, the throughput enhancement of the CP equipment promises a lower cost in developing photomasks if the CP method is utilized in developing photomasks in the future.

#### 4. Technology mapping technique for character projection equipment

Technology mapping techniques were discussed for character projection lithography of a single-column-cell system (Sugihara et al., 2006b, 2007c). A technology mapping technique was also proposed for a multi-column-cell system (Sugihara et al., 2007a). This section mainly discusses a technology mapping technique which reduces projection time of a single-column-cell system (Sugihara et al., 2006b, 2007c).

##### 4.1 Review on technology mapping

In the most popular paradigm for logic synthesis, after a technology independent optimization of a set of logic equations, the result is mapped into a feasible circuit which is optimal with respect to area and satisfies a maximum critical-path delay. In this paradigm, the role of *technology mapping* is to finish the synthesis of the circuit by performing the final gate selection from a particular cell library. The role of technology mapping is the actual cell choice to implement the equations – for example, choosing the fastest cells along the critical path, and using the most area-efficient combination of cells off the critical path (Hachtel, 1996).

A set of base functions is chosen such as a two-input NAND-gate and an inverter. The logic equations are optimized in a technology-independent manner and are then converted into a graph where each node is restricted to one of the base functions. This graph is called the *subject graph*. The logic function for each library gate is also represented by a graph where

each node is restricted to one of the base functions. Each graph for a library gate is called a *pattern graph*. For any given logic function there are many different representations of the function using the base function set. Therefore, each library gate is represented by many different pattern graphs (Hachtel, 1996).

Let us see some examples of technology mapping for the following Boolean network:

$$F = \overline{(d + e) \cdot (a \cdot (b + h) + c) + f \cdot g \cdot h} \tag{7}$$

The Boolean network and its subject graph are shown as Fig. 7 and Fig. 8. Note that a two-input NAND-gate and an inverter are chosen as the base functions. Fig. 9 and Fig. 10 show differently technology-mapped circuits for the original one.

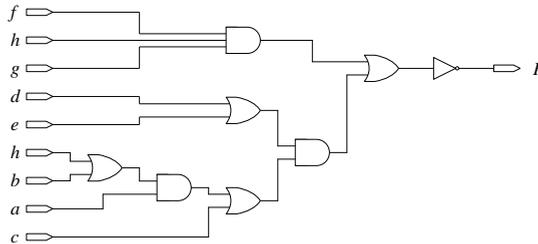


Fig. 7. A Boolean network

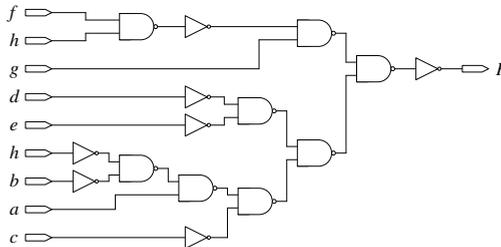


Fig. 8. A subject graph

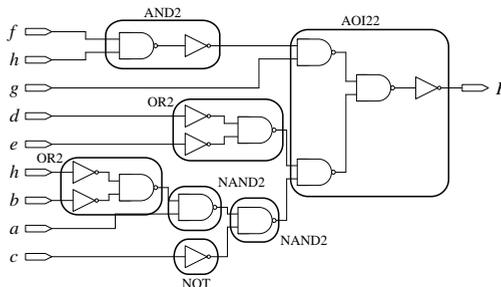


Fig. 9. A technology mapping result

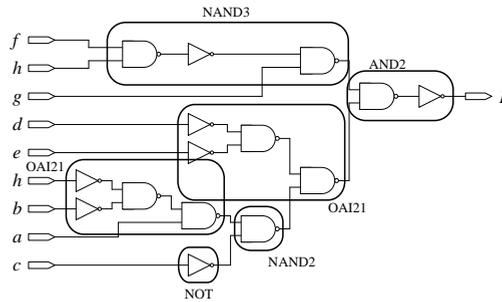


Fig. 10. Another technology mapping result

**4.2 Linear combination of area and the number of EB shots**

The conventional technology mapping does not consider the number of EB shots for the CP lithography because most ICs are fabricated with photolithography. The price of a photomask set is getting unaffordable and the CP lithography will be utilized gradually. This section discusses how to treat the number of EB shots to project an entire IC in the process of technology mapping.

Now let us discuss the objectives in technology mapping. The area of a circuit is simply represented with the sum of areas of the cell instances which are utilized for realizing the function the designers want and is shown as follows:

$$Area_{all} = \sum_i Ref_i \cdot Area_i, \tag{8}$$

where  $Area_{all}$ ,  $Ref_i$ , and  $Area_i$  are the total area of the IC, the reference count of Cell Function  $i$ , and the area of an instance of Cell  $i$  respectively. Likewise, the number of EB shots to project the entire IC is shown as follows:

$$Shots_{all} = \sum_i Ref_i \cdot Shots_i, \tag{9}$$

where  $Shots_{all}$  and  $Shots_i$  are the number of EB shots to project entire IC and that to project an instance of Cell Function  $i$  respectively.

In the conventional IC design, only Equation (6) is minimized under a timing constraint. In the design adopting the CP lithography, both of Equations (6) and (7) must be taken into account to fabricate small ICs within short fabrication time. We introduce the linear combination of  $Area_{all}$  and  $Shots_{all}$  as follows:

$$\alpha \cdot Area_{all} + \beta \cdot Shots_{all}, \tag{10}$$

where  $\alpha$  and  $\beta$  are some constant values and should be chosen depending on the importance of area and EB shots. Technology-mapped circuits which are implemented with small area and a small number of EB shots can be obtained by minimizing the objective values in Equation (10) under a timing constraint.

**4.3 Case study**

**4.3.1 Experimental setup**

We have developed a design framework in which both area and the number of EB shots can be optimized in the process of technology mapping as shown in Fig. 11. The design flow

starts with the generation of a cell library for the CP lithography. The cell library for the CP can be directly applied to a commercial logic synthesis tool. Once ASIC designers obtain the cell library for the CP, they can logic-synthesize their circuit in the same manner as the typical logic synthesis flow.

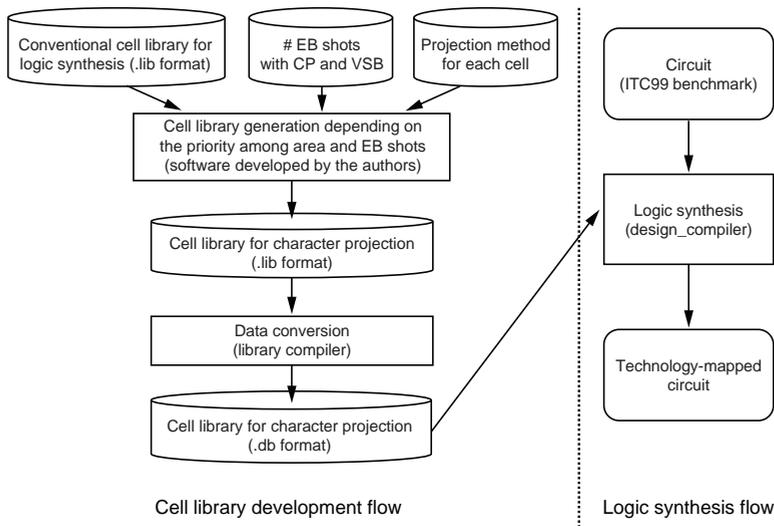


Fig. 11. Design flow in our design framework

In the design framework, a conventional cell library, the number of EB shots for every cell function, and a projection method for every cell function are required for generating a cell library specialized in the CP. The optimal projection method for every cell function can be obtained with the cell library development methodology, which we proposed in the previous work (Sugihara et al., 2005, 2006a). The simplified procedure for choosing the optimal projection method for every cell function is summarized as follows.

1. Obtain the reference counts of all cell functions, their numbers of EB shots to project a cell instance with the CP and VSB lithographies, and the number of characters available on a CP aperture mask.
2. With the above numbers, solve the mathematical problem instance shown in the previous work (Sugihara et al., 2005, 2006a). A solution to the mathematical problem instance specifies the optimal projection method for every cell functions.

To obtain the projection method for every cell functions, we have utilized a benchmark circuit, b19 from the ITC'99 benchmark circuit suite (Davidson, 1999), as a referential circuit. The benchmark circuit has been logic-synthesized to minimize its area and then the mathematical problem instance has been solved for its netlist with a commercial ILP solver (ILOG, 2003).

We adopted commercial EDA tools as possible as we could in order to reduce software development. For the design framework, we have adopted the Synopsys Design Compiler as a logic synthesis tool and the Synopsys Library Compiler as a cell library generation tool. A cell library specialized in the CP (written in the Synopsys ".lib" format) has been generated with the following three things: a conventional cell library (also written in the

Synopsys “.lib” format), the numbers of EB shots which are needed to project an instance of every cell function with the CP and VSB lithographies, and the optimal projection method of every cell function. In the cell library file format specification for the Design Compiler, the attributes designating area, delay, and power can be specified for each cell function but the number of EB shots cannot be specified. The attribute “area” has been used to represent both area and the number of EB shots by setting the linear combination of them as the attribute “area” for making the Design Compiler capable of optimizing them. And then the “.lib” file of the cell library has been converted into the Synopsys “.db” format file with the Synopsys Library Compiler.

We have utilized two cell libraries, high-performance and low-power ones, which were provided by the VLSI Design and Education Center (VDEC) at the University of Tokyo, as conventional cell libraries. The technology node of the two cell libraries was 0.35  $\mu\text{m}$ . We have demagnified all patterns of the two cell libraries by a factor of 90/350 in order to simulate the number of EB shots at the 90 nm technology node. With the two conventional cell libraries, we have generated cell libraries specialized in the CP system whose specification is shown in Table 12. The numbers of cell functions, on-characters cell functions, and off-characters cell functions are described in Table 13. Note that the cell libraries were supplied from academia and the number of cell functions is smaller than commercial ones. This means that the usage of an industrial cell library increases the number of off-characters cell functions and possibly deteriorates the throughput of the projection system in exchange for more design flexibility.

The maximum width and height of rectangles for VSB	3.5 $\mu\text{m}$
The width and height of characters for CP	5.0 $\mu\text{m}$
The number of characters available on a CP aperture mask	440

Table 12. Specification of projection equipment

	# cells	# cells on characters	# cells off characters
High performance cell library	310	53	257
Low power cell library	310	101	209

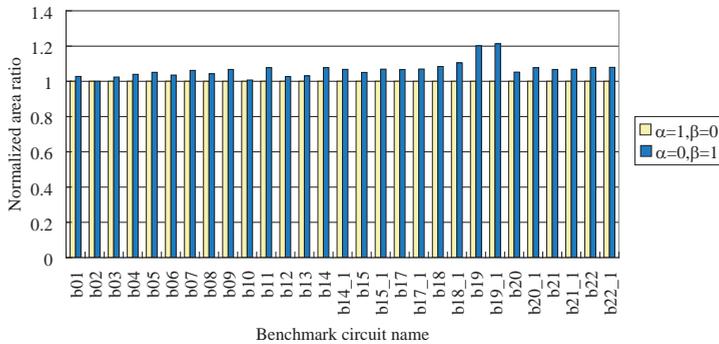
Table 13. Two cell library description

### 4.3.2 Experimental results

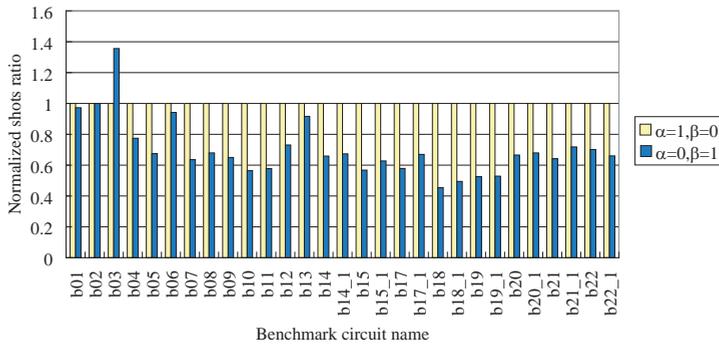
We examined the numbers of EB shots to project several benchmark circuits with the two cell libraries.

First, we examined the relation between area and the number of EB shots to project each of ITC'99 benchmark circuits (Davidson, 1999). In the examination, all circuits were logic-synthesized for two objectives: area-minimization ( $\alpha=1$ ,  $\beta=0$  in Equation (8)) and EB-shots-minimization ( $\alpha=0$ ,  $\beta=1$  in the equation). The purpose of this examination was to obtain the minimal values of both area and EB shots of all benchmark circuits. We logic-optimized each of circuits ten times and have taken the best value of area and EB shots among the results. Fig. 12 and Fig. 13 show area and shots ratios for both area-minimized logic synthesis ( $\alpha=1$ ,  $\beta=0$ ) and shots-minimized one ( $\alpha = 0$ ,  $\beta = 1$ ) with the two cell libraries, respectively.

Depending on  $\alpha$  and  $\beta$ , the cell library was optimized for Circuit b19. The cell library is equivalent to the original one under  $\alpha=1$  and  $\beta=0$ . The area and EB shot count are normalized with those of area-minimized circuits. Note that the numbers of EB shots shown in the figures are the ones for projecting the FEOL patterns. They do not include any EB shots to project the BEOL patterns. Shots-minimizing logic synthesis reduced 54.6% of EB shot count at the best case in exchange for 8.4% area increase. Shots-minimization logic synthesis has increased 0.0% to 24.0% of area on logic-synthesizing all circuits.

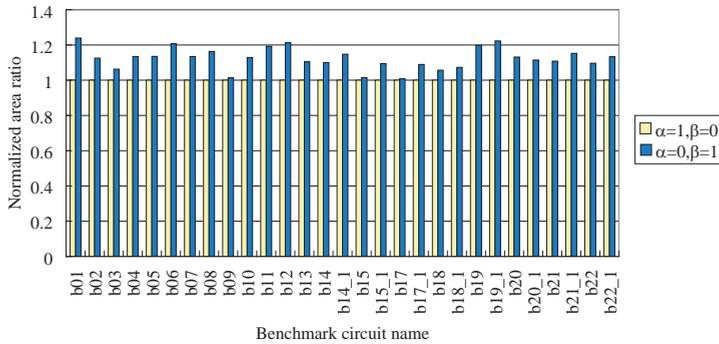


(a) Area under area- and EB shots-minimizations

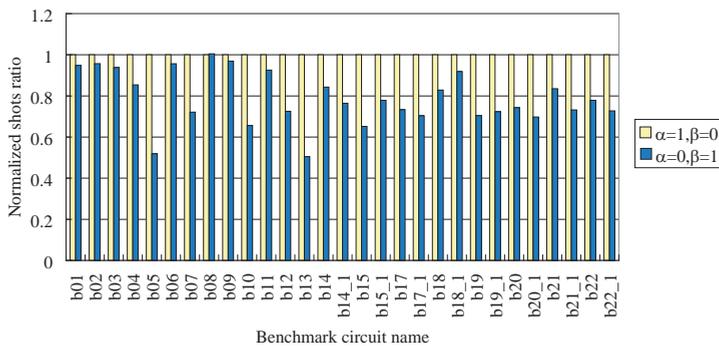


(b) The number of EB shots under area- and EB shots-minimizations

Fig. 12. Area and the number of EB shots of ITC'99 benchmark circuits with HP cell library



(a) Area under area- and EB shots-minimizations



(b) The number of EB shots under area- and EB shots-minimizations

Fig. 13. Area and the number of EB shots of ITC'99 benchmark circuits with LP cell library

Changing ratio  $\beta/\alpha$ , we examined the relation between area and the number of EB shots for a benchmark circuit, b18\_1, as shown in Fig. 14. We show the range of both area and the number of EB shots observed in the process of ten logic optimizations in the figure in order to observe the tendency of area and the number of EB shots to change. This is because the logic synthesis tool returns quasi-optimal circuits with some variation of both area and EB shots and makes it hard to observe a consistent tendency of them. The figure shows that area tends to increase as the ratio  $\beta/\alpha$  increases while the number of EB shots tends to decrease. These results show that there exists a tradeoff between area and the number of EB shots. We think that area-saving and off-characters cell functions are mapped as area is important. Such cell functions are substituted on-characters ones as the number of EB shots becomes important. ASIC designers should choose the ratio  $\beta/\alpha$  according as they want to reduce area or the number of EB shots.

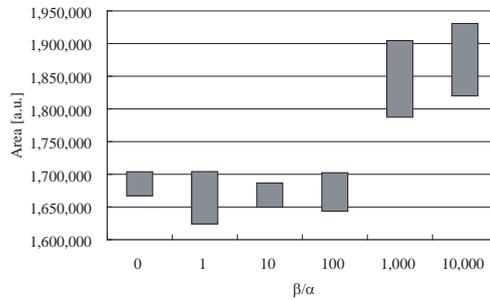
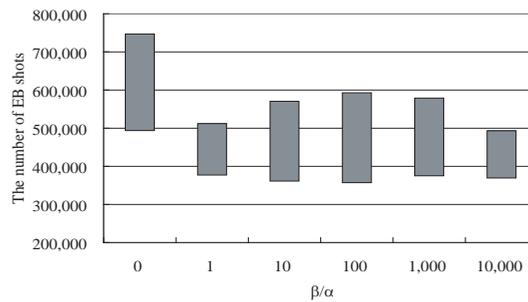
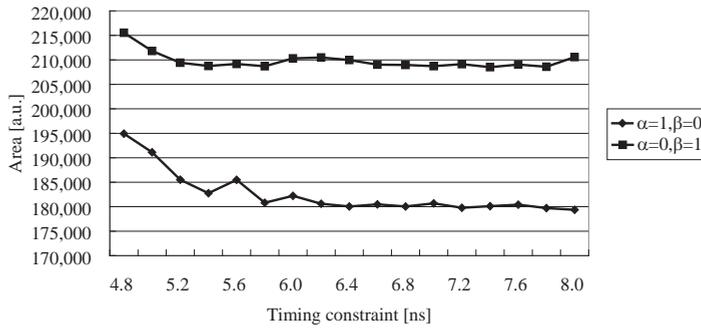
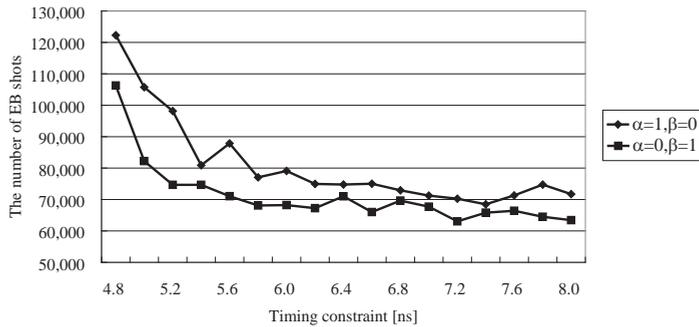
(a) Area versus  $\beta/\alpha$ (b) The number of EB shots versus  $\beta/\alpha$ 

Fig. 14. Tradeoff between area and the number of EB shots

We have examined area and the number of EB shots under several timing constraints with a Z80-compatible processor. Fig. 15 and Fig. 16 show area and the number of EB shots under various timing constraints. When timing constraints were given, the effectiveness of the shots-minimization and area-minimization became less but the number of EB shots was reduced up to 26.6% nevertheless. The area increase accompanied with EB shots minimization was from 10.6% to 46.2%. These results show that area and the number of EB shots decreased as the timing constraint was loosened. We think that there exists a tradeoff between delay time and the number of EB shots (or area). A timing constraint for shorter delay time causes logic synthesis tools to choose off-characters cell functions that have higher current drivability. Such cell functions have larger transistors and require many EB shots to be projected with the VSB lithography.



(a) Area versus timing constraint



(b) The number of EB shots versus timing constraint

Fig. 15. Area and the number of EB shots with the HP cell library under timing constraints

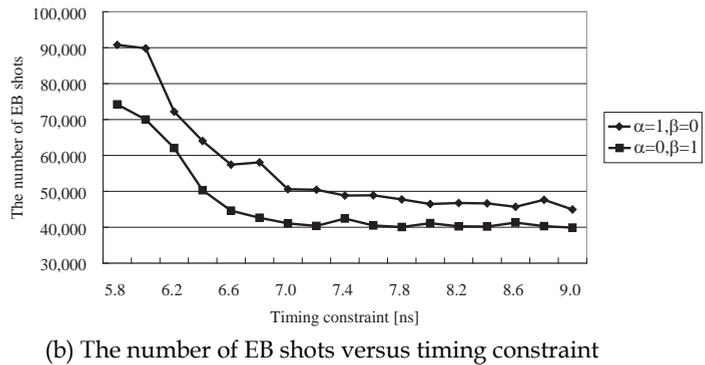
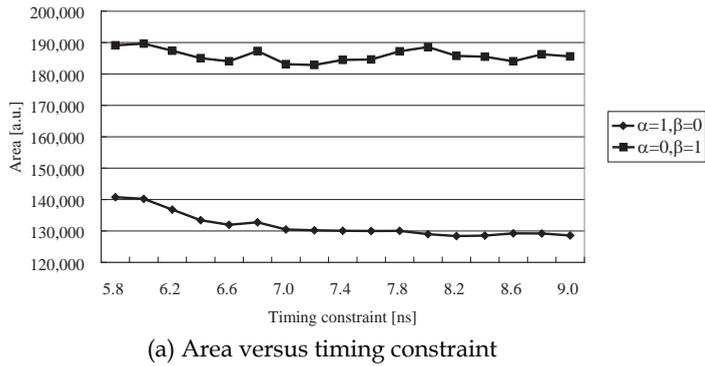


Fig. 16. Area and the number of EB shots with the LP cell library under timing constraints

#### 4.4 Conclusion

Our technology mapping technique for the CP lithography achieved a 54.6% less number of EB shots with 8.4% area increase under no timing constraints than the conventional one. Our technology mapping for the CP lithography also achieved a 26.6% less number of EB shots with 41.1% area increase and without any performance degradation than the conventional one. Varying the ratio  $\beta/\alpha$ , we found that there exists a tradeoff between area and the number of EB shots.

In the other experiments, tightening timing constraint increased area and the number of EB shots. It was found that there exists a tradeoff between delay time and the number of EB shots. We think that a timing constraint for shorter delay time has caused a logic synthesis tool to choose the off-characters cell functions that have higher current drivability.

Our technology mapping technique reduced the number of EB shots to project patterns for the FEOL with some area increase. It is probable that some increase of cell instances causes the number of wires to increase and does the number of EB shots for projecting the BEOL patterns to increase. A technology mapping technique should be studied for reducing the number of EB shots required for both the FEOL and the BEOL patterns as future work.

The number of cell functions which are placed on a CP aperture mask will increase as the technology node proceeds. It is probable that all cell functions of a commercial cell library, which includes more than 500 cell functions, will be placed on a single CP aperture mask at the 32 nm technology node. This indicates that the VSB lithography will be required less and less for projecting such cell functions. We suppose that our technology mapping technique is effective before the 32 nm technology node. We think that another technology mapping technique will be needed to increase throughput of MCC systems after the 32 nm technology node.

It is easy for both IC designers and equipment developers to adopt our technology mapping technique because a software approach such as our technique imposes no modification on CP equipment. This means that no additional cost is necessary to adopt our technique in their IC design.

#### 5. Conclusion

Character projection lithography is one of promising projection methods for manufacturing application specific integrated circuits at a low cost. From the viewpoint of ASIC design, the number of EB shots, which reflects the manufacturing cost for ASICs, is reduced by (i) cell library generation and (ii) technology mapping.

Cell library generation consists of two parts: cell selection and character sizing. We presented a cell selection method (Sugihara et al., 2005, 2006a) and character sizing methods (Sugihara et al., 2006c, 2007b). Cell selection and character sizing achieved 72.0% reduction of EB shots with a feasible EB size in the best, comparing with the conventional and intuitional character sizing.

We also presented a technology mapping technique for reducing the number of EB shots in character projection lithography. Our technology mapping technique for the CP lithography has achieved a 54.6% less number of EB shots with 8.4% area increase under no timing constraints than the conventional one. Our technology mapping for the CP lithography has also achieved a 26.6% less number of EB shots with 41.1% area increase and without any performance degradation than the conventional one. Our experiments suggested that there exists a tradeoff between area and the number of EB shots.

## 6. Acknowledgment

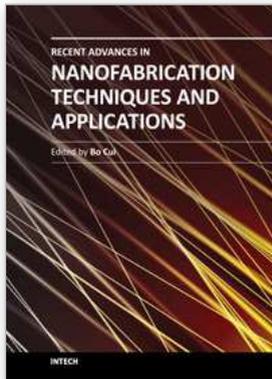
This work was supported by the VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc.

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## **Recent Advances in Nanofabrication Techniques and Applications**

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Nanotechnology has experienced a rapid growth in the past decade, largely owing to the rapid advances in nanofabrication techniques employed to fabricate nano-devices. Nanofabrication can be divided into two categories: "bottom up" approach using chemical synthesis or self assembly, and "top down" approach using nanolithography, thin film deposition and etching techniques. Both topics are covered, though with a focus on the second category. This book contains twenty nine chapters and aims to provide the fundamentals and recent advances of nanofabrication techniques, as well as its device applications. Most chapters focus on in-depth studies of a particular research field, and are thus targeted for researchers, though some chapters focus on the basics of lithographic techniques accessible for upper year undergraduate students. Divided into five parts, this book covers electron beam, focused ion beam, nanoimprint, deep and extreme UV, X-ray, scanning probe, interference, two-photon, and nanosphere lithography.

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