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Subthreshold Frequency Synthesis for Implantable Medical Transceivers

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1. Introduction

Implantable medical devices (IMDs) have evolved greatly since the first pacemaker was designed in the 1950s. The current generation of IMDs are capable of replacing damaged or malfunctioning organs, and are designed for long-term patient care. Cochlear implants, which differ greatly from hearing aids, convert received audio signals to electrical impulses and are capable of bypassing damaged parts of the ear and interfacing directly with auditory nerves. Microstimulators for neuromuscular stimulation can restore functionality to paralysed limbs. Implantable drug administration devices can deliver precise amounts of a drug, such as insulin for diabetics, at particular intervals, replacing the need for regular injections. Wireless IMDs designed for biotelemetry applications include implantable ECG and EEG recording, intra-ocular pressure sensing and wireless endoscopy capsules. In order to address the unique design requirements of wireless IMDs, namely ultra-low power consumption to extend battery life, small form factor to make the device suitable for implantation, and reliability to ensure correct operation once implanted, circuit designers must use new topologies and design techniques when conventional designs fail to address these requirements. In this work, we propose several novel circuits for an integer-N frequency synthesizer operating in the 402 MHz to 405 MHz Medical Implant Communication Service (MICS).

2. Design specifications

The designs presented in this work consist of novel circuits for an ultra-low power CMOS integer-n frequency synthesizer for use in a wireless implantable medical device operating the the 402 MHz to 405 MHz Medical Implant Communication Service spectrum. The architecture of an integer-n frequency synthesizer is shown in Fig. 1. In order to be suitable for use in an implantable device, the synthesizer should utilize as few off chip components as possible (ideally none) to achieve the required specifications and functionality, and to decrease its physical size and cost, be as insensitive as possible to process variations and temperature in order to provide accurate and stable carrier frequencies for data transmission under all conditions, and consume minimal power resulting in maximum lifetime of the device.
Frequency synthesizers and phase-locked loops have been covered extensively in literature (Gardner, 2005), (Lee, 2004), (Razavi, 2001), (Razavi, 1998), and the reader is encouraged to review those references for a thorough treatment of frequency synthesis. The main components of the frequency synthesizer are the phase/frequency detector, charge pump, loop filter, voltage-controlled oscillator and programmable frequency divider. For the

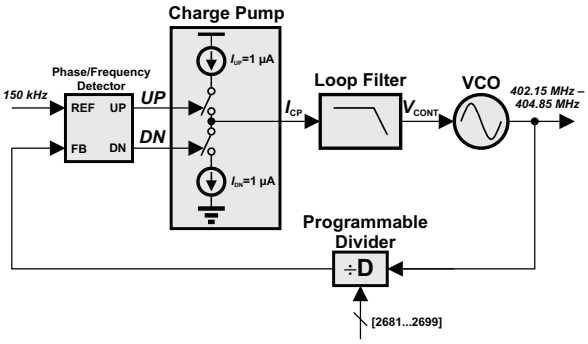


Fig. 1. Proposed integer-n frequency synthesizer.

purposes of this work, it is enough to say that frequency synthesizers generate a multitude of frequencies from a fixed reference frequency. The relationship between the output frequency and input frequency is $f_{OUT} = D \times f_{IN}$, and by changing the control word of the programmable divider, different output frequencies can be generated which satisfy this relationship. For integer-n frequency synthesizers, f_{IN} must be equal to the channel spacing.
The application for the proposed frequency synthesizer is the Medical Implant Communication Service frequency band, which was established in 1999 for use by implantable medical devices. Favourable propagation characteristics, international availability and low probability of interference are the reasons for choosing the 402 MHz to 405 MHz spectrum for the MICS band. Although there is no fixed channel arrangement for the MICS band, an MICS channel is permitted to have an emission bandwidth between 25 kHz and 300 kHz. In the proposed frequency synthesizer, we will use the maximum bandwidth of 300 kHz per channel, resulting in 10 channels (Fig. 2).
In this work, novel designs for the main components of the integer-n frequency are proposed to address the design constraints of implantable medical devices. The proposed designs are implemented using a 130 nm CMOS process from IBM and simulated using Cadence Spectre circuit simulator.

3. The proposed current-reuse quadrature voltage-controlled oscillator

Since the first quadrature *LC*-tank VCO was proposed (Rofougaran et al., 1996), a number of modified topologies have been presented which improve RF performance metrics such as phase noise and quadrature accuracy. These include the disconnected-source QVCO (DS-QVCO) (Mazzanti et al., 2006), the series QVCO (SQVCO) (Chamas & Raman, 2007b), the phase-tunable QVCO (PT-QVCO) (Chamas & Raman, 2007a), and the transformer-coupled

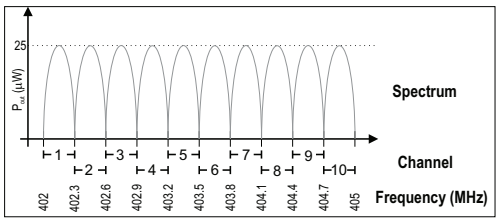
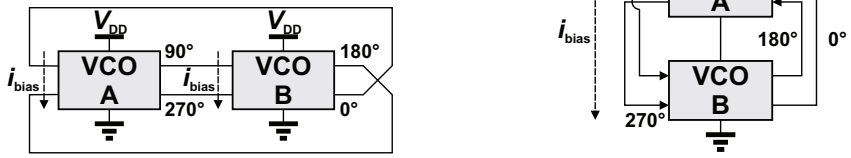


Fig. 2. Allocated frequency spectrum for Medical Implant Communication Service.



(a) Conventional QVCO.

(b) Proposed QVCO with current-reuse.

Fig. 3. Quadrature VCO block diagram.

QVCO (TC-QVCO) (Ng & Luong, 2007). However there have not been many attempts to reduce the power consumption of the QVCO. In order to make the *LC* QVCO a viable choice for ultra-low power applications, such as implantable medical devices, we propose a novel QVCO topology utilizing three design principals to lower the power consumption: current-reuse, supply voltage scaling and weak inversion operation.

3.1 Circuit design

Existing QVCO topologies consume significant amounts of power, making them unsuitable for ultra-low power applications such as IMDs. Increasing the quality factor of the tank to achieve high oscillation amplitude for small bias currents has it's limits, since the quality factor of inductors in CMOS processes is typically between 10 to 20. Therefore, it is necessary to explore other means to reduce power consumption of the QVCO. One of the salient properties of the QVCO is that its power consumption is double that of the standard *LC* VCO, as shown in Fig. 3(a). When stacking two different circuits, the performance of one circuit may be compromised because it may have better performance when biased independently. However in the QVCO both oscillator cores are ideally identical, thus current reuse is viable and will provide a 50% improvement in power consumption. The conceptual QVCO with current-reuse (CR-QVCO) is shown in Fig. 3(b), where two coupled *LC* tank oscillators are stacked between the supply rails.

The circuit implementation of the CR-QVCO is shown in Fig. 4. In this topology, the oscillator nodes for both cores are at the same DC level (ignoring the losses across the inductors), eliminating the need for DC level shifting of the coupling transistor inputs and the use of a frequency tuning circuit for the varactors. The capacitor, C_{GND}, at the intermediate node provides AC ground for both oscillators, and allows the cores to be decoupled for analytical purposes. An expression for the QVCO oscillation amplitude was given in (Andreani et al., 2002), however the equation requires modification due to the loading effect of the coupling transistors (Rofougaran et al., 1998) and the use of a differential spiral inductor:

$$\hat{V_0} = \frac{1}{\sqrt{2}\pi}(1-\delta) I_{bias} R_p. \tag{1}$$

When the CR-QVCO is to be designed for weak inversion (subthreshold) operation the supply voltage can be approximated as

$$V_{DD} = V_{thn} + \left|V_{thp}\right| + V_{DSAT}, \tag{2}$$

where V_{thn} and V_{thp} are the threshold voltages of the NMOS and PMOS transistors respectively, and V_{DSAT} is the saturation voltage of the current source transistor. Since the transistors are biased in the subthreshold region, the supply voltage can be lower than this value because the DC bias points of the switching transistors will be less than $V_{thn,p}$.

To reduce the current drawn by the CR-QVCO, an inductor with high inductance and quality factor was used. The inductors provided with the PDK did not provide high quality factors at low frequencies ($>$ 1 GHz), which required the use of a custom spiral inductor. Cadence Virtuoso Passive Component Designer was used to synthesize a symmetrical octagonal inductor with high inductance and quality factor at the center frequency of the MICS band. The inductor was formed over an M1 groundplane to decrease substrate coupling and raise the quality factor (Yue & Wong, 1998). The layout of the synthesized inductor and its simulated inductance and quality factor are shown in Fig. 5.

The bias current was provided using the PMOS transistor. The upconversion of flicker noise generated by the current source transistor is a known contributor to the phase noise of the oscillator. To combat this effect, the PMOS bias current transistor was sized to have long channel length and width as flicker noise is inversely proportional to the area of the active device. NMOS varactors were used as the frequency tuning element in the tank, and a fixed metal-insulator-metal (MIM) capacitor was used to set the tuning range around the frequency band of interest. Existing CR-QVCOs require the use of a frequency tuning circuit that accounted for the different DC voltages between the differential output nodes, which resulted in different voltage drops across the varactors in each tank. By designing the CR-QVCO such that the top tank is PMOS only and the bottom tank is NMOS only, a frequency tuning circuit was not necessary as the DC voltage of the quadrature outputs was the same. A small DC offset can be attributed to series resistance of the inductors. Omitting the frequency tuning circuit also improves the phase noise as the thermal noise generated by biasing resistors is not present.

3.2 Results

Voltage-controlled oscillators are subjected to variations due to process, supply voltage and temperature which cause the oscillation frequency to drift from the nominal value. In order to ensure the CR-QVCO can operate on across the MICS frequency band, simulations were

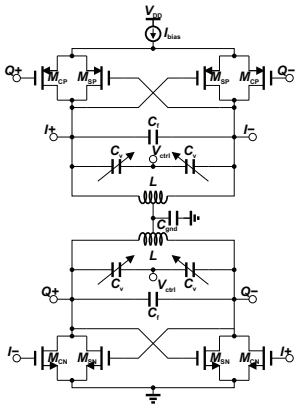
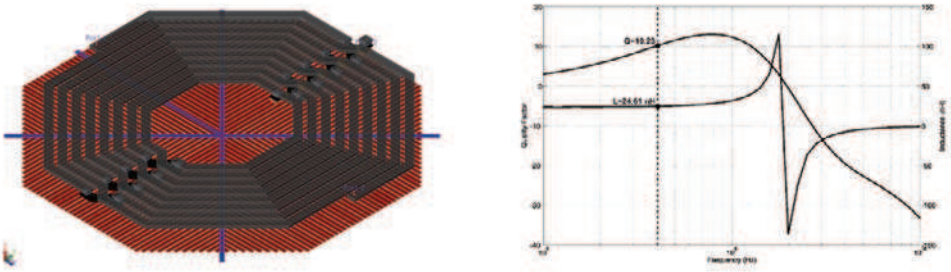


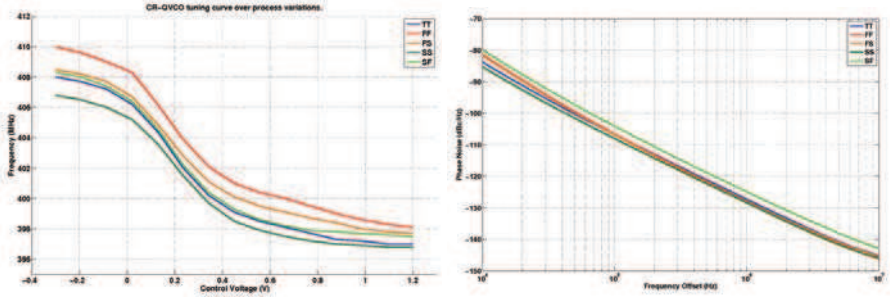
Fig. 4. Current-reuse quadrature voltage-controlled oscillator.



(a) Three dimensional view. (b) Simulated inductance and quality factor

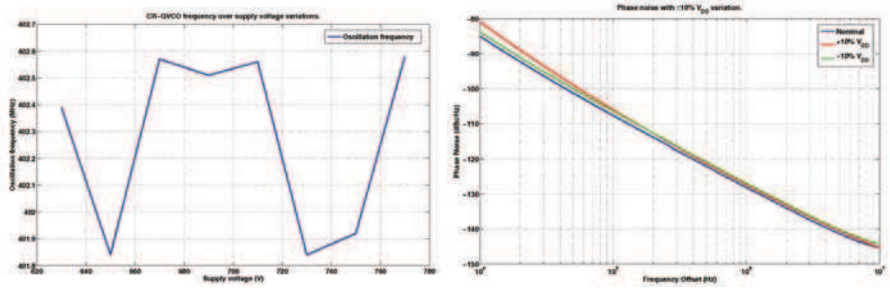
Fig. 5. Synthesized spiral inductor for current-reuse quadrature VCO.

performed to verify its oscillation frequency. The results of corner analysis and supply voltage sensitivity are shown in Fig. 6 and Fig. 7 respectively (biasing adjusted for each simulation to achieve same oscillation amplitude).
As per the requirements of the MICS frequency band, the IMD must be tested over temperature variations from 0° C to 55° C (Federal Communications Commission, 1999).



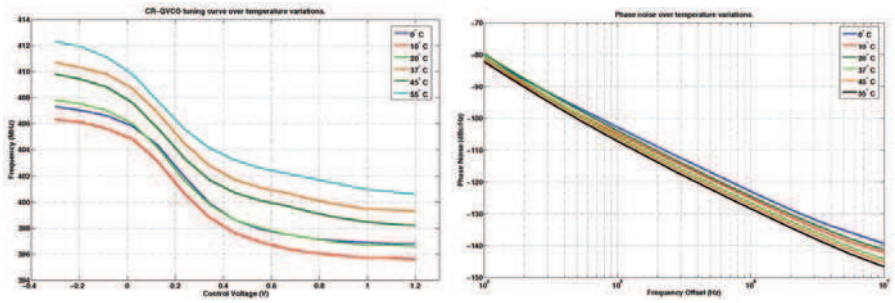
(a) Tuning range. (b) Phase noise.

Fig. 6. CR-QVCO simulated over process variations.



(a) Free-running frequency. (b) Phase noise.

Fig. 7. CR-QVCO simulated over ± 10% supply voltage variations.



(a) Tuning range. (b) Phase noise.

Fig. 8. CR-QVCO simulated over temperature variations.

Although the proposed work is not a complete IMD, the CR-QVCO performance at different temperatures in the required range was simulated to ensure the operating frequency and phase noise do not degrade significantly. The graphs in Fig. 8 show the tuning curves and phase noise plots for simulations at 0° C, 10° C, 20° C, 37° C, 45° C and 55° C.
The CR-QVCO consumed 600 μW from a 0.7 V supply, and the phase noise was -127.2 dBc/Hz. The simulation results of the proposed CR-QVCO were compared with existing VCOs designed to operate in the MICS band, and are summarized in Table 1.
As shown in the comparison results, the proposed CR-QVCO demonstrates improved power consumption and phase noise performance. Although both (Bae et al., 2009) and (Ryu et al., 2007) have lower power consumption, it is important to note that these designs do not produce quadrature signals. If the VCOs in these works were used to implement a PQVCO to produce quadrature signals, the power consumption would at least double. Furthermore the VCOs use off-chip inductors with high Q values. Although off-chip inductors are a valid method

Reference (Technology)	Tuning Range [MHz]	V_{DD} [V]	Power [mW]	Phase Noise [dBc/Hz]	Topology
This work (0.13 μm)	**398 to 410**	**0.7**	**0.42**	**-127.2 @ 1 MHz**	**Current-reuse quadrature oscillator**
(Carrara et al., 2009) (0.13 μm)	401 to 406	1.2	0.72	-96 @ 1 MHz	LC tank VCO
(Tekin, Yuce, Shabani & Liu, 2006) (TSMC 0.18 μm)	——	1.5	1.11	——	Differential ring VCO
(Liu et al., 2009) (TSMC 0.18 μm)	402	1.3	0.78	——	6-bit digitally controlled oscillator
(Bae et al., 2009) (0.18 μm)	398 to 408	0.7	0.21	-118 @ 1 MHz	7-bit digitally controlled oscillator
(Bohorquez et al., 2009) (0.09 μm)	391 to 415	0.7	0.46	-108 @ 100 kHz	Digitally controlled oscillator
(Liu et al., 2006) (TSMC 0.18 μm)	——	1.5	——	——	Dual band LC tank VCO
(Tekin, Yuce & Liu, 2006) (TSMC 0.18 μm)	——	1.5	1.2	-98 @ 160 kHz	LC tank VCO
(Li et al., 2009) (0.13 μm)	380 to 440	1.2	1.2	-107 @ 100 kHz	Injection-locked oscillator
(Ryu et al., 2007) (0.18 μm)	440	1.5	0.231	-103 @ 100 kHz	Single-ended cross-coupled oscillator

Table 1. Comparision of existing MICS VCOs

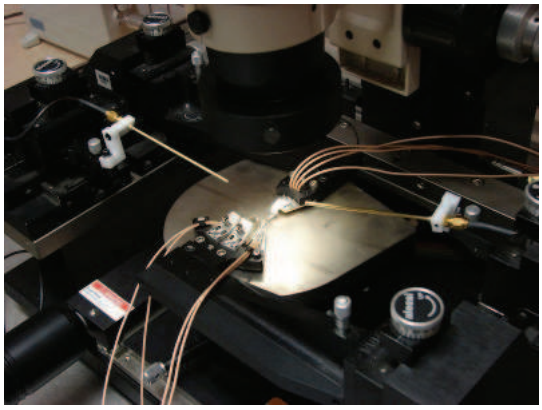
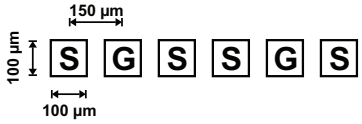


Fig. 9. Wafer probe station

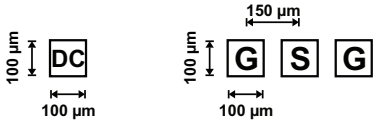
of reducing power consumption, their use violates one of the objectives of this work in this thesis which is to eliminate the need for off-chip components to lower the size and cost of the frequency synthesizer.

The proposed CR-QVCO was fabricated using a 130 nm CMOS process from IBM through MOSIS Integrated Fabrication Service to provide validation of the design beyond simulation results. Testing of the integrated circuit was performed using wafer probing on a Cascade Microtech IC probe station. Each of the four positioners on the probe station is capable of holding a different set of probes for applying and measuring signals to and from the device under test. The available probe configurations were Ground-Signal-Ground (GSG) operating at up to 40 GHz, Signal-Ground-Signal-Signal-Ground-Signal (SGSSGS) "wedge" operating up to 100 MHz, and a DC needle. The wafer probe station and probe pad configuration diagrams are shown in Fig. 9 and Fig. 10 respectively. The square probe pads have side lengths of 100 μm and a pitch of 150 μm.

The CR-QVCO had four RF outputs ($I+$, $I-$, $Q+$, $Q-$) and four DC bias voltages (core V_{DD}, V_{cont}, V_{bias}, and buffer V_{DD}). To implement the required input and output configuration four sets of probe pads for the GSG probes were used (only two could be probed at a time), a DC needle was used for the output buffer supply voltage and the SGSSGS wedge was used for

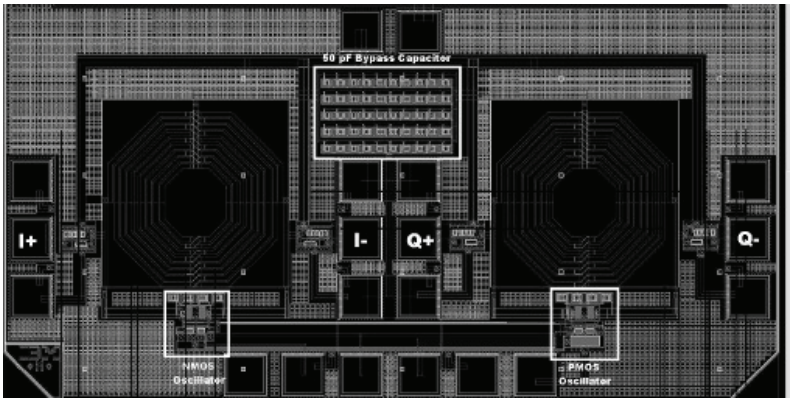


(a) SGSSGS

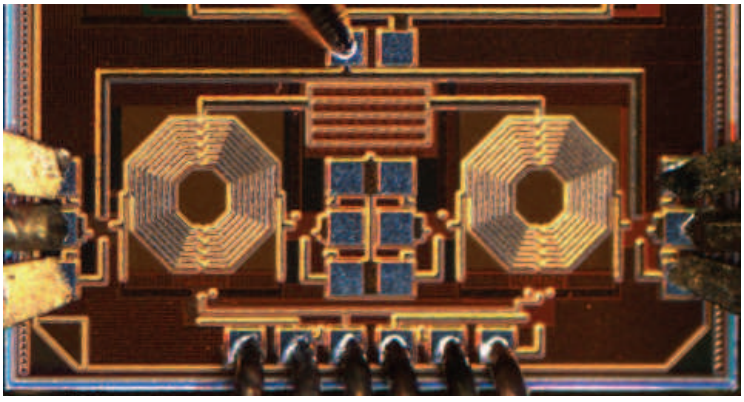


(b) DC needle (c) GSG

Fig. 10. Probe configurations



(a) CR-QVCO layout.



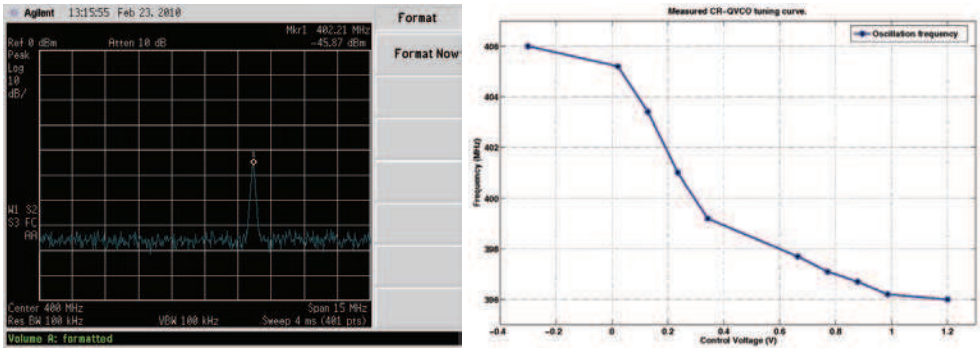
(b) CR-QVCO die photo.

Fig. 11. Physical implementation of current-reuse quadrature VCO.

the remaining DC signals. The layout and die photo of the CR-QVCO are shown in Fig. 11. The total silicon area occupied by the CR-QVCO including bond pads was 2 mm $\times$ 1 mm. Measurement results were obtained using an Agilent 4407B spectrum analyser, and power and bias voltages were provided using two high precision DC sources. The measured output spectrum and control voltage are shown in Fig. 12. The tuning curve was obtained by adjusting the control voltage across the desired range and observing the change in the output spectrum. It can be observed that although the frequency range of the MICS is covered, the total tuning range is narrower than the desired range due to parasitics and other variations in the fabrication process such as increased capacitance density of the MIM capacitors or smaller tuning range of the varactors.

4. The proposed source-coupled logic clear/preset D-latch

D-type latches and flip-flops are important components of the frequency synthesizer. The conventional phase/frequency detector, which consists of two resettable D flip-flops and an



(a) Output spectrum. (b) Tuning range.

Fig. 12. Measurement results of CR-QVCO.

AND gate, has its UP and DN outputs cleared when $UP \cdot DN = 1$. The Pulse and Swallow counters in the programmable frequency divider are programmed to their initial value by clearing and presetting the D flip-flops, each corresponding to a bit in the control word. Previously proposed low power programmable frequency dividers and phase/frequency detectors were implemented using true single-phase clocked (TSPC) logic (Lee et al., 1999), (Kuo & Wu, 2006), (Kuo & Weng, 2009), (Lei et al., 2009). Although TSPC logic occupies small silicon area, it suffers from drawbacks such as generation of switching noise, charge leakage at low frequencies, and requires rail-to-rail input signal swing (Luong, 2004). These drawbacks can be avoided by using source-coupled logic (SCL) at the expense of increased silicon area. Additionally these implementations were designed for saturation region operation and therefore their power consumption is high relatively compared to ultra-low power requirements. These reasons provide the motivation for choosing the SCL logic family for implementing the programmable frequency divider and phase/frequency detector.
Existing SCL latches presented in literature are not suitable for applications such as implantable medical devices because they required too many stacked transistors (Cong et al., 2001), (Desikachari et al., 2007) or do not perform both clear and preset functions (Cheng & Silva-Martinez, 2004), (Dai et al., 2004). To this end, we present a SCL D latch with clear and preset capability which is suitable for low power, low voltage applications.

4.1 Circuit design

The proposed D-latch is shown in Fig. 13. It consists of two stages and requires an additional input to enable the clear and preset circuit. The first stage is a latch where the sensing pair ($M1, M2$) is active while CLK is high and the latching pair ($M3, M4$) is active while CLK is low. Instead of cross coupling the outputs of the sensing pair via the latching pair as in a conventional SCL D-latch, the intermediate outputs ($X, \overline{X}$) are routed to the second stage. Devices $M5, M6$ act as a buffer when EN is low, and the outputs are fed back to the latching pair. When EN is high, the Set/Reset latch ($M7, M8$) is active and the latch is initialized according to the state of CLR and PRE. The complementary enable signals can be generated by

$$EN = CLR \oplus PRE, \tag{3a}$$

$$\overline{EN} = \overline{CLR \oplus PRE}. \tag{3b}$$

This comes at the cost of an additional XOR/XNOR gate, since SCL gates produce complementary outputs. However in this application EN can be obtained from the $RELOAD$ signal generated by the pulse counter in the programmable frequency divider or by the AND gate output in the phase/frequency detector, eliminating the need for the additional logic gate. The clear/preset circuit in the D-latch avoids the $S = R = 1$ state since when CLR and PRE are both high, EN is low and the D-latch continues to operate normally.
In (Tajalli et al., 2008), the authors demonstrated that a high resistance load device can be obtained by shorting the bulk of a minimum sized PMOS transistor to its drain, reducing the amount of bias current required to achieve an output voltage sufficient to drive subsequent gates. By exploiting this result in the design of the proposed clear/preset D-latch, the power consumption can be significantly reduced when compared with conventional SCL logic.

4.2 Results

The proposed D-latch was simulated along with an ideal D-latch written in Verilog-A to verify that the proposed design produces the correct output. The latch was simulated for two cases to verify that it can operate over the required frequency range. In Fig. 14(a), the frequency of the data and clock inputs are 250 kHz and 120 kHz respectively, and in Fig. 14(b) they are 20 MHz and 15 MHz respectively.
To demonstrate the clear and preset functionality, the proposed D-latch was connected in a master-slave D flip-flop divide-by-two configuration and alternating PRE and CLR signals were applied every 20 ns. As shown in Fig. 15 the output signal (V_{CLKOUT}) is pulled high when V_{PRE} is applied, and pulled low when V_{CLR} is applied.

5. A subthreshold source-coupled logic pulse/swallow programmable divider

The pulse-swallow frequency division architecture shown in Fig. 16 is used in the proposed design. It consists of a dual-modulus prescaler and two programmable counters, referred to as the Pulse counter and Swallow counter. The DMP divides by M when MC is logic 0 and by $M + 1$ when MC is logic 1, and the programmable counters are initialized by N-bit control words and count down from that value, then reload from zero to the value of the control

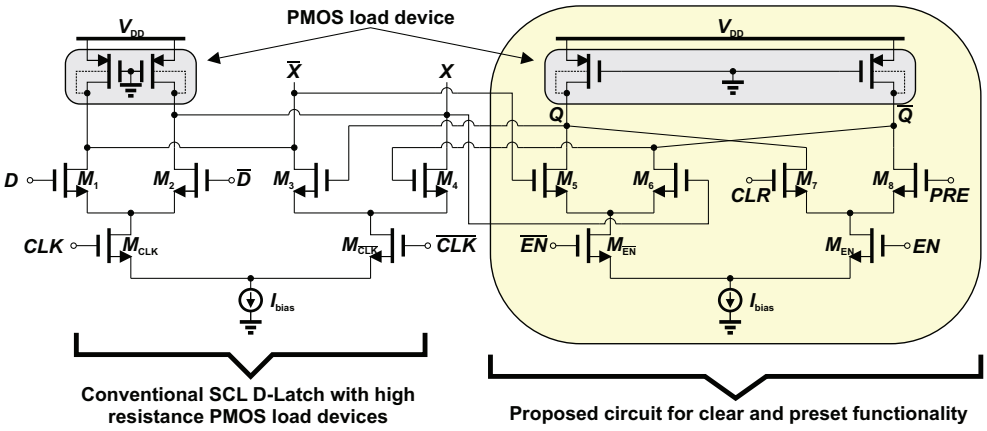
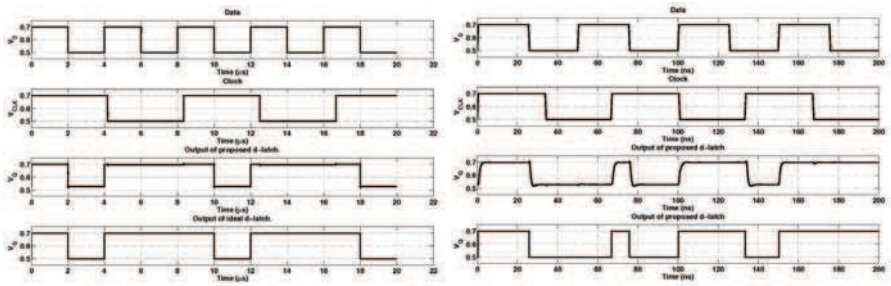


Fig. 13. Proposed D-latch with clear and preset.



(a) D=250 kHz, CLK=120 kHz. (b) D=20 MHz, CLK=15 MHz.

Fig. 14. Transient simulation of proposed D-latch and ideal D-latch.

word. The programmable divider operates as follows: When a CLK_{OUT} pulse is generated by the Pulse counter, both counters reload to their initial states and the MC signal goes high. The initial states are determined by the S and P control words. The DMP divides CLK_{IN} by $(M+1)$ until the swallow counter has counted down to 0. The Swallow counter generates a CLK_{OUT} pulse which changes the MC to low and the DMP divides CLK_{IN} by M until the Pulse counter has counted down to 0. The Pulse counter generates a CLK_{OUT} pulse and the process repeats. Since the DMP divides by $(M+1)$ S times and by M $(P-S)$ times, the division ratio, D, of the programmable divider is given by

$$D = (M+1)S + (P-S)M, \tag{4}$$

$$= MP + S. \tag{5}$$

5.1 Circuit design

The synthesizer must be able to operate on one of the 10 channels in the 402 MHz to 405 MHz spectrum, with each channel spaced 300 kHz apart. Intuitively one would design the divider so that the output frequency is the center frequency of the i^{th} channel,

$$f_{OUT} = 402.15 \text{ MHz} + \text{(i-1)}300 \text{ kHz}. \tag{6}$$

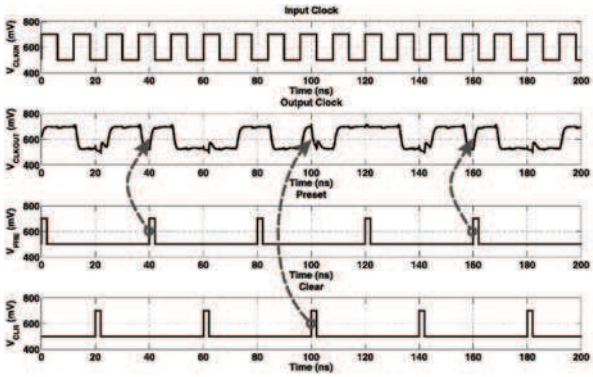


Fig. 15. Simulation of D-flip flop with clear and preset.

Channel #	f_{out}	D
1	402.15 MHz	2681
2	402.45 MHz	2683
3	402.75 MHz	2685
4	403.05 MHz	2687
5	403.35 MHz	2689
6	403.65 MHz	2691
7	403.95 MHz	2693
8	404.25 MHz	2695
9	404.55 MHz	2697
10	404.85 MHz	2699

Table 2. Division ratios for integer-n frequency synthesizer with 150 kHz reference frequency.

However, the corresponding divider moduli calculated by $D = \frac{f_{OUT}}{f_{IN}}$ and $f_{IN} = 300$ kHz result in non-integer values. Integer value of the division ratio by changing the synthesizer reference frequency from 300 kHz to 150 kHz. Table 2 summarizes the required division ratios for the integer-n frequency synthesizer.
Now that an integer value of D has been obtained, the dual-modulus divider, pulse counter and swallow counter values must be obtained to satisfy (5). By using a divide-by-32/33 dual-modulus divider (M=32), the values of the pulse (P) and swallow (S) counters can be obtained by assuming a value for P and solving for the range of values for S. If we assume P=83,

$$S = D - MP \tag{7}$$
$$= 2699 - (32)(83) \tag{8}$$
$$= 2699 - 2656 \tag{9}$$
$$= 43, \tag{10}$$

and so on for the remaining values of D. Using these values, the range of S is [25, 27, ... 43], therefore the P counter must be 7-bits and the S counter can be a 6-bit counter. The pulse counter has a fixed modulus and its control bits can be set on-chip, but the swallow counter must be programmable – either off-chip or by separate control logic. Consider the control word $S[5:0] = S_5S_4S_3S_2S_1S_0$, the control bits are assigned as shown in Table 3.
By analysing the truth table of Fig. 3 we can observe that $S_5 = \overline{S_4}$ and $S_0 = 1$. The number of inputs for the Swallow counter can be reduced to four by inverting S_5 to obtain S_4 and forcing

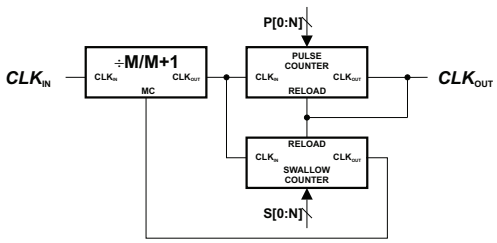


Fig. 16. Block diagram of programmable frequency divider.

Decimal	S_5	S_4	S_3	S_2	S_1	S_0	Division Ratio
25	0	1	1	0	0	1	2681
27	0	1	1	0	1	1	2683
29	0	1	1	1	0	1	2685
31	0	1	1	1	1	1	2687
33	1	0	0	0	0	1	2689
35	1	0	0	0	1	1	2691
37	1	0	0	1	0	1	2693
39	1	0	0	1	1	1	2695
41	1	0	1	0	0	1	2697
43	1	0	1	0	1	1	2699

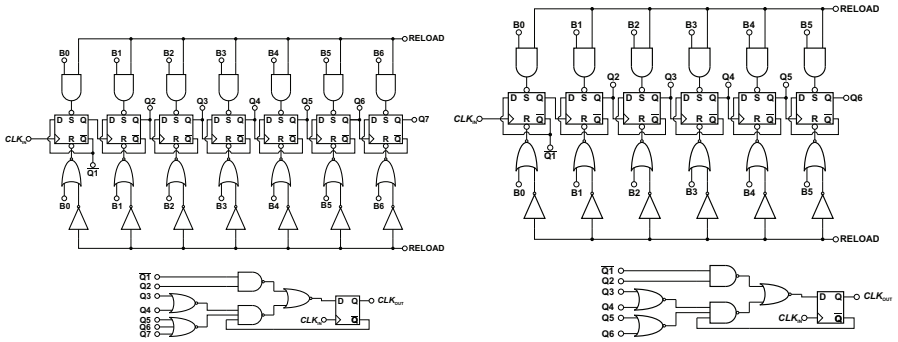
Table 3. Control bits for the swallow counter.

the state of S_0 to a logic 1. The gate-level diagrams of the 7-bit pulse counter, the 6-bit swallow counter and divide-by-32/33 DMP are shown below.

5.2 Results

The divide-by-32/33 dual modulus prescaler in Fig. 18 was implemented Using subthreshold source-coupled logic gates. Since clear and preset functionality were not needed for the DMP, the conventional SCL D-latch was used, and the load resistors were replaced with the PMOS load device proposed in (Tajalli et al., 2008). The divide-by-32 and divide-by-33 operations were simulated using a 990 MHz input signal, and the results are shown in Fig. 19. As shown in the figure the divider output frequency is 30.9375 MHz when dividing by 32, and 30 MHz when dividing by 33.

Transient simulations of the 6-bit and 7-bit programmable counters were performed to verify the desired behaviour of the down counters. Since clear and preset functionality were necessary for correct operation of the programmable counters, the D-latch proposed in Section 4was used. The control word for the 6-bit counter was set to $S[5:0] = S_5S_4S_3S_2S_1S_0 = 011001$, corresponding to a count-down starting from 25. In Fig. 20 the input frequency was 12 MHz and an output pulse was produced from the counter every 25 pulses, resulting in an output frequency of 480 kHz. For the 7-bit counter the control word was $P[6:0] = P_6P_5P_4P_3P_2P_1P_0 =$



(a) Pulse counter. (b) Swallow counter.

Fig. 17. Block diagram of programmable counters.

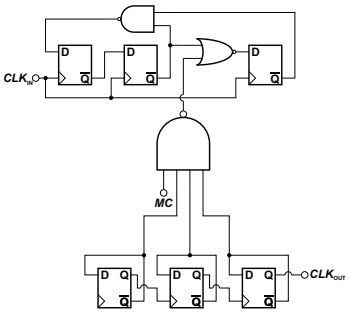
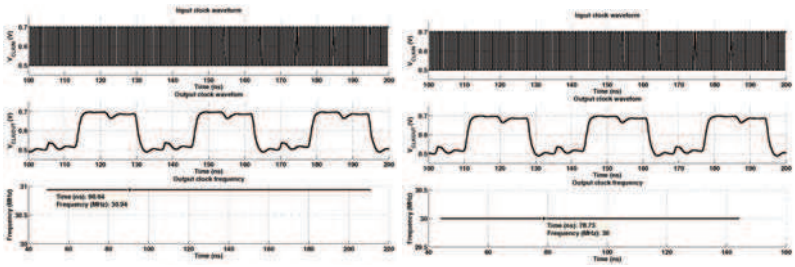


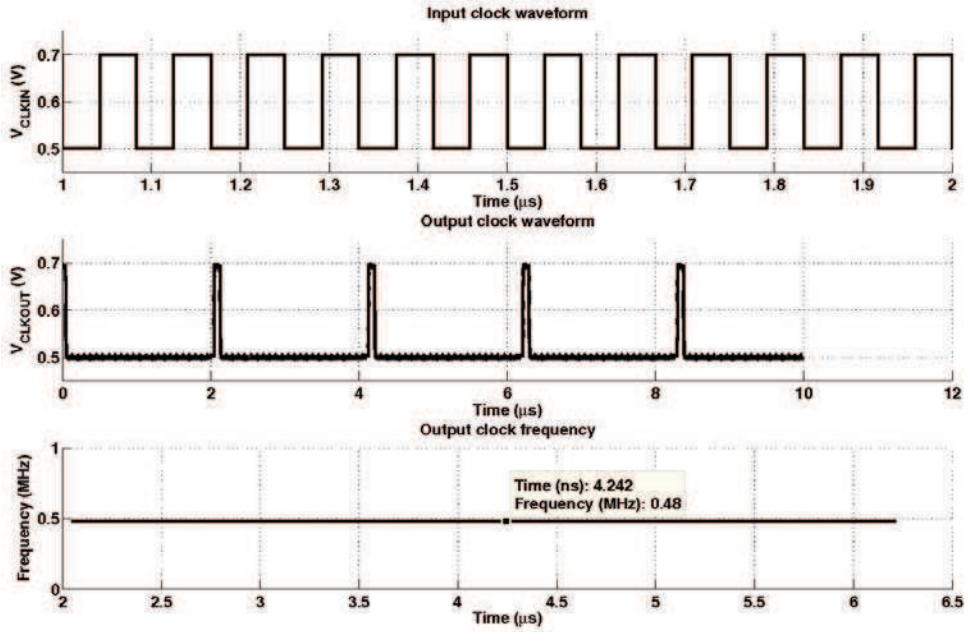
Fig. 18. Block diagram of dual modulus prescaler.

1010011, or 83 in decimal. In Fig. 21 the input frequency was 50 MHz and an output pulse was produced from the counter every 83 pulses, resulting in an output frequency of 602.4 kHz.
Once the major blocks of the proposed programmable divider were simulated, the divider itself was implemented and simulated to ensure it can produce the correct output frequency which would serve as the FB input for the phase/frequency detector. The frequency for each MICS channel was used as the input for the divider, and the control word of the Swallow Counter was adjusted so that the corresponding division ratio was used. It was verified that for each channel, the corresponding division ratio produced an output frequency of 150 kHz. The simulation waveforms in Fig. 22 and Fig. 23 show the input waveform, output waveform and output frequency of the programmable divider when the input frequency is 402.15 MHz (channel 1) and 404.85 MHz (channel 10) respectively.
A comparison between the proposed subthreshold programmable divider and recently published programmable dividers is given in Table 4. The figure of merit used to compare the results is the power consumption at the operating frequency, given in μW/MHz.
The programmable divider was submitted for fabrication as part of an MICS band frequency synthesizer. The layout of the programmable divider is shown in Fig. 24. Measurement results were not available as the design was still being fabricated. The total simulated power consumption of the proposed programmable divider was 200 μW. A summary of the power consumption for each of the major blocks is given in Table 5.



(a) Divide by 32. (b) Divide by 33.

Fig. 19. Transient simulation of dual-modulus prescaler.

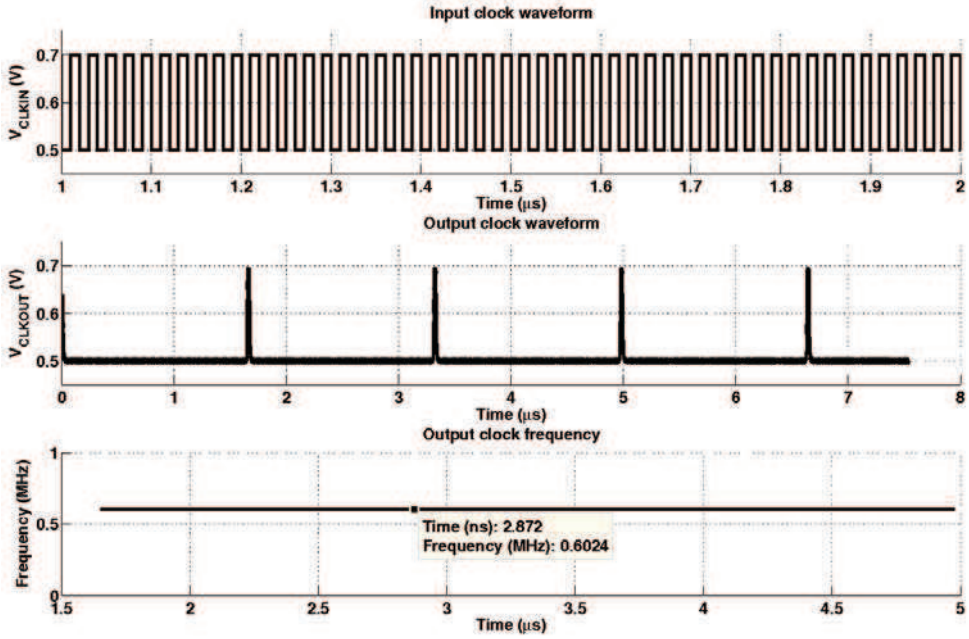


(a) Input and output waveforms.

Fig. 20. Transient simulation of 6-bit down counter.

Reference (Technology)	Frequency [MHz]	V_{DD} [V]	Power [mW]	FOM [μW/MHz]
This Work (0.13μm)	**200 to 1000**	**0.7**	**0.21**	**0.247**
(Kuo & Wu, 2006) (0.18μm)	2400 and 5000	1.8	2.6	1.08
(Kuo & Weng, 2009) (0.18μm)	5141 to 5860	1.5	4.8	0.934
(Lei et al., 2009) (0.18μm)	500 to 3500	1.8	3.01	0.86
(Pan et al., 2008) (0.18μm)	1600	1.2	0.475	0.296
(Kim et al., 2008) (0.18μm)	3000	1.5	3.58	1.19
(Zhang et al., 2009) (0.18μm)	1700	1.5	3.2	1.88
(Zhang et al., 2006) (0.18μm)	440	1.8	0.54	1.23

Table 4. Comparison of low power programmable dividers



(a) Input and output waveforms.

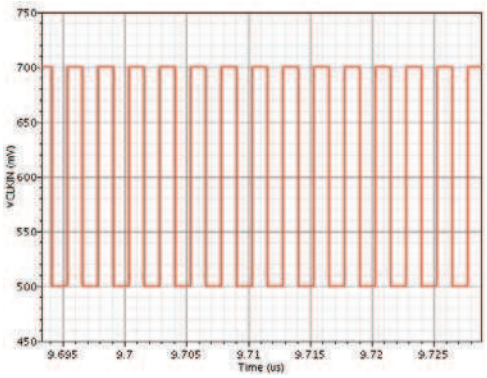
Fig. 21. Transient simulation of 7-bit down counter.

6. A subthreshold source-coupled logic phase/frequency detector, current-steering charge pump, and loop filter

The phase/frequency detector (PFD) uses the architecture of Fig. 25(a). The proposed D-latch with clear preset is used to implement the master-slave D flip-flops in the PFD. The outputs of the 2-input SCL AND/NAND gate drives the EN and $\overline{EN}$ signals in the proposed D-latch. In order to perform the required function, the CLR signal is tied to the positive supply and the PRE signal is tied to the negative supply. The block diagram of the PDF is shown in Fig. 25(b) The charge-pump used in this work is a modification of the low voltage charge pump circuit proposed in (Chang & Kuo, 2000) shown in Fig. 26.

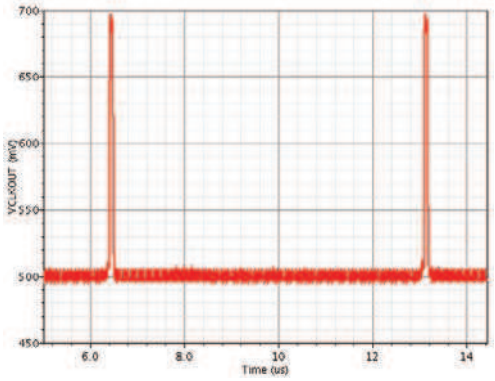
Block	Power consumption [μW]
Dual modulus prescaler	30
6-bit programmable counter	76
7-bit programmable counter	89
Pulse-swallow programmable divider	200

Table 5. Power consumption of programmable divider components.

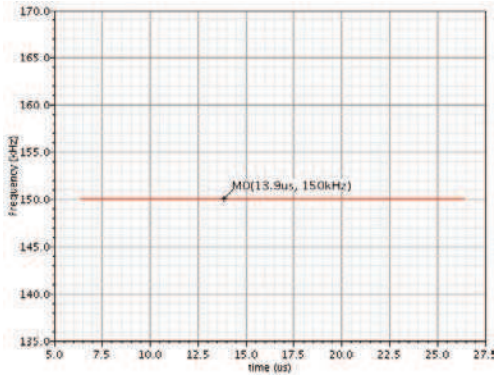


p!]

(a) Input voltage waveform

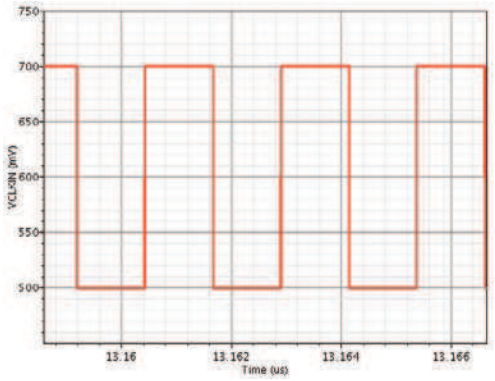


(b) Output voltage waveform

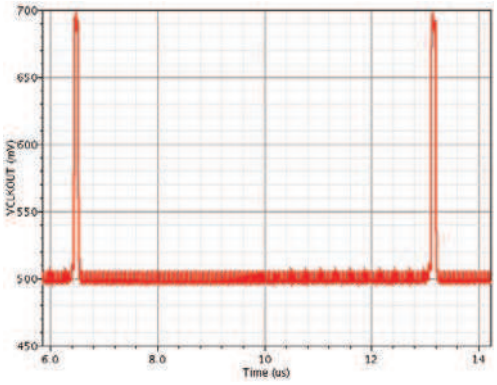


(c) Output frequency

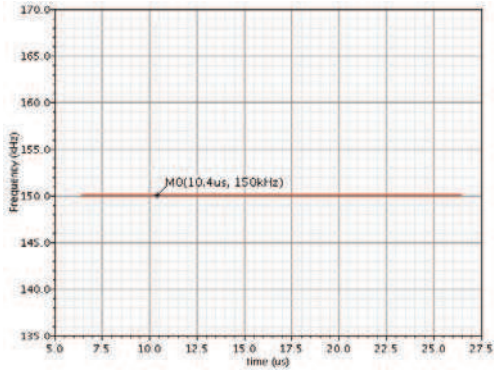
Fig. 22. Programmable divider output when f_{in} = 402.15 MHz



(a) Input voltage waveform



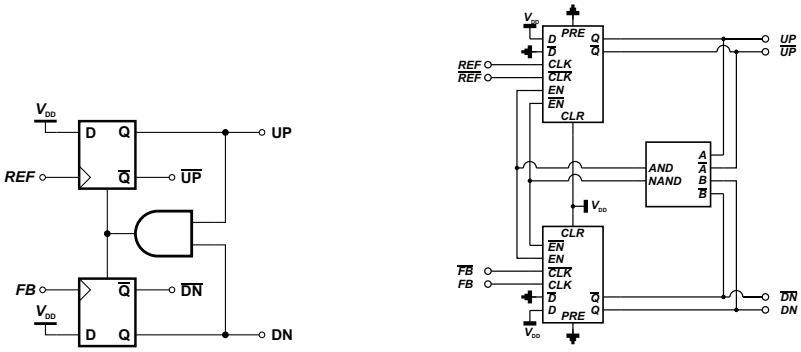
(b) Output voltage waveform



(c) Output frequency

Fig. 23. Programmable divider output when f_{in} = 404.85 MHz

Fig. 24. Programmable frequency divider layout.



(a) Conventional architecture. (b) Adapted architecture.

Fig. 25. Phase/frequency detector.

The circuit consists of a wide-swing current mirror and symmetric charge pumps to provide I_{UP} and I_{DN}. Each charge pump is controlled by a differential input pair biased with a tail current source, a current mirror load and a diode connected load. In the "pump up" circuit, when UP is high the bias current flows through M_1 and is mirrored to the output through the current mirror $M_{5,16}$. A pull-up transistor M_9 is added to immediately bring the gate of the current mirror transistors to V_{DD} when UP is low in order to shut off the current mirror and prevent any current from leaking into the output. The "pump down" circuit can be analysed in the same fashion. The wide-swing current mirror M_{11-14} mirrors the pump down current to the output of the charge pump. The loop filter is a 3rd order passive filter and the components were chosen to have a loop bandwidth of approximately 15 kHz to reduce reference spurs.

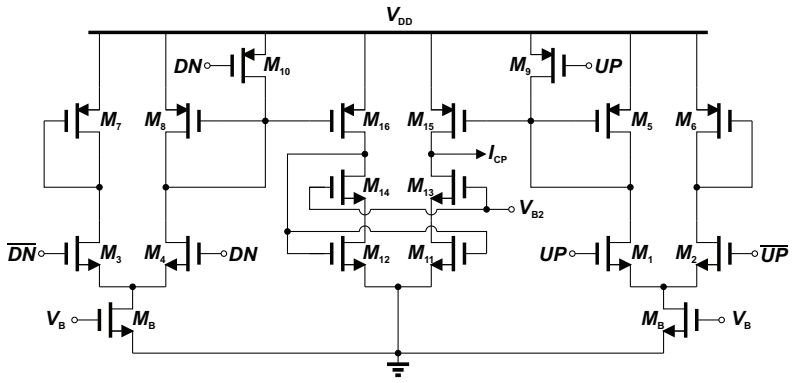
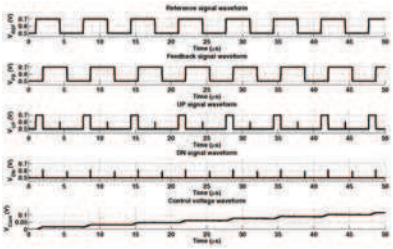
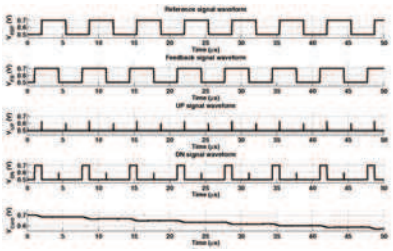


Fig. 26. Current-steering charge pump.



(a) Reference leads feedback.



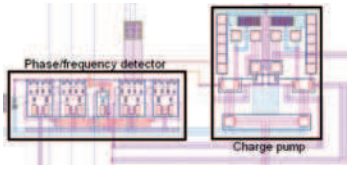
(b) Reference lags feedback.

Fig. 27. Transient simulation of PFD/CP/LF.

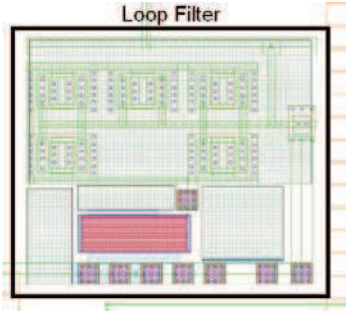
The simulation results of the proposed subthreshold source-coupled logic phase/frequency detector, current-steering charge pump and loop filter are presented in Fig. 27. In Fig. 27(a), the reference signal phase leads the feedback signal phase and the control voltage increases as expected. Similarly in Fig. 27(b), the reference signal phase lags the feedback signal phase and the control voltage decreases. It should be noted that an initial voltage was placed on the loop filter capacitor for the simulation in Fig. 27(b) because when the simulator starts the initial control voltage would be zero and the charge pump cannot remove any more charge from the capacitor.
The PFD/CP/LF was submitted for fabrication as part of the previously mentioned MICS band frequency synthesizer, and measurement results are not currently available. The layout of the PFD/CP/LF is shown in Fig. 28. The CP was designed to have I_{UP}=I_{DN}=1 μA. The entire PFD/CP/LF consumes under 20 μW of power, most of which is consumed by the PFD.

7. The proposed ultra-low power integer-n frequency synthesizer

Using the proposed proposed CR-QVCO, subthreshold SCL programmable frequency divider and PFD implemented using the proposed clear/preset D latch, the modified current-steering charge pump and third order loop filter, a 402 MHz to 405 MHz integer-n frequency synthesizer was implemented.



(a) Phase/frequency detector and charge pump.



(b) Loop filter.

Fig. 28. Phase/frequency detector, charge pump and loop filter layouts.

Block	Power consumption [μW]
Current-reuse quadrature voltage-controlled oscillator	420
Pulse-swallow programmable divider	200
Charge pump, phase/frequency detector and loop filter	20
Total	640

Table 6. Power consumption of programmable divider components.

7.1 Results

The frequency synthesizer in Fig. 1 was simulated to verify the locking behaviour, and simulation results show that the synthesizer reaches the lock stated in 250 μs. The total power consumption is 700 μW. A summary of the power consumption for all the blocks of the proposed frequency synthesizer is presented in Table 6.

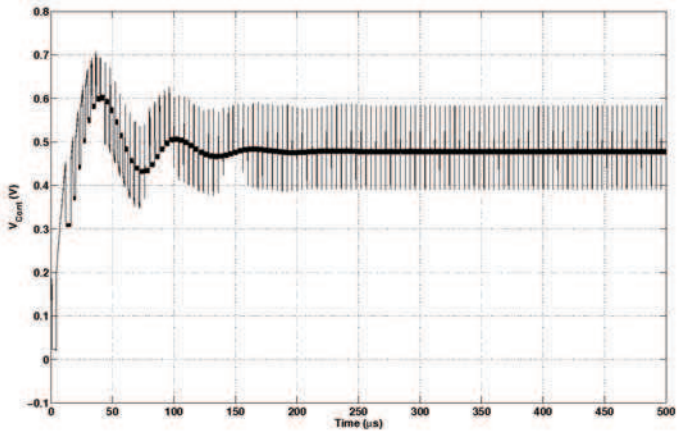


Fig. 29. Frequency synthesizer control voltage.

The chip layout of the entire subthreshold integer-n frequency divider is shown in Fig. 30. The total silicon area including probe pads is 2 mm $\times$ 1.5 mm. At the time of publication, the synthesizer was still in fabrication thus measurement results were not available.

8. Conclusion

In this research, novel circuits and design methodologies were presented for the design and implementation of an ultra-low power integer-n frequency synthesizer operating in the 402 MHz to 405 MHz Medical Implant Communication Service band of frequencies. The principal design concepts to achieve ultra-low power operation were introduced, namely current reuse, supply voltage scaling and subthreshold operation. Using these techniques, several novel circuits for use in the ultra-low power integer-n frequency synthesizer were proposed, namely:

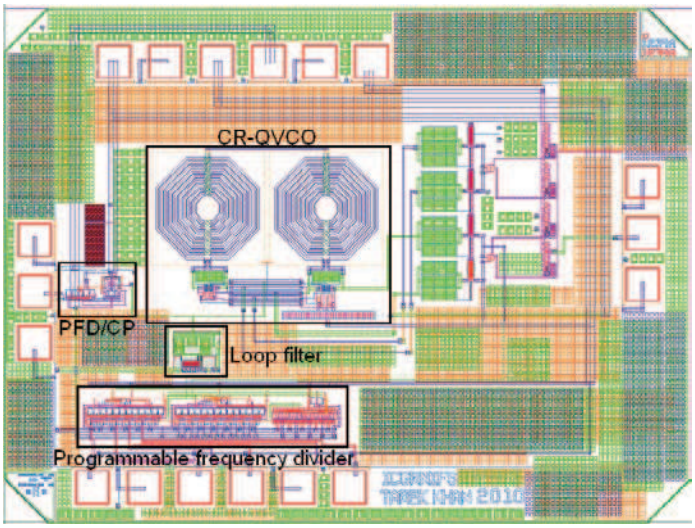


Fig. 30. Frequency synthesizer layout.

- A current reuse quadrature voltage-controlled oscillator.
- A novel clear/preset SCL D-latch.
- A subthreshold SCL programmable divider and phase/frequency detector based on the proposed clear/preset SCL D-latch.

Using IBM CMRF8SF 130 nm CMOS technology, the proposed circuits were used to implement an integer-n frequency synthesizer. Simulations and preliminary silicon measurements confirmed that the proposed CR-QVCO, ST-SCL programmable divider and ultra-low power frequency synthesizer achieve better performance than existing designs.

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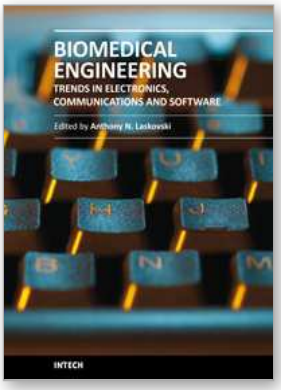

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Rapid technological developments in the last century have brought the field of biomedical engineering into a totally new realm. Breakthroughs in materials science, imaging, electronics and, more recently, the information age have improved our understanding of the human body. As a result, the field of biomedical engineering is thriving, with innovations that aim to improve the quality and reduce the cost of medical care. This book is the first in a series of three that will present recent trends in biomedical engineering, with a particular focus on applications in electronics and communications. More specifically: wireless monitoring, sensors, medical imaging and the management of medical information are covered, among other subjects.

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