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3-D Quantum Numerical Simulation of Transient Response in Multiple-Gate Nanowire MOSFETs Submitted to Heavy Ion Irradiation

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1. Introduction

The bulk MOSFET scaling has recently encountered significant limitations, mainly related to the gate oxide (SiO_2) leakage currents (Gusev et al., 2006; Taur et al., 1997), the large increase of parasitic short channel effects and the dramatic mobility reduction (Fischetti & Laux, 2001) due to highly doped Silicon substrates precisely used to reduce these short channel effects. Technological solutions have been proposed in order to continue to use the "bulk solution" until the 32 nm ITRS node (ITRS, 2009). Most of these solutions envisage the introduction of high-permittivity gate dielectric stacks (to reduce the gate leakage, (Gusev et al., 2006; Houssa, 2004), midgap metal gate (to suppress the Silicon gate polydepletion-induced parasitic capacitances) and strained Silicon channel (to increase carrier mobility (Rim et al., 1998). However, in parallel to these efforts, alternative solutions to replace the conventional bulk MOSFET architecture have been proposed and studied in the recent literature. These options are numerous and can be classified in general according to three main directions: (i) the use of new materials in the continuity of the "bulk solution", allowing increasing MOSFET performances due to their dielectric properties (permittivity), electrostatic immunity (SOI materials), mechanical (strain), or transport (mobility) properties; (ii) the complete change of the device architecture (e.g. Multiple-Gate devices, Silicon nanowires MOSFET) allowing better electrostatic control, and, as a result, intrinsic channels with higher mobilities and currents; (iii) the exploitation of certain new physical phenomena that appear at the nanometer scale, such as quantum transport, substrate orientation or modifications of the material band structure in devices/wires with nanometer dimensions (Haensch et al., 2006; Hiramoto et al., 2006).

Multiple-Gate nanowire MOS transistors (Fig. 1) are now widely recognized as one of the most promising solutions for meeting the roadmap requirements in the deca-nanometer scale (Park & Colinge, 2002). A wide variety of architectures, including planar Double-Gate (DG) (Frank et al., 1992; Harrison et al, 2004), Vertical Double-Gate, Triple-Gate (Tri-gate) (Guarini et al., 2001; Park & Colinge, 2002), FinFET (Choi et al., 2001; Kedzierski et al., 2002), Omega-Gate (Ω -Gate) (Park et al., 2001), Pi-Gate (π -Gate) (Yang et al., 2002), Δ-channel SOI MOSFET (Jiao & Salama, 2001), DELTA transistor (Hisamoto et al., 1989), Gate-All-Around (GAA) (Colinge et al., 1990; Park & Colinge, 2002), Rectangular or Cylindrical nanowires

(Jimenez et al., 2004), has been proposed in the literature. These structures exhibit a superior control of short channel effects resulting from an enhanced electrostatic coupling between the conduction channel and the surrounding gate electrode. It has been shown that the electrostatic control is enhanced when increasing the "Equivalent Number of Gates" (EGN) from 2 (for Double-Gate devices, Fig. 1) to 4 (for Gate-All-Around devices where the gate electrode is wrapped around the entire channel, Fig. 1) (Bescond et al., 2004).

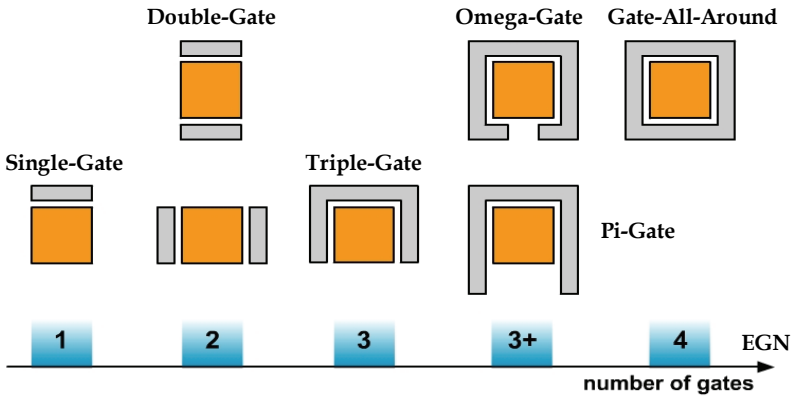

Fig. 1. Schematic cross-sections of the Multiple-Gate devices classified as a function of the "Equivalent Number of Gates" (EGN)

The scaling of Multiple-Gate MOSFET requires the use of an increasingly thinner Silicon film, for which new phenomena have to be taken into account, such as quantum-mechanical confinement. These phenomena induce a strong subband splitting and the carrier confinement in the narrow potential well formed by the Silicon film (Taur & Ning, 1998). Quantum effects sensibly modify the three dimensional (3-D) carrier distribution in the channel, the most important effect being the shift of the charge centroid away from the interfaces into the Silicon film. The inversion charge and then the drain current are reduced in the quantum case with respect to the "classical" case (i.e. without quantum effects). Quantum-mechanical confinement is stronger when the film is thinner. It has been shown that the energy quantization becomes important for channels below 10 nm thick, for which it becomes mandatory to take into account quantum effects in the device simulation (Bescond et al., 2004). In Single-Gate or Double-Gate configurations the carriers are confined in a single direction (vertically, perpendicular to the gate electrode and to the source-to-drain axis). In multiple-gate architectures, and especially in Gate-All-Around devices, the quantum-mechanical confinement is stronger because the carrier energy is quantified in two directions (vertically but also horizontally, in both directions perpendicular to the gates electrodes and to the source-to-drain axis). Then, the carrier confinement and its effects (such as the reduction of the total inversion charge) are stronger in Multiple-Gate devices with EGN≥3 than for single-gate or double-gate architectures.

As the MOSFET is scaling down, the sensitivity of integrated circuits to radiation, coming from the natural space or present in the terrestrial environment, has been found to seriously increase (Baumann, 2005; Dodd, 1996; Dodd & Massengill, 2003; Dodd, 2005). In particular, ultra-scaled memory ICs are more sensitive to single-event-upset (SEU) and digital devices

are more subjected to digital single-event transient (DSETs). Single-event-effects (SEE) are the result of the interaction of highly energetic particles, such as protons, alpha particles, or heavy ions, with sensitive regions of a microelectronic device or circuit. These SEE may perturb the device/circuit operation (e.g., reverse or flip the data state of a memory cell, latch, flip-flop, etc.) or definitively damage the circuit (e.g. gate oxide rupture, destructive latch-up events).

Modeling and simulating the effects of ionizing radiation has long been used for better understanding the radiation effects on the operation of devices and circuits. In the last two decades, due to substantial progress in simulation codes and computer performances which reduce computation times, simulation reached an increased interest. Due to its predictive capability, simulation offers the possibility to reduce radiation experiments and to test hypothetical devices or conditions, which are not feasible (or not easily measurable) by experiments. Physically-based numerical simulation at device-level presently becomes an indispensable tool for the analysis of new phenomena specific to short-channel devices (non-stationary effects, quantum confinement, quantum transport), and for the study of radiation effects in new device architectures (such as multiple-gate, Silicon nanowire MOSFET), for which experimental investigation is still limited. In these cases, numerical simulation is an ideal investigation tool for providing physical insights and predicting the operation of future devices expected for the end of the roadmap. A complete description of the modeling and simulation of SEE, including the history and the evolution of this research domain, have been presented in the reference survey papers by Dodd (Dodd, 1996; Dodd & Massengill, 2003; Dodd, 2005) and Baumann (Baumann, 2005).

In a previous work (Munteanu et al., 2006), we investigated the impact of the quantum effects on the transient response of 50 nm gate length Fully-Depleted (FD) Single-Gate MOSFET with 11 nm thick Silicon film. In that work, we found an excellent agreement between experimental bipolar gain values (measured by heavy ions experiments) and simulated bipolar gain obtained by quantum-mechanical simulation. The results were also consistent with experimental data obtained by pulsed laser irradiation performed on 50 nm gate length transistors fabricated with the same technology (Ferlet-Cavrois et al., 2005). The study presented in (Munteanu et al., 2006) illustrated the importance of taking into account quantum effects in the simulation of the device response when submitted to heavy ion irradiation. The simulation results also showed that even if the impact of quantum effects can be considered as limited in these 11 nm thick FD Single-Gate devices, it will become important for thinner films and for double-gate architectures.

The transient response of Multiple-Gate nanowire MOSFETs under heavy ion irradiation has been already addressed (Castellani et al., 2006; Francis et al., 1995), but to the best of our knowledge, all the previous studies considered the "classical" approach. In this work we use 3D quantum numerical simulation for investigating the drain current transient produced by the ion strike in Multiple-gate nanowire MOSFETs with ultra-thin channels (≤ 10 nm). We firstly consider devices with a gate length of 32 nm and 10 nm-thick Silicon film. For these devices we compare the classical and quantum simulation in terms of drain current transient induced by the ion strike, carrier density and bipolar amplification. Three different Multiple-Gate configurations are considered: Double-Gate, Triple-Gate and Gate-All-Around. In a second step, the devices scaling is addressed and the impact of the quantum effects is analyzed for two cases: (a) 32 nm gate length devices with thinner film (8 nm and 5 nm) and (b) completely scaled devices with 25 nm gate length (8 nm thick film) and 20 nm gate length (5 nm thick film). For each point the classical and the quantum results are

compared and the differences between the four architectures from the view-point of the devices immunity to heavy ion irradiation are analyzed.
This chapter is organized as follows: section 2 presents a detailed description of simulated devices and section 3 describes the simulation code, including the modelling of quantum confinement effects and the simulation of the effects of an ion strike. Section 4 details the simulation of transient effects in Multiple-Gate MOSFET submitted to heavy-ion irradiation. Static and transient characteristics calculated in both quantum and classical cases are presented and compared. Finally, a detailed study concerns the impact of device scaling on the transient response to radiation effects.

2. Simulated devices

In this work, we simulate square cross-section nanowire Double-Gate, Triple-Gate and Gate-All-Around MOSFETs with 32 nm, 25 nm and 20 nm physical gate lengths. The description of the 3-D architectures considered in the simulation and the definition of their geometrical parameters are represented in Fig. 2.

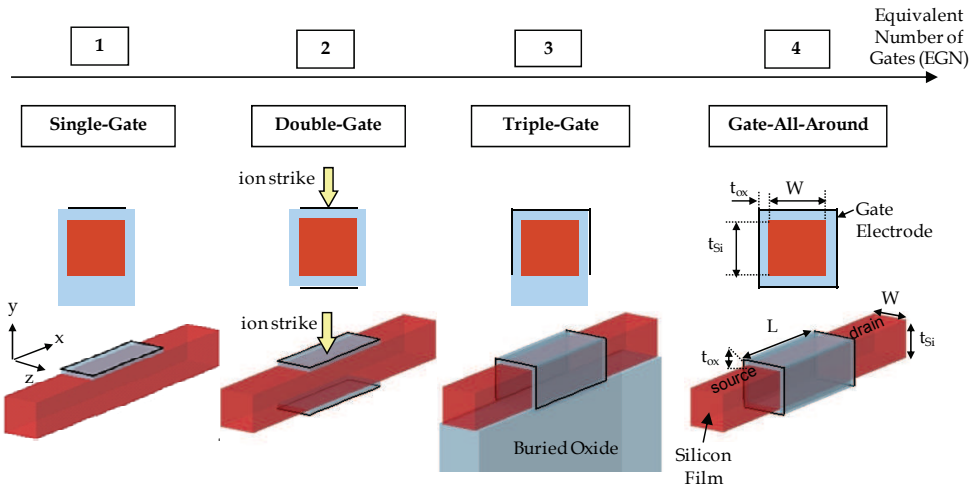

Fig. 2. Schematic description of the 3-D simulated Double-Gate, Triple-Gate and Gate-All-Around structures and their main geometrical parameters considered in this work. The Single-Gate structure is also shown for comparison. The devices are classified as a function of the "Equivalent Number of Gates" (EGN). The schematic cross-sections in the (y-z) plane are also shown. For all the simulated structures, there is no gate overlap with the S/D regions and the S/D doping concentration is $10^{20}cm^{-3}$. The position of the ion strike is also indicated by the arrow; the ion strikes vertically in the middle of the channel (between the source and drain region) and in a direction parallel to the y axis. The Silicon substrate was simulated for the Triple-Gate structures. All structures have Silicon film with square section (t_{Si}=W)

All devices have been calibrated to fill the ITRS requirements for Low Power Technology in terms of drain current in the off-state (I_{OFF}<5×10^{-3} A/μm) (ITRS, 2009). The Silicon film and

the gate oxide have the following dimensions: (a) t_{Si}=W=10 nm and t_{ox}=1.2 nm for devices with L=32 nm gate length, (b) t_{Si}=W=8 nm and t_{ox}=1 nm for devices with L=25 nm and (c) t_{Si}=W=5 nm and t_{ox}=0.9 nm for devices with L=20 nm. All devices have intrinsic channel and mid-gap gate, and the thickness of the buried oxide is 100 nm. The supply voltage is 0.8 V for devices with L=32 nm and L=25 nm and 0.7 V for devices with L=20 nm.

3. Description of the simulation code

3-D numerical simulations have been performed with both 3-D Sentaurus code (Sentaurus, 2009) and with our full quantum homemade Fortran code BALMOS3D (Munteanu & Autran, 2003). The physical models considered in the Sentaurus code include the SRH and Auger recombination models and the Fermi-Dirac carrier statistics.
Concerning the transport modelling, the drift-diffusion (DD) model was for many years the standard level of solid-state device modelling, mainly due to its simple concept and short simulation times. This approach is appropriate for devices with large feature lengths. This model considers that carrier energy does not exceed the thermal energy and carrier mobility is only a local function of the electric field (mobility does not depend on carrier energy). These assumptions are acceptable as long as the electric field changes slowly in the active area, as is the case for long devices (Munteanu & Autran, 2008). When the device feature size is reduced, the electronic transport becomes qualitatively different from the DD model since the average carrier velocity does not depend on the local electric field. In short devices steep variations of electric field take place in the active area of the devices. Then, non-stationary phenomena occur following these rapid spatial or temporal changes of high electric fields. Since these phenomena play an important role in small devices, new advanced transport models become mandatory for accurate transport simulation. The hydrodynamic model, obtained by taking the first three moments of the Boltzmann Transport Equation (BTE), represents the carrier transport effects in short devices more accurately than the DD model. The hydrodynamic model is a macroscopic approximation to the BTE taking into account the relaxation effects of energy and momentum. This model removes several limiting assumptions of DD: the carrier energy can exceed the thermal energy and all physical parameters are energy-dependent (Munteanu & Autran, 2008). In this work we use the hydrodynamic model for the transport modelling. Then, both the impact ionization and the carrier mobility depend on carrier energy calculated with the hydrodynamic model. The mobility model also includes the dependence on the lattice temperature and on the channel doping level. The mobility also depends on the doping level and the lattice temperature. Quantum confinement effects have been considered in the simulation using the Density Gradient model, as explained in section 3.1.

3.1 Modeling of quantum effects

The aggressive scaling-down of bulk MOSFETs in the deep submicrometer domain requires ultrathin oxides and high channel doping levels for minimizing the drastic increase of short channel effects. The direct consequence is a strong increase of the electric field at Si/SiO_2 interface, which creates a sufficiently steep potential well for inducing the quantization of carrier energy (Munteanu & Autran, 2008). In bulk architecture, carriers are then confined in a vertical direction in a quantum well (formed by the Silicon conduction band bending at the interface and the oxide/Silicon conduction band-offset) having feature size close to the electron wavelength. This gives rise to a splitting of the energy levels into subbands (two-

dimensional (2-D) density of states) (Hareland et al., 1998), such that the lowest of the allowed energy levels for electrons (resp. for holes) in the well does not coincide with the bottom of the conduction band (resp. the top of the valence band). In addition, the total density of states in a 2-D system is less than that in a three-dimensional (3-D) (or classical) system, especially for low energies. Carriers occupying the lowest energy levels behave like quantized carriers while those lying at higher energies, which are not as tightly confined in the potential well, can behave like classical (3-D) particles with three degrees of freedom (Munteanu & Autran, 2008). As the surface electric field increases, the system becomes more quantized as more and more carriers become confined in the potential well. The quantum-mechanical confinement considerably modifies the carrier distribution in the channel: the maximum of the inversion charge is shifted away from the interface into the Silicon film (Munteanu & Autran, 2008). Because of the smaller density of states in the 2-D system, the total population of carriers will be smaller for the same Fermi level than in the corresponding 3-D (or classical) case. This phenomenon affects the net sheet charge of carriers in the inversion layer, thus requiring a larger gate voltage in order to populate a 2-D inversion layer to have the same number of carriers as the corresponding 3-D system. This leads to an increase of the threshold voltage of a MOSFET, which is an important issue, especially as the power supply voltages drop to lower levels. The gate capacitance and carrier mobility are also modified by quantum effects. These considerations indicate that the wave nature of electrons and holes can no longer be neglected in ultra-short devices and have to be considered in simulation studies. Quantum confinement becomes also important for the device response to single events.

Various methods have been suggested to model these quantum effects. Among the approaches that are compatible with classical device simulators based on the drift-diffusion (or hydrodynamic) approach, the physically most accurate method is to include the Schrödinger equation into the self-consistent computation of the device characteristics (Stern, 1972). However, solving the Schrödinger equation in itself is very much time-consuming. Various simpler methods have been suggested, such as the Van Dort model or the Hansch model. The van Dort model (van Dort, 1994) expresses the quantum effect by an apparent band edge shift that is a simple function of the electric field. The model is based on the expression for the lowest eigenenergy of a particle in a triangular potential and reproduces the characteristics obtained with the Schrödinger equation quite well. However, this model does not give the correct charge distribution in the device. The Hansch (Hansch et al., 1989] model proposes a quantum correction of the density of states as a function of depth below the Si/SiO_2 interface. The charge distribution is better reproduced, but the model strongly overestimates the impact of quantum effects on the drain current characteristics.

Other alternative to take into account quantum confinement of carriers is the Density-Gradient model (Ancona & Iafrate, 1989; Grubin et al., 1993; Wettstein & al., 2002), coupled with the Drift-Diffusion or the hydrodynamic transport equations. The Density-Gradient model considers a modified equation of the electronic density including an additional term dependent on the gradient of the carrier density. To include quantization effects in a classical device simulation, a simple approach is to introduce an additional potential-like quantity Λ in the classical electron density formula, as follows (Sentaurus, 2009):

$$n = N_C \exp\left(\frac{E_{Fn} - E_C - \Lambda}{kT}\right) \tag{1}$$

where n is the electron density, T is the carrier temperature, k is the Boltzmann constant, N_C is the conduction band density of states, E_C is the conduction band energy, and E_{Fn} is the electron Fermi energy. The impact of the quantum confinement on the carrier density in the device can be taken into account by properly modelling the quantity Λ. For the Density Gradient model, Λ is given in terms of a partial differential equation:

$$\Lambda = -\frac{\gamma\hbar}{6m}\frac{\nabla^2\sqrt{n}}{\sqrt{n}} \tag{2}$$

where ħ = h/2π is the reduced Planck constant, m is the density of states mass, and γ is a fit factor. An equation similar to (1) applies for the holes density. These new equations for electrons and holes density are then used in the self-consistent resolution of the Poisson equation and of the transport equation (Drift-Diffusion or hydrodynamic model), as explained in (Munteanu & Autran, 2008).

3.2 Calibration of the simulation code

It has been shown that the Density Gradient model can accurately account for quantum carrier confinement in Single-Gate SOI and Double-Gate devices with an appropriate calibration step of the fit factor γ (Wettstein & al., 2002). In this work, we have used the exact solution of the Schrödinger –Poisson system of equations (as given by BALMOS3D) for calibrating the Density Gradient model.

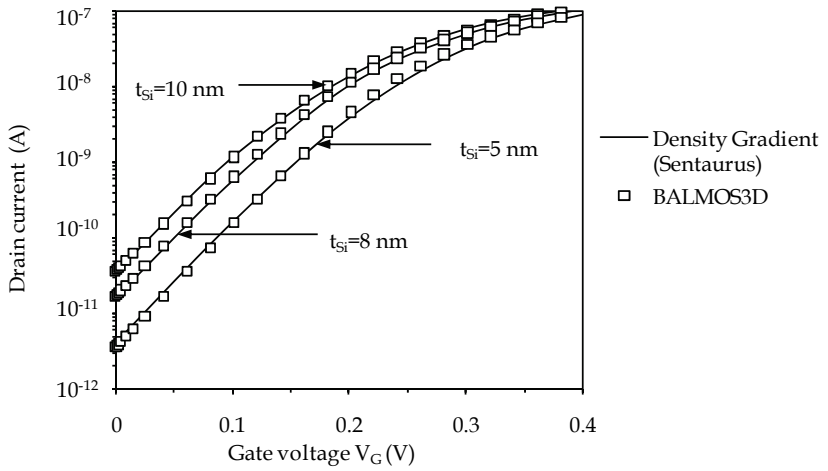

Fig. 3. Calibration of the Density-Gradient model (Sentaurus, 2009) on BALMOS3D. The simulated devices are 32 nm gate length Double-Gate MOSFETs with three Silicon thicknesses (t_{Si}=10 nm, 8 nm and 5 nm). For better illustration, the figure only shows the subthreshold region of the drain current characteristics. V_D=0.8 V

BALMOS3D (Munteanu & Autran, 2003) is a homemade full quantum Fortran simulator, which solves self-consistently the Schrödinger equation and the Poisson equations on a 3-D-grid. The solution of this system of equation is coupled with the Drift-Diffusion transport equation in the channel. A finite difference scheme with a non-uniform mesh has been

considered on a 3-D domain, which includes the channel, the source and drain regions, the gate oxide layers and the gate electrodes. Electric field penetration in the source/drain and electron wave-function penetration in the gate oxide can be also taken into account.
A calibration step of the Density Gradient model on BALMOS3D has been performed on each simulated device, for obtaining the fit factor γ. This factor has different values as a function of the film thickness and gate length. For each particular device, the drain current static characteristics as a function of the gate bias, $I_D(V_G)$, has been computed with BALMOS3D. The same device (with identical geometry) has been implemented in the 3D Sentaurus code and its $I_D(V_G)$ characteristic has been simulated, taken into account the Density Gradient model. The fit factor γ has been then finely tuned in order to obtain a perfect match between the characteristics calculated with BALMOS3D and that simulated by Sentaurus. Figure 3 shows an example of the calibration step on 32 nm gate length Double-Gate MOSFET with three different Silicon film thicknesses.

3.3 Modeling the effect of a particle strike

The physical parameters calibrated previously have been further used in the simulation of drain current transients produced by an ion strike on the sensitive regions of the device. The drain current transients have been simulated in two cases: the classical case (i.e. without quantum effects) and in the quantum case (using Density Gradient model with the fit factor γ as calibrated on BALMOS3D).
The radiation effects have been simulated using the HeavyIon module (Sentaurus, 2009), considering an electron-hole pair column centred on the ion track axis to model the ion strike. The ion track structure to be used as input in simulation is presently a major issue for device simulation. The first representations included a simple cylindrical charge generation with a uniform charge distribution and a constant LET along the ion path. However, the real ion track structure is radial and varies as the particle passes through the matter. When the particle strikes a device, highly energetic primary electrons (called δ-rays) are released. They further generate a very large density of electron-hole pairs in a very short time and a very small volume around the ion trajectory, referred as the ion track. These carriers are collected by both drift and diffusion mechanisms, and are also recombined by different mechanisms of direct recombination (radiative, Auger) in the very dense core track, which strongly reduces the peak carrier concentration. All these mechanisms modify the track distribution both in time and space. As the particle travel through the matter, it loses energy and then the δ-rays become less energetic and the electron-hole pairs are generated closer to the ion path. Then, the incident particle generates characteristic cone-shaped charge plasma in the device (Dodd, 2005).
The real ion track structure has been calculated using Monte-Carlo methods (Hamm et al., 1979; Martin et al., 1987; Oldiges et al., 2000). These simulations highlighted important differences between the track structure of low-energy and high-energy particles, even if the LET is the same (for details see (Dodd et al., 1998; Dodd, 2005)). High-energy particles are representative for ions existing in the real space environment, but they are not available in typical laboratory SEU measurements (Dodd, 1996). Then the investigation of the effects of high-energy particles by simulation represents an interesting opportunity, which may be difficult to achieve experimentally.
Analytical models for ion track structure have been also proposed in the literature and implemented in simulation codes. One of the most interesting models is the "non-uniform

power law" track model, based on the Katz theory (Kobetich & Katz, 1968) and developed by Stapor (Stapor & McDonald, 1988). In this model, the ion track has a radial distribution of excess carriers expressed by a power law distribution and allows the charge density to vary along the track (Dussault et al., 1993). Other analytical models propose constant radius non-uniform track or Gaussian distribution non-uniform track.
In commercial simulation codes, the effect of a particle strike is taken into account as an external generation source of carriers. The electron-hole pair generation induced by the particle strike is included in the continuity equations via an additional generation rate. This radiation-induced generation rate can be connected to the parameters of irradiation, such as the particle Linear Energy Transfer (LET). The LET is the energy lost by unit of length (-dE/dl), which is expressed here in MeV cm²/mg (1pC/μm≈100MeV cm²/mg). The particle LET can be converted into an equivalent number of electron-hole pairs by unit of length using the mean energy necessary to create an electron-hole pair (E_{ehp}) (Roche, 1999):

$$\frac{dN_{ehp}}{dl} = \frac{1}{E_{ehp}} \frac{dE}{dl} \tag{3}$$

where N_{ehp} is the number of electron-hole pairs created by the particle strike. By associating two functions describing the radial and temporal distributions of the created electron-hole pairs, the number of electron-hole pairs is included in the continuity equations (Munteanu & Autran, 2008) via the following radiation-induced generation rate:

$$G(w,l,t) = \frac{dN_{ehp}}{dl}(l) \cdot R(w) \cdot T(t) \tag{4}$$

where R(w) and T(t) are the functions of radial and temporal distributions of the radiation induced pairs, respectively. Equation (4) assumes the following hypothesis: the radial distribution function R(w) depends only on the distance traversed by the particle in the material and the generation of pairs along the ion path follows the same temporal distribution function in any point. Since function G must fill the condition:

$$\int_{w=0}^{\infty} \int_{\theta=0}^{2\pi} \int_{t=-\infty}^{\infty} G\, w\, dw\, d\theta\, dt = \frac{dN_{ehp}}{dl} \tag{5}$$

functions R(w) and T(t) are submitted to the following normalization conditions:

$$2\pi \int_{w=0}^{\infty} R(w)\, w\, dw = 1 \tag{6}$$

$$\int_{t=-\infty}^{\infty} T(t)\, dt = 1 \tag{7}$$

The ion track models available in commercial simulation codes usually propose a Gaussian function for the temporal distribution function T(t):

$$T(t)=\frac{e^{-(\frac{t}{t_C})^2}}{t_C\sqrt{\pi}} \tag{8}$$

where t_C is the characteristic time of the Gaussian function which allows one to adjust the pulse duration. The radial distribution function is usually modelled by an exponential function or by a Gaussian function:

$$R(w)=\frac{e^{-(\frac{w}{r_C})^2}}{\pi r_C^2} \tag{9}$$

where r_C is the characteristic radius of the Gaussian function used to adjust the ion track width. Previous works have demonstrated that the different charge generation distributions used for the radial ion track does affect the device transient response, but the variation is typically limited to ~5% for ion strikes on bulk p-n diodes (Dodd, 2005; Dussault et al., 1993). Considering a LET which is not constant with depth along the path has a more significant impact on the transient response in bulk devices. The key parameters of the single event transient (peak current, time to peak and collected charge) have up to 20% variation when LET is allowed to vary with depth compared to the case of a constant LET (Dussault et al., 1993). Nevertheless, the LET variation with depth has no influence on the transient response of actual SOI devices with thin Silicon film.
In this work, the irradiation track simulated in vertical incidence has a Gaussian shape with narrow radius (14 nm) and a Gaussian time dependence, centred on 10 ps and with a characteristic width of 2 ps. The ion strikes in the middle of the channel. The deposited charge is calculated considering the Gaussian distribution of the ion track and the 3D geometry of the Silicon film. The collected charge is given by the integration of the drain current over the transient duration and the bipolar amplification is finally calculated as the ratio between the collected and deposited charges, as it will be shown in section 4.3.

4. Simulation of multiple-gate devices

4.1 Static characteristics

Figure 4 shows the quantum confinement directions in three different generic configurations: Single-Gate, Double-Gate and Gate-All-Around devices. The impact of quantum effects on the electron density extracted along a cut-line parallel to the confinement directions is also illustrated for the three devices.
In the Single-Gate devices carriers are confined in a very narrow triangular potential well, formed at the Si/SiO_2 interface. The quantum carrier density in the y direction is then modified as compared to the classical one: the classical electron density is maximal at the Si/SiO_2 interface, since the quantum density profile show a maximum shifted inside the Silicon film at several nanometers depth. Then, the electron density near the interface (as well as the total electron charge in the conduction channel) is strongly reduced. In the case of a Double-Gate archtecture, the potential well is rectangular and its dimension is now controlled by the Silicon film thickness, which becomes a key parameter in the quantum effects analysis. Similar to the Single-Gate configuration, the electron density is maximum at

the two interfaces in the classical case. In the quantum case, the density profile has two maxima situated within the Silicon film at several nanometers depth from each interface. Our results are in perfect concordance with (Majkusiak et al., 2002), where quantum effects are simulated using the solution of the 1-D Schrödinger equation. The drain current is splitted in two separate channels, but they are no more located at the interface as in the classical case. Finally, in the Gate-All-Around structure, carriers are confined in a double rectangular potential well (along the y and the z directions), which considerably enhances the quantum confinement effects. The carrier motion is no more free in the z direction (as is the case of the Single-Gate and the Double-Gate devices), but their energy is quantized as in the y direction. Both the gate electrode width (W) and the Silicon film thickness control here the quantum effects. The quantum electron density in the z direction is no more maximal at the interface but has two maxima moved into the Silicon film as for the carrier density in the y direction. Then the total inversion charge is lower than in the Double-Gate configuration.

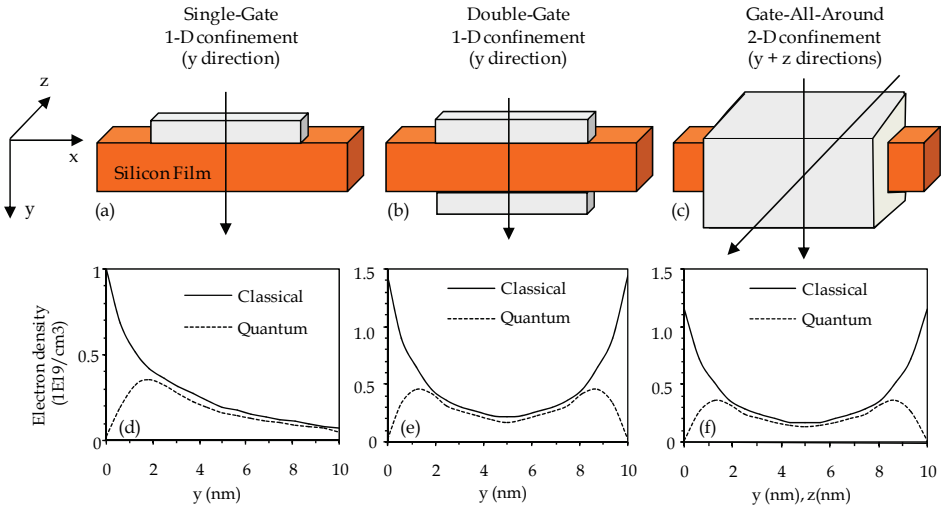

Fig. 4. Schematically representation of the quantum-mechanical confinement directions in (a) Single-Gate, (b) Double-Gate and (c) Gate-All-Around configurations. The profile of the carrier density in a cut-line along the film thickness is also reported for both classical and quantum cases: (d) Single-Gate, (e) Double-Gate and (f) Gate-All-Around. V_D=V_G=0.8 V, L=32 nm

The $I_D(V_G)$ curves for the different 32 nm Multiple-Gate MOSFET architectures simulated in the classical and quantum cases are shown in Fig. 5.

The results show that increasing the "equivalent number of gates" reduces the off-state current (Munteanu et al., 2007) and improves the subthreshold swing S (S = 70 mV/dec for Double-Gate, S = 68.5 mV/dec for Triple-Gate and S = 61.5 mV/dec for Gate-All-Around). This is due to the better electrostatic control of the gate over the channel that reduces short channel effects. At the same time, the on-state current increases with EGN (Fig. 5), due to the multiple-channel conduction. As expected, the quantum current is lower than the classical

one, because the total inversion charge is reduced in the quantum case. Figure 5 also shows that the difference between the classical and the quantum off-state current increases when going from Double-Gate to Gate-All-Around device. The ratio between the classical and quantum off-state currents is reported in Table 1 for the three considered configurations.

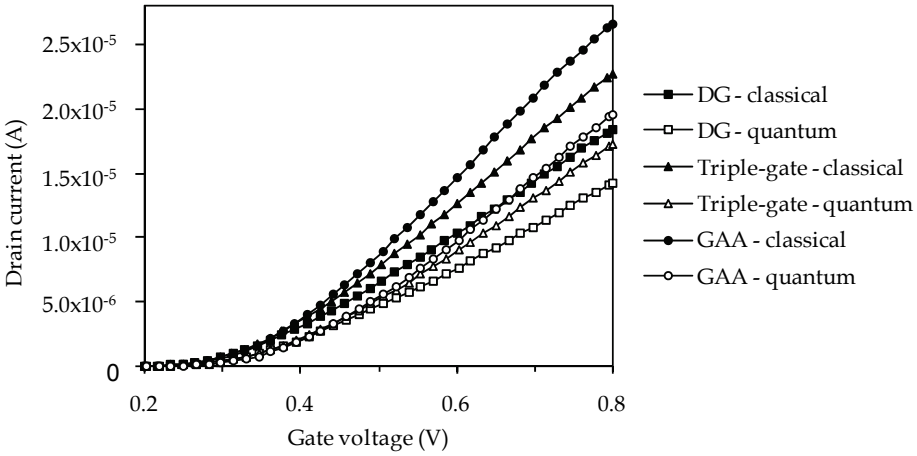

Fig. 5. Drain current $I_D(V_G)$ characteristics in classical and quantum-mechanical cases for 32 nm Double-Gate, Triple-gate, Ω-Gate and Gate-All-Around architectures (V_D=0.8 V). The quantum drain current was simulated using the Density-Gradient model calibrated on BALMOS3D numerical results

	t_{Si}=W=10 nm L=32 nm	t_{Si}=W=8 nm L=25 nm	t_{Si}=W=5 nm L=22 nm
Double-Gate (EGN=2)	1.91	2.02	3.01
Triple-Gate (EGN=3)	2.24	2.3	3.66
Gate-All-Around (EGN=4)	2.36	2.67	4.11

Table 1. Ratio Ioff_cl/Ioff_q of the off-state currents in classical (Ioff_cl) and quantum (Ioff_q) approaches for the three technological nodes studied in this work. The quantum drain current has been calculated using the Density Gradient model calibrated on BALMOS3D for each configuration.

We remark that this ratio increases with EGN for a given technology node. This effect can be explained by the dimensionality of the confinement. In Double-Gate, carriers are confined in one direction (y direction), since in Triple-Gate and Gate-All-Around carriers are confined in two directions (y and z), which strongly enhances the energy quantization with respect to the Double-Gate case.

4.2 Transient simulation results

The time evolution of the electron density distribution in a vertical cross-section (y-z plane) in the middle of the channel is represented in Fig. 6 for three configurations: Double-Gate, Tri-Gate and Gate-All-Around. We observe that for all devices the quantum electron charge is centred in the middle of the film and the electron density has lower values than in the classical case. In off-state bias condition, the carrier conduction in all devices is mainly dominated by the volume inversion phenomenon: carriers flow from source to drain over the entire Silicon film thickness. In consequence, the off-state current is directly proportional to the film thickness. In the quantum case the volume inversion phenomenon is reinforced because the quantum carrier density becomes more centred in the middle of the film (Fig. 6). This effect is enhanced when EGN increases from 2 (Double-Gate) to 4 (Gate-All-Around), as illustrated in Fig. 6.

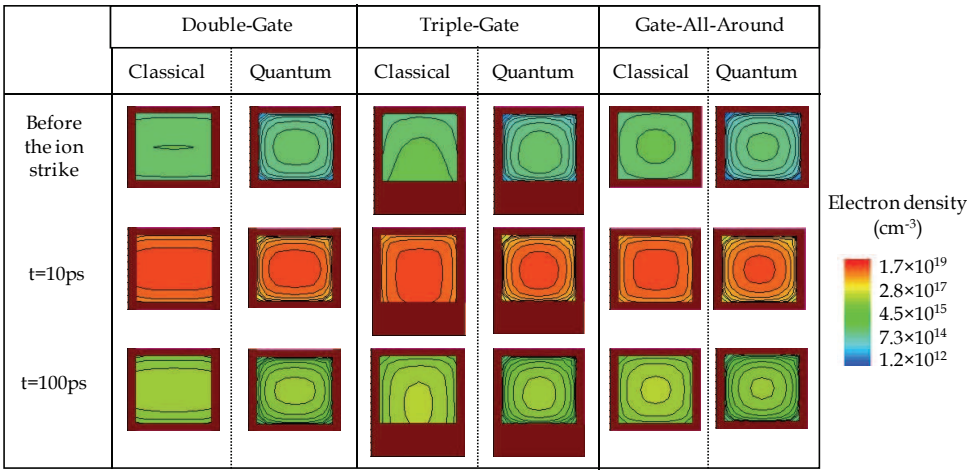

Fig. 6. Classical and quantum electron density (expressed in cm^{-3}) in a vertical cross-section (y-z plane) in the middle of the channel of 32 nm Double-Gate, Triple-Gate and Gate-All-Around at different times before and after the ion strike. The devices are biased in the off-state at V_G=0 V and V_D=0.8 V. The brown regions represent the gate oxide (in Double-Gate and Gate-All-Around devices) and the gate and buried oxide in Triple-Gate devices

The drain current transients produced by the ion strike are illustrated in Fig. 7 for the classical case and for a LET value of 1 MeV/(mg/cm^2). The four configurations corresponding to the 32 nm gate length ITRS LP technology node are simulated in the off-state. The peak value of the drain current transient is reduced when EGN increases. When EGN increases, the channel is better controlled by the gate and the floating body effects are strongly reduced. Then the drain current transient tail is shorter when going from Double-Gate to Gate-All-Around devices. Figure 8 compares the classical and the quantum drain current transient for two configurations: Double-Gate and Gate-All-Around devices with 32 nm gate length. As expected, the peak of the quantum drain current transient is lower than the classical one for both configurations, due to the quantum confinement which induces lower quantum off-state current.

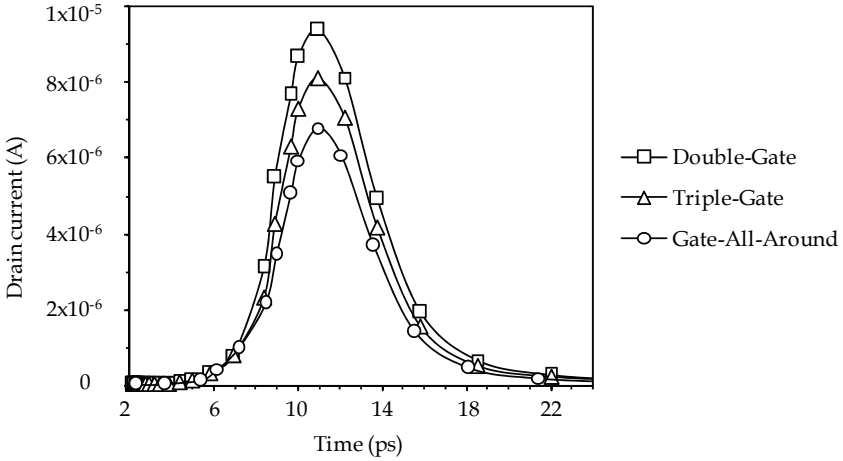

Fig. 7. Drain current transients induced by an ion strike vertically (y direction) in the middle of the Silicon film (classical simulation). The ion track generation has a Gaussian shape versus time (characteristic time of 2 ps), centred at 10 ps and a LET=1 MeV/(mg/cm^2). The simulated devices are 32 nm gate length MOSFETs. All devices are off-state biased (V_G=0 V, V_D=0.8 V)

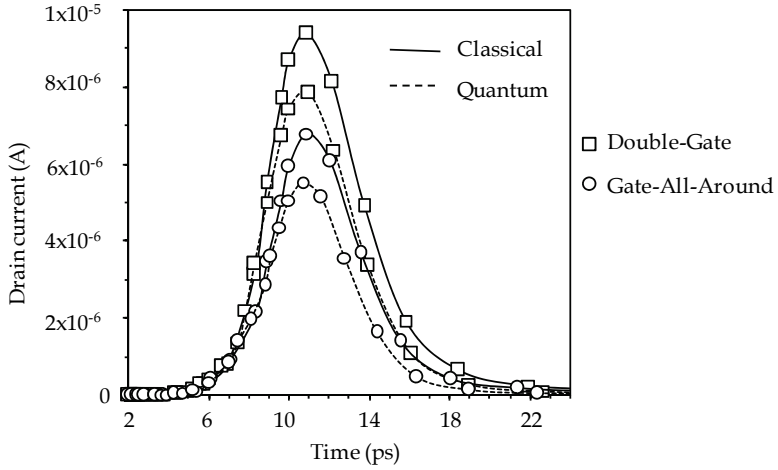

Fig. 8. Drain current transients induced by an ion strike vertically (y direction) in the middle of the Silicon film. Comparison between classical and quantum simulation in Double-Gate and Gate-All-Around MOSFETs. All devices are off-state biased (V_G=0 V, V_D=0.8 V)

4.3 Bipolar amplification

The bipolar amplification is a phenomenon specific to partially-depleted SOI devices and its basic mechanism was largely explained and simulated in previous works (Ferlet-Cavrois et

al., 2002; Ferlet-Cavrois et al., 2004; Schwank et al., 2003). Bipolar amplification can also occur in fully depleted devices, as those studied here.

The bipolar transistor mechanism in fully depleted devices has been explained in (Brisset et al., 1994) using Monte Carlo simulations of 0.25 μm fully depleted SOI transistors: after irradiation of a n-channel MOSFET biased in its off state, excess holes are accumulated in the channel (mainly near the gate oxide) and lower the potential barrier; then electrons diffuse from source to drain to maintain the electrical neutrality. This mechanism is comparable to the bipolar transistor effect in partially depleted SOI transistors (Massengill et al., 1990). Because bipolar amplification is less important for fully depleted than for partially depleted devices, circuits based on fully depleted transistors are less sensitive to single-event upset than partially depleted circuits (Ferlet-Cavrois et al., 2002).

The effect of the parasitic bipolar transistor in SOI devices is quantified using the bipolar gain, β. The bipolar gain corresponds to the amplification of the deposited charge and is given by the ratio between the total collected charge, Q_{coll}, at the drain electrode and the deposited charge, Q_{dep}:

$$\beta = \frac{Q_{coll}}{Q_{dep}} \tag{10}$$

The total collected charge at drain electrode is given by:

$$Q_{coll} = \int_0^{\infty} I_D dt \tag{11}$$

The deposited charge in a SOI device is calculated as a function of the particle LET using the following equation (Ferlet-Cavrois, 2004; Munteanu & Autran, 2008):

$$Q_{dep}[fC] = 10.3 \times LET[MeV/(mg/cm^2)] \times t_{Si}[\mu m] \tag{12}$$

where t_{Si} is the Silicon film thickness and 10.3 is a multiplication factor for Silicon calculated using the Silicon density and the energy needed for creating an electron-hole pair in Silicon (– 3.6 eV) (Ferlet-Cavrois, 2004; Munteanu & Autran, 2008). In this equation a normal incident ion strike is considered and the LET is supposed constant along the ion path in the active Silicon film.

The bipolar gain for 32 nm gate length Multiple-Gate devices in both classical and quantum cases is shown in Fig. 9 as a function of the LET value. The bipolar amplification decreases when increasing EGN due to less floating body effects. However, at high LET (>2 MeV/(mg/cm²)), the classical bipolar gain becomes the same for all configurations. This can be explained by the huge deposited charge by the ion which masks the impact of other phenomena such as the electrostatic control by the gate.

Previous experimental and theoretical studies showed that, generally, fully depleted SOI-based devices (with either single- or double-gate configuration) present reduced floating body effects and then lower bipolar amplification of the collected charge than partially-depleted SOI devices (Ferlet-Cavrois et al., 2002; Ferlet-Cavrois et al., 2005). In Multiple-Gate devices the control of the channel by the gates is naturally reinforced, and reduces even more the floating body effects. Then very low values are obtained for the bipolar gain. Our results are consistent with simulation data from (Munteanu et al., 2006) and (Castellani et

al., 2006), but they are very low compared with those expected by extrapolation from simulations in (Dodd et al., 2004). This is probably due to the partially depleted SOI Single-Gate structures used in (Dodd et al., 2004), whereas ultra-thin fully-depleted devices and multiple-gate configurations are considered here.
The quantum bipolar gain is lower than the classical one, excepted at very high LET (Fig. 9). Our results show that two phenomena, with opposite effects on the bipolar gain, are to be considered. On one hand, the lower off-state current in the quantum case leads to a lower quantum bipolar amplification (Castellani et al., 2006). On the other hand, in the quantum case, the electron density is lower leading to slower recombination process (reflected in a longer transient tail) and then to a higher collected charge. Depending on the injection regime, one phenomenon or the other prevails. At low injection regime, the generated charge is not very high and carriers recombine rapidly. Then the bipolar gain follows the off-state current behaviour, both being lower for a quantum approach than for a classical one. In very high injection conditions, the electron charge in the film is not sufficient to recombine the enormous generated charge and then, the recombination process is sensibly slower. This has been verified by simulation: the recombination rate in the Silicon film is higher in the classical case than in the quantum case. As a consequence, the quantum collected charge and the quantum bipolar amplification are higher than in the classical ones.

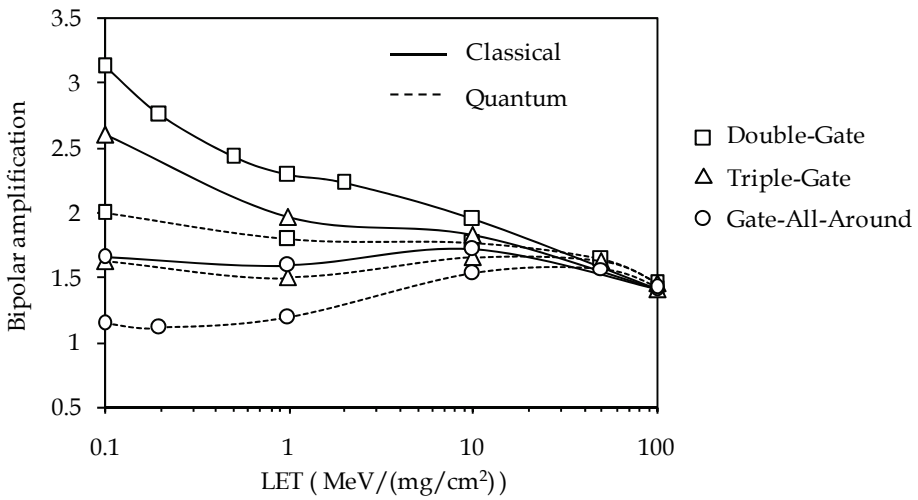

Fig. 9. Simulated classical and quantum bipolar gain as a function of LET in 32 nm gate length Multiple-Gate MOSFET. The transistors are biased in the off-state at V_G=0 V and V_D=0.8 V

5. Device scaling

The effects of the carrier confinement become more important when the Silicon film is thinned because the energy subband splitting is directly proportional with the reverse of the square of the potential well dimension (equal to the film thickness). The ratio between the

classical and quantum off-state currents, reported in Table 1 as a function of t_{Si}, confirms that the quantum confinement is strongly enhanced when the film is thinned down. The collected charge and the bipolar gain (shown in Figs. 10(a) and 10(b)) are lower for thinner channel, in both quantum and classical cases, because the off-state current decreases with the film thickness. The maximal value of the gain is shifted to higher LET values when Silicon film thickness decreases. Our results also indicate that, in the quantum approach, the difference in the bipolar gain when reducing the film thickness (at the same LET) is lower than in the classical case.

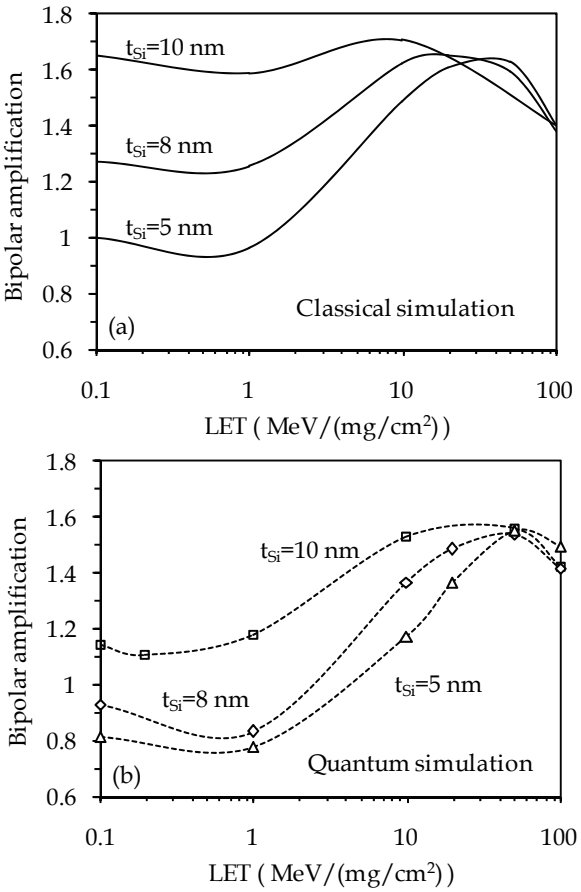

Fig. 10. Bipolar gain variation when reducing the Silicon film thickness in Gate-All-Around MOSFET with 32 nm gate length (the gate width is W=10 nm): (a) classical simulation; (b) quantum simulation. The transistors are biased in the off-state at V_G=0 V and V_D=0.8 V

The quantum bipolar gain for Multiple-Gate devices scaled down to 20 nm gate length and 5 nm Silicon film cross-section was also predicted. As shown in Fig. 11, the difference between the three architectures is reduced for devices with 20 nm gate lengths compared to those with 32 nm and 25 nm gate lengths, due to the very thin square wire cross-section (t_{Si}=W=5

nm). When decreasing the cross-section, the influence of the gate configuration is attenuated and the values of the bipolar gain for the different structures are almost the same. This behaviour can be explained by the fact that, around 5 nm and below, the combination of gate electrostatic control and quantum-mechanical confinement leads to similar carrier density distributions in the film for all gate configurations (Bescond et al., 2004). At this ultimate scale of integration, it should be expected that the sensitivity of all Multiple-Gate nanowire architectures (EGN ≥ 2) to heavy ion irradiation sensibly become equivalent.

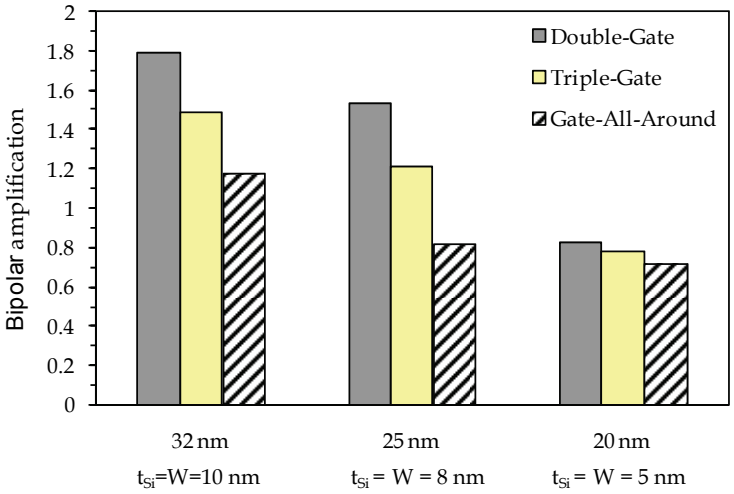

Fig. 11. Bipolar gain calculated in the quantum case for Multiple-Gate nanowire MOSFETs with different gate lengths. The dimensions of the Silicon film cross-section are also indicated. The ion strikes vertically (parallel to the y direction) in the middle of the film

6. Conclusion

In this work we analyzed the impact of quantum confinement on single-event transient immunity of several Multiple-Gate architectures. We showed that the 3-D carrier distribution is strongly affected by the quantum effects, which not only reduces the drain current but also modifies the recombination rate and the charge collection compared to the classical case. Increasing the "number of equivalent gates" induces less floating body effects and then lowers the bipolar gain. Our simulations also showed that when the Silicon channel cross-section is thinned down (around 5nm and below), the bipolar amplification of Multiple-Gate nanowire architectures (EGN ≥ 2) sensibly becomes the same mainly due to carrier quantum confinement.

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This book will interest researchers, scientists, engineers and graduate students in many disciplines, who make use of mathematical modeling and computer simulation. Although it represents only a small sample of the research activity on numerical simulations, the book will certainly serve as a valuable tool for researchers interested in getting involved in this multidisciplinary ï¬eld. It will be useful to encourage further experimental and theoretical researches in the above mentioned areas of numerical simulation.

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