6

The Doherty Power Amplifier

Paolo Colantonio, Franco Giannini, Rocco Giofrè and Luca Piazzon
University of Roma Tor Vergata
Italy

1. Introduction

The Doherty Power Amplifier (DPA) was invented in the far 1936 by W. H. Doherty, at the Bell Telephone Laboratories of Whippany, New Jersey (Doherty, 1936). It was the results of research activities devoted to find a solution to increase the efficiency of the first broadcasting transmitters, based on vacuum tubes. The latter, as it happens in current transistors, deliver maximum efficiency when they achieve their saturation, i.e. when the maximum voltage swing is achieved at their output terminals. Therefore, when the signal to be transmitted is amplitude modulated, the typical single ended power amplifiers achieve their saturation only during modulation peaks, keeping their average efficiency very low. The solution to this issue, proposed by Doherty, was to devise a technique able to increase the output power, while increasing the input power envelope, by simultaneously maintaining a constant saturation level of the tube, and thus a high efficiency. The first DPA realization was based on two tube amplifiers, both biased in Class B and able to deliver tens of kilowatts.

Nowadays, wireless systems are based on solid state technologies and also the required power level, as well as the adopted modulation schemes, are completely different with respect to the first broadcasting transmitters. However, in spite of more than 70th years from its introduction, the DPA actually seems to be the best candidate to realize power amplifier (PA) stage for current and future generations of wireless systems. In fact, the increasing complexity of modulation schemes, used to achieve higher and higher data rate transfer, is requiring PAs able to manage signals with a large time-varying envelope. The resulting peak-to-average power ratio (PAPR) of the involved signals critically affects the achievable average efficiency with traditional PAs. For instance, in the European UMTS standard with W-CDMA modulation, a PAPR of 5-10 dB is typical registered. As schematically reported in Fig. 1, such high values of PAPR imply a great back-off operating condition, dramatically reducing the average efficiency levels attained by using traditional PA solutions.

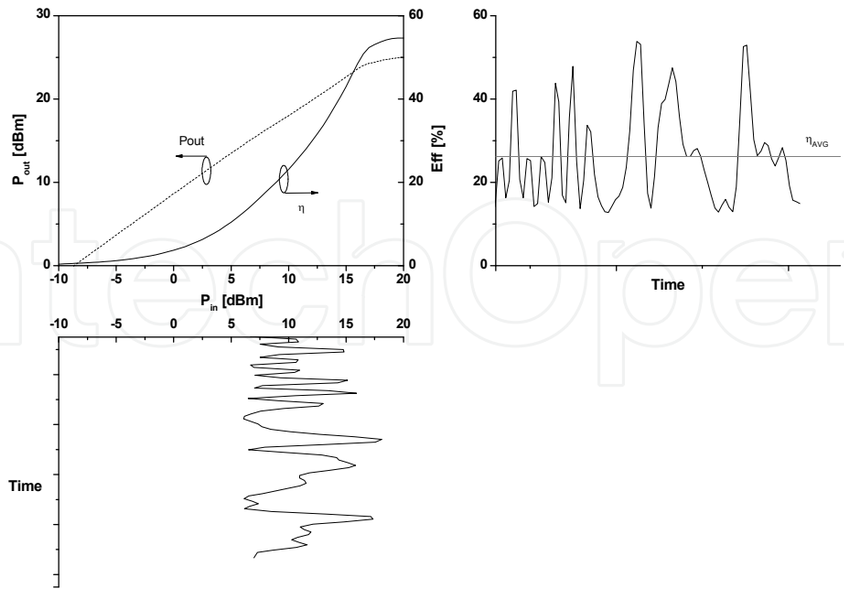

Fig. 1. Average efficiency using traditional PA.

To stress this effect, it is helpful to refer to an ideal Class B PA, which delivers an efficiency of 78.6% at its maximum output power, whereas it becomes only 25% at 10dB back-off. Therefore, when dealing with amplitude modulation signal, it is more useful to refer to the average efficiency, which is defined as the ratio of the average output power ($P_{out,AVG}$) to the average supply DC power ($P_{DC,AVG}$) (Raab, 1986):

$$\eta_{AVG} = \frac{P_{out,AVG}}{P_{DC,AVG}} \tag{1}$$

Clearly, the average efficiency depends on both the PA instantaneous efficiency and the probability density function (*PDF*), i.e. the relative amount of time spent by the input signal envelope at different amplitudes. Therefore, to obtain high average efficiency when time-varying envelope signals are used, the PA should work at the highest efficiency level in a wide range of its output (i.e. input) power. This requirement represents the main feature of the DPA architecture, as shown in Fig. 2, where its theoretical efficiency behavior is reported.
The region with almost constant efficiency identifies the DPA Output Back-Off (OBO) range, and it is fixed according to the PAPR of the signal to be amplified. As will be later detailed, the OBO value represents the first parameter to be chose in the design process.

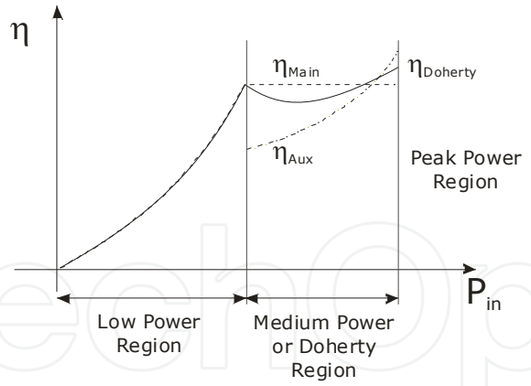

Fig. 2. Typical DPA efficiency behavior versus input power.

Due to this attractive characteristic and the relative simple implementation scheme, the DPA is being the preferred architecture for new communication systems.
The Doherty technique is usually adopted to design PA for wireless systems and, in particular, in base stations, working in L-S-C Band with time-varying envelope signals such as WiMax, WLAN, Cellular network etc. In this field, a lot of experimental results have been published using different active device technologies such as Si LDMOS, GaN HEMT, GaAs PHEMT and GaAs HBT. Typically, these DPAs are realised in hybrid form and they work around 2.14 GHz with W-CDMA input signals. Drain efficiencies up to 70% have been demonstrated for output powers between 5W and 10W (Kim et al., 2008 – Lee et al., 2008 – Markos et al., 2007 – Kim et al., 2005), whereas 50% of drain efficiency has been demonstrated for 250W output power (Steinbeiser et al., 2008). Also for high frequency applications the DPA has been successfully implemented using GaAs MMIC technologies (McCarroll et al., 2000 – Campbell, 1999 – Tsai & Huang, 2007). For instance, in (Tsai & Huang, 2007) it has been reported a fully integrated DPA at millimeter-wave frequency band with 22dBm and 25% of output power and efficiency peak, respectively. Also DPA realizations based on CMOS technology was proposed (Kang et al., 2006 – Elmala et al., 2006 – Wongkomet et al., 2006). However, in this case, due to the high losses related to the realization of required transmission lines, the achieved performances are quite low (peak efficiency lower than 15%).
In this chapter the theory and the design guidelines of the DPA will be reviewed in deep detail with the aim to show to the reader the proper way to design a DPA.

2. The Doherty operating principle

The DPA operating principle is based on the idea to modulate the load of the active device, namely Main (or Carrier) typically biased in Class AB, exploiting the active load pull concept (Cripps, 2002), by using a second active device, namely Auxiliary (or Peaking), usually biased in Class C.
In order to understand the active load-pull concept, it is possible to consider the schematic reported in Fig. 3, where two current sources are shunt connected to an impedance Z_L.

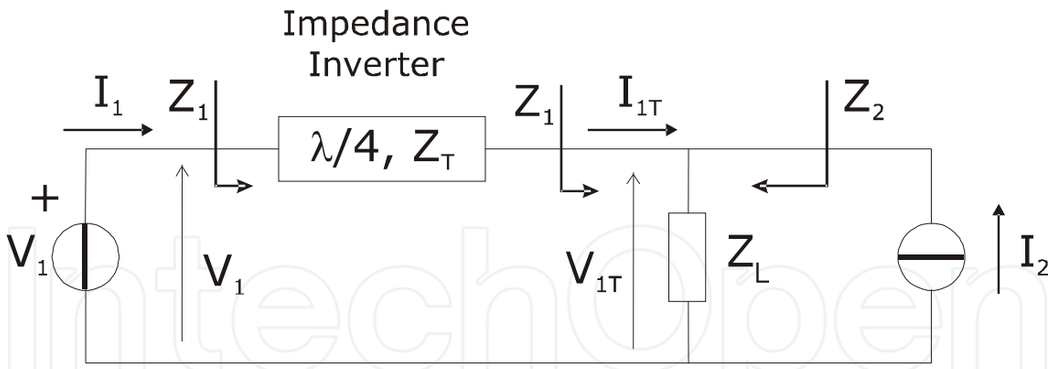

Fig. 3. Schematic of the active load-pull.

Appling Kirchhoff law, the voltage across the generic loading impedance Z_L is given by:

$$V_L = Z_L \left(I_1 + I_2 \right) \tag{2}$$

Where I_1 and I_2 are the currents supplied by source 1 and 2, respectively. Therefore, if both currents are different from zero, the load seen by each current source is given by:

$$Z_1 = Z_L \cdot \left(1 + \frac{I_2}{I_1} \right) \tag{3}$$

$$Z_2 = Z_L \cdot \left(1 + \frac{I_1}{I_2} \right) \tag{4}$$

Thus, the actual impedance seen by one current source is dependent from the current supplied by the other one.
In particular, if I_2 is in phase with I_1, Z_L will be transformed in a higher impedance Z_1 at the source 1 terminals. Conversely, if I_2 is opposite in phase with I_1, Z_L will be transformed in a lower impedance Z_1. However, in both cases also the voltage across Z_L changes becoming higher in the former and lower in the latter situation.
Replacing the current sources with two equivalent transconductance sources, representing two separate RF transistors (Main and Auxiliary respectively), it is easy to understand that to maximize the efficiency of one device (i.e. Main) while its output load is changing (by the current supplied by the Auxiliary device), the voltage swing across it has to be maintained constant. In order to guarantee such constrain, it is necessary to interpose an Impedance Inverting Network (IIN) between the load (Z_L) and the Main source, as reported in Fig. 4.
In this way, the constant voltage value V_1 at the Main terminals will be transformed in a constant current value I_{1T} at the other IIN terminals, independently from the value of Z_L.

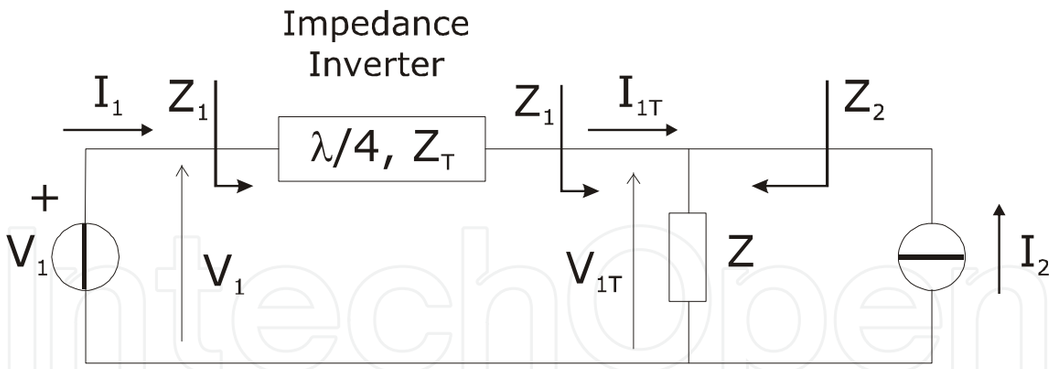

Fig. 4. Simplified schema of the DPA.

For the IIN implementations, several design solutions could be adopted (Cripps, 2002). The most typical implementation is through a lambda quarter transmission line (λ/4 TL), which ABCD matrix is given by:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} 0 & j \cdot Z_0 \\ \frac{j}{Z_0} & 0 \end{pmatrix} \cdot \begin{pmatrix} V_2 \\ I_2 \end{pmatrix} \tag{5}$$

being Z_0 the characteristic impedance of the line.
From (5) it is evident that the voltage at one side (V_1) is dependent only on the current at the other side (I_2) through Z_0, but it is independent from the output load (Z_L) in which the current I_2 is flowing.
Thus, actual DPAs are implemented following the scheme reported in Fig. 5, which is composed by two active devices, one IIN connected at the output of the Main branch, one Phase Compensation Network (PCN) connected at the input of the Auxiliary device and by an input power splitter besides the output load (R_L). The role of the PCN is to allow the in phase sum on R_L of the signals arising from the two active devices, while the splitter is required to divide in a proper way the input signal to the device gates.

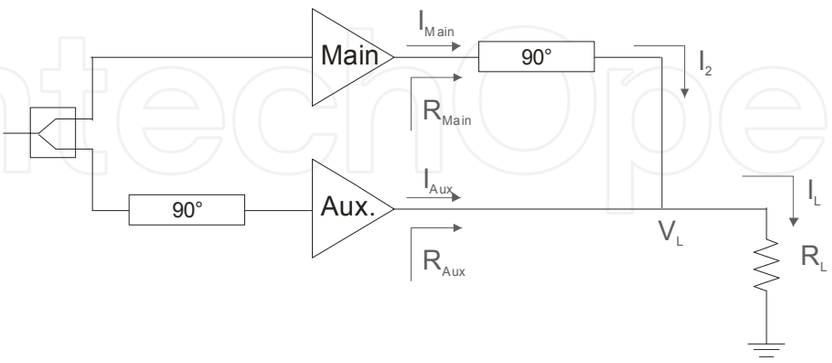

Fig. 5. Typical DPA structure.

In order to easy understand the DPA behavior, the following operating regions can be recognized (Raab, 1987).

For low input power level (i.e. Low Power Region, see Fig. 2), the DPA acts as a typical PA, since the Main device is conducting while the Auxiliary is OFF due to its Class C bias condition.
Increasing the input power level, the current supplied by the Main device to R_L increases reaching the device saturation ($I_{critical}$), thus the maximum efficiency condition. The corresponding input power level reaches a "break point" condition, while the expected load curve of both active devices are indicated in Fig. 6 with the letter A. For higher input power level (P_{in_DPA}>$P_{in\_DPA(break\ point)}$), the Auxiliary device will automatically turned on, injecting current into the output load R_L. Consequently, the impedance (Z_1) seen by the Main device is modulated and, thanks to the λ/4 TL, its value becomes lower with respect to the one at the break point (load curve "A" in the Fig. 6). In this way, the efficiency of the Main device remains constant, due to the constant level of saturation, while the efficiency of the Auxiliary device starts to increase (see Fig. 2). As a result, the overall DPA efficiency shows the typical behavior reported in Fig. 2.
At the end of the DPA dynamic, i.e. for the peak envelope value, both devices achieve their saturation corresponding to the load curves "C" in Fig. 6.

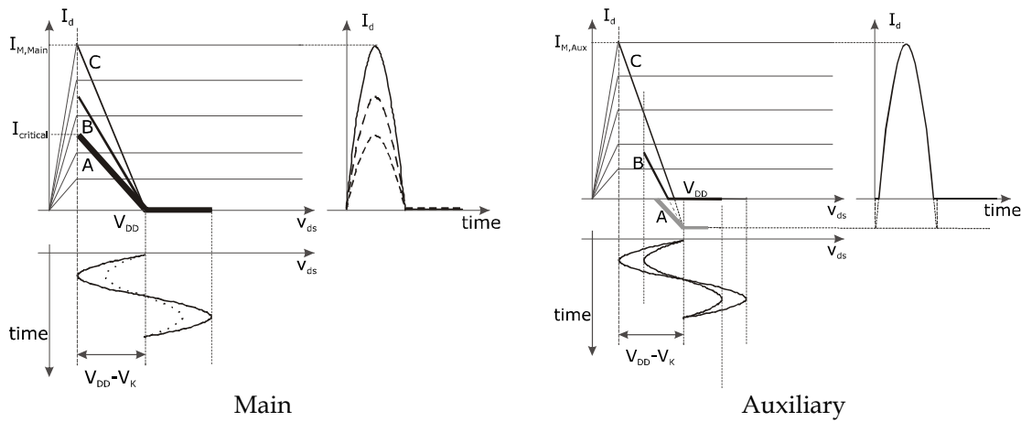

Fig. 6. Evolution of the load curves for both DPA active devices: Main (left) and Auxiliary (right) amplifiers.

3. The Doherty design guidelines

In order to infer useful design relationships and guidelines, simplified models are assumed for the elements which are included in the DPA architecture. In particular, the passive components (λ/4 TLs and power splitting) are assumed to be ideally lossless, while for the active device (in the following assumed as a FET device) an equivalent linearised model is assumed, as shown in Fig. 7. It is represented by a voltage-controlled current source, while for simplicity any parasitic feedback elements are neglected and all the other ones are embedded in the matching networks.

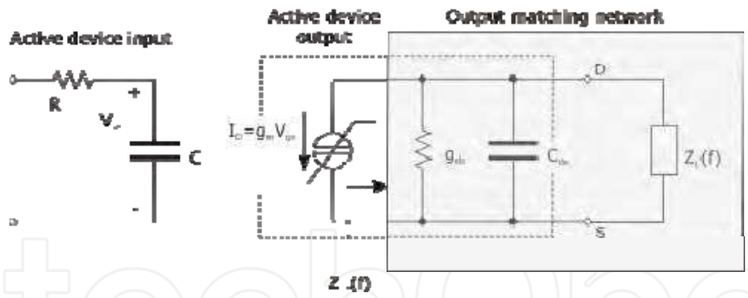

Fig. 7. Simplified model assumed for the active device.

The device output current source is described by a constant transconductance (g_m) in the saturation region, while a constant ON resistance (R_{ON}) is assumed for the ohmic region, resulting in the output I-V linearised characteristics depicted in Fig. 8.

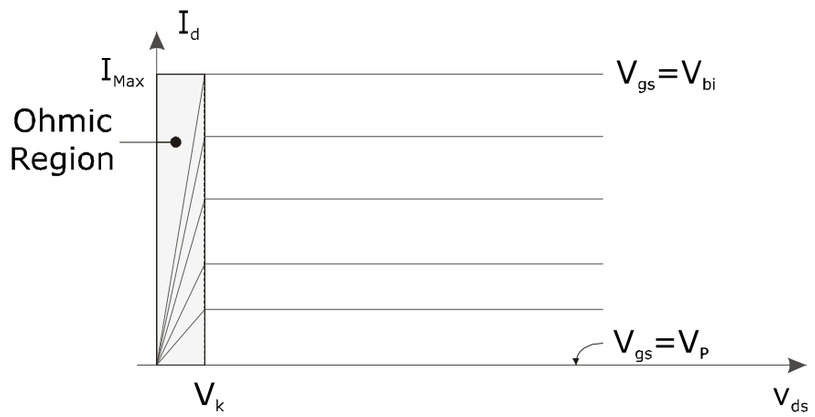

Fig. 8 I-V output characteristics of the simplified model assumed for the active device.

The main parameter taken into account to represent the simplified I-V characteristics are the maximum achievable output current (I_{Max}), the constant knee voltage (V_k) and the pinch-off voltage (V_p).
As it commonly happens in the amplifiers design, some parameters are assumed as starting requirements, thus imposed by the designer, while other ones are consequently derived. Obviously, the following guidelines outline only one of the possible design flows.
The design starts by fixing the OBO level, required to the DPA, accounting for the peculiar PAPR of the application which the DPA is oriented for. The OBO can be defined by the following equation:

$$OBO = \frac{P_{out,DPA(x=x_{break})}}{P_{out,DPA(x=1)}} = \frac{P_{out,Main(x=x_{break})}}{P_{out,Main(x=1)} + P_{out,Aux(x=1)}} \tag{6}$$

where the subscripts are used to refer to the entire DPA or to the single amplifiers (Main and Auxiliary respectively). Moreover a parameter x ($0 \le x \le 1$) is used to identify the dynamic point in which those quantities are considered. In particular $x=0$ identifies the quiescent state, i.e. when no RF signal is applied to the input, while $x=1$ identifies the saturation condition, i.e. when the DPA reaches its maximum output power level. Similarly, $x=x_{break}$ identifies the break point condition, i.e. when the Auxiliary amplifier is turned on.

Clearly, eqn. (6) is based on the assumption that only the Main amplifier delivers output power until the break point condition is reached, and the output network is assumed lossless.
In order to understand how the selected OBO affects the design, it is useful to investigate the expected DLLs of the Main and Auxiliary amplifiers for $x=x_{break}$ (load curves "A" in Fig. 6) and $x=1$ (load curves "C" in Fig. 6). It is to remark that the shape of the DLLs is due, for sake of simplicity, to the assumption of a Tuned Load configuration (Colantonio et al., 2002) both for Main and Auxiliary amplifiers.
Assuming a bias voltage V_{DD}, the drain voltage amplitude of the Main device is equal to V_{DD}-V_k both for $x=x_{break}$ and $x=1$
The same amplitude value is reached by the drain voltage of the Auxiliary device for $x=1$, as shown by the load curve "C" in Fig. 6.
Consequently the output powers delivered by the Main and Auxiliary amplifiers in such peculiar conditions become:

$$P_{out,Main(x=x_{break})} = \frac{1}{2} \cdot (V_{DD} - V_k) \cdot I_{1,Main(x=x_{break})} \tag{7}$$

$$P_{out,Main(x=1)} = \frac{1}{2} \cdot (V_{DD} - V_k) \cdot I_{1,Main(x=1)} \tag{8}$$

$$P_{out,Aux(x=1)} = \frac{1}{2} \cdot (V_{DD} - V_k) \cdot I_{1,Aux(x=1)} \tag{9}$$

where the subscript "1" is added to the current in order to refer to its fundamental component.
Referring to Fig. 5, the power balance at the two ports of the λ/4 both for $x=x_{break}$ and $x=1$ is given by:

$$\frac{1}{2} \cdot (V_{DD} - V_k) \cdot I_{1,Main(x=x_{break})} = \frac{1}{2} \cdot V_{L(x=x_{break})} \cdot I_{2(x=x_{break})} \tag{10}$$

$$\frac{1}{2} \cdot (V_{DD} - V_k) \cdot I_{1,Main(x=1)} = \frac{1}{2} \cdot (V_{DD} - V_k) \cdot I_{2(x=1)} \tag{11}$$

being I_2 the current flowing into the load R_L from the Main branch.
From (11) it follows:

$$I_{1,Main(x=1)} = I_{2(x=1)} \tag{12}$$

Moreover, remembering that the current of one side of the λ/4 is function only of the voltage of the other side, it is possible to write

$$I_{2(x=x_{break})} = I_{2(x=1)} \tag{13}$$

since the voltage at the other side is assumed constant to V_{DD}–V_k in all medium power region, i.e. both for $x=x_{break}$ and $x=1$.
Consequently, taking into account (11), the output voltage for $x=x_{break}$ is given by:

$$V_{L(x=x_{break})} = (V_{DD} - V_k) \cdot \frac{I_{1,Main(x=x_{break})}}{I_{1,Main(x=1)}} = \alpha \cdot (V_{DD} - V_k) \tag{14}$$

where α defines the ratio between the currents of the Main amplifier at $x=x_{break}$ and $x=1$:

$$\alpha = \frac{I_{1,Main(x=x_{break})}}{I_{1,Main(x=1)}} \tag{15}$$

Regarding the output resistance (R_L), its value has to satisfy two conditions, imposed by the voltage and current ratios at $x=x_{break}$ and $x=1$ respectively:

$$R_L = \frac{V_{L(x=x_{break})}}{I_{2(x=x_{break})}} = \frac{\alpha \cdot (V_{DD} - V_k)}{I_{1,Main(x=1)}} \tag{16}$$

$$R_L = \frac{V_{L(x=1)}}{I_{2(x=1)} + I_{1,Aux(x=1)}} = \frac{(V_{DD} - V_k)}{I_{1,Main(x=1)} + I_{1,Aux(x=1)}} \tag{17}$$

Therefore, from the previous equations it follows:

$$I_{1,Aux(x=1)} = \frac{1-\alpha}{\alpha} \cdot I_{1,Main(x=1)} \tag{18}$$

Consequently, substituting (7)-(9) (9) in (6)and taking into account for (18), the following relationship can be derived:

$$OBO = \alpha^2 \tag{19}$$

which demonstrates that, selecting the desired OBO, the ratio between the Main amplifier currents for $x=x_{break}$ and $x=1$ is fixed also.
Since the maximum output power value is usually fixed by the application requirement, it represents another constraints to be selected by the designer. Such maximum output power is reached for $x=1$ and it can be estimated by the following relationship:

$$P_{out,DPA(x=1)} = P_{out,Main(x=1)} + P_{out,Aux(x=1)} = \frac{1}{\alpha} \cdot \frac{1}{2} \cdot (V_{DD} - V_k) \cdot I_{1,Main(x=1)} \tag{20}$$

which can be used to derive the maximum value of fundamental current of Main amplifier ($I_{1,Main(x=1)}$), once its drain bias voltage (V_{DD}) and the device knee voltage (V_k) are selected.
Knowing the maximum current at fundamental, it is possible to compute the values of R_L by (16)(16) and the required characteristic impedance of the output λ/4 TL (Z_0) by using:

$$Z_0 = \frac{(V_{DD} - V_k)}{I_{1,Main(x=1)}} \tag{21}$$

which is derived assuming that the output voltage (V_L) reaches the value V_{DD}-V_k for $x=1$.
Clearly the maximum value $I_{1,Main(x=1)}$ depends on the Main device maximum allowable output current I_{Max} and its selected bias point.

Referring to Fig. 9, where it is reported for clearness a simplified current waveform, assuming a generic Class AB bias condition, the bias condition can be easily identified defining the following parameter

$$\xi = \frac{I_{DC,Main}}{I_{Max,Main}} \tag{22}$$

being $I_{DC,Main}$ the quiescent (i.e. bias) current of the Main device.
Consequently, ξ=0.5 and ξ=0 refer to a Class A and Class B bias conditions respectively, while 0<ξ<0.5 identifies Class AB bias condition.

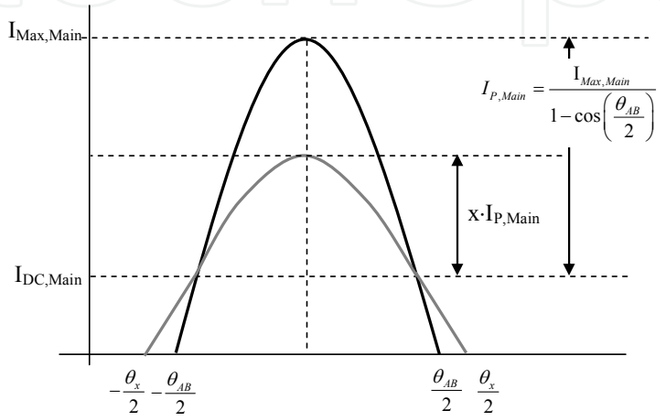

Fig. 9. Current waveform in time domain of the Main amplifier.

The current waveform of Fig. 9 can be analytically described by the following expression:

$$i_{D,Main} = I_{DC,Main} + x \cdot \frac{I_{Max,Main}}{1-\cos\left(\frac{\theta_{AB}}{2}\right)} \cdot \cos(\theta) \tag{23}$$

whose fundamental component can be written as following:

$$I_{1,Main(x=1)} = \frac{I_{Max,Main}}{2\pi} \cdot \frac{\theta_{AB} - \sin(\theta_{AB})}{1-\cos\left(\frac{\theta_{AB}}{2}\right)} \tag{24}$$

being θ_{AB} the current conduction angle (CCA) of the Main output current, achieved for *x=1*.
The bias point ξ and the CCA θ_{AB} can be easily related by the following relationship:

$$\theta_{AB} = 2\pi - 2\arccos\left(\frac{\xi}{1-\xi}\right) \tag{25}$$

Manipulating (24), the value of $I_{Max,Main}$, required to reach the desired maximum power, can be estimated, once the bias point ξ of the Main amplifier has been selected (the last parameter should be fixed by the designer).
As made with Main amplifier, the value of the Auxiliary maximum current can be obtained by using the equation of the first order coefficient of the Furier series, since the value of $I_{1,Aux,(x=1)}$ should fulfill (18).
Consequently, it follows:

$$I_{1,Aux(x=1)} = \frac{I_{Max,Aux}}{2\pi} \cdot \frac{\theta_C - \sin(\theta_C)}{1 - \cos\left(\frac{\theta_C}{2}\right)} \tag{26}$$

being θ_C the CCA of the Auxiliary device output current for $x=1$.
Referring to Fig 10, where it is reported the current waveform of the Auxiliary amplifier, assuming a virtual negative bias point, the Auxiliary device current can be written similarly to (23), thus:

$$i_{D,Aux} = I_{DC,Aux} + x \cdot \frac{I_{Max,Aux}}{1 - \cos\left(\frac{\theta_C}{2}\right)} \cdot \cos(\theta) \tag{27}$$

Moreover, for a proper behavior of the Auxiliary amplifier, the peak of the current has to reach zero for $x=x_{break}$, as highlighted in Fig10. Consequently the following condition has to be taken into account.

$$x_{break} \cdot \frac{I_{Max,Aux}}{1 - \cos\left(\frac{\theta_C}{2}\right)} = -I_{DC,Aux} \tag{28}$$

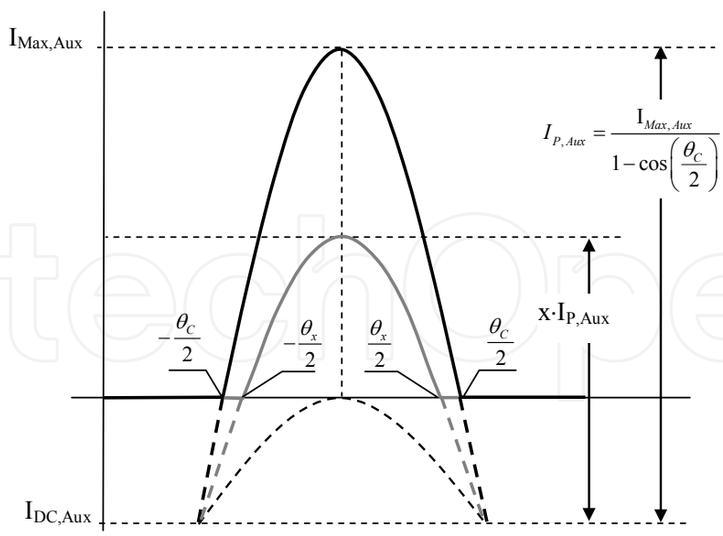

Fig. 10. Current waveform in time domain of the Auxiliary amplifier for $x=x_{break}$ and $x=1$.

Substituting (28) in (27), it is possible to refer the value of θ_C directly to x_{break}:

$$\theta_C = 2 \cdot \arccos(x_{break}) \tag{29}$$

Now, from (15) and replacing the respective Fourier expressions, it follows:

$$x_{break} \cdot \left[\theta_{Main(x=x_{break})} - \sin\left(\theta_{Main(x=x_{break})}\right) \right] = \alpha \cdot \left(\theta_{AB} - \sin\left(\theta_{AB}\right)\right) \tag{30}$$

where from (23) it can be inferred:

$$\theta_{Main(x=x_{break})} = 2\pi - 2\arccos\left(\frac{\xi}{x_{break} \cdot (1-\xi)}\right) \tag{31}$$

The value of x_{break} has to be numerically obtained solving (30), having fixed the OBO (i.e. a) and the Main device bias point (i.e. ξ).
Once the value of $I_{Max,Aux}$ is obtained, the one of $I_{DC,Aux}$ is immediately estimable manipulating (28):

$$I_{DC,Aux} = -I_{Max,Aux} \cdot \frac{x_{break}}{1 - x_{break}} \tag{32}$$

At this point, an interesting consideration can be done about the ratio between the maximum currents required by the devices. Fig. 11 reports this ratio as function of OBO and ξ. As it is possible to note, the dependence on ξ can be practically neglected, while the one by the OBO is very high. Moreover, the same amount of maximum current is required from both devices in case of nearly 5dB as OBO, while an higher current has to be provided by the Auxiliary device for greater OBO.
From the designer point of view, the maximum currents ratio can be used as an useful information to choice the proper device periphery. In fact, supposing for the used technology a linear relationship between maximum current and drain periphery, Fig. 11 gives the possibility to directly derive the drain periphery of the Auxiliary device, once the Main one has been selected in order to respect the maximum output power constraint.

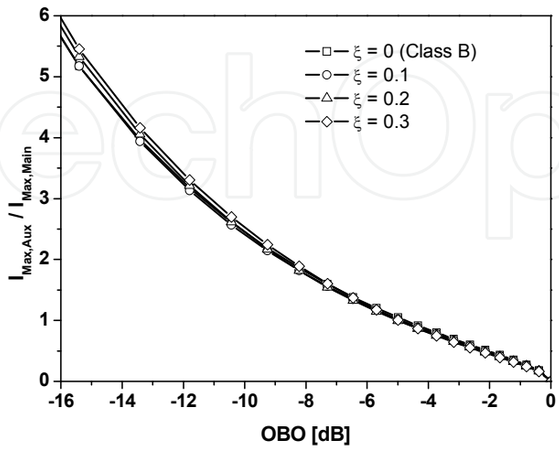

Fig. 11. Ratio between Auxiliary and Main maximum currents as function of OBO and ξ.

3.1. Power splitter dimensioning

In this subsection the dimensioning of the input power splitter is discussed, highlighting its critical role in the DPA architecture.

Following the simplified analysis based on an active device with constant transconductance (g_m), the amplitude of the gate voltage for *x=1*, for Main and Auxiliary devices respectively, can be written as

$$V_{gs,Main(x=1)} = \frac{I_{Max,Main} - I_{DC,Main}}{g_{m,Aux}} = \frac{I_{Max,Main} \cdot (1-\xi)}{g_{m,Main}} \tag{33}$$

$$V_{gs,Aux(x=1)} = \frac{I_{Max,Aux} - I_{DC,Aux}}{g_{m,Aux}} = \frac{I_{Max,Aux}}{g_{m,Aux}} \cdot \frac{1}{1-x_{break}} \tag{34}$$

Using the previous equations, it is possible to derive the powers at the input of the devices by using the following relationships:

$$P_{in,Main(x=1)} = \frac{1}{2} \cdot \frac{\left(V_{gs,Main(x=1)}\right)^2}{R_{in,Main}} = \frac{1}{2} \cdot \frac{\left(I_{Max,Main} \cdot (1-\xi)\right)^2}{R_{in,Main} \cdot \left(g_{m,Main}\right)^2} \tag{35}$$

$$P_{in,Aux(x=1)} = \frac{1}{2} \cdot \frac{\left(V_{gs,Aux(x=1)}\right)^2}{R_{in,Aux}} = \frac{1}{2} \cdot \frac{\left(I_{Max,Aux}\right)^2}{R_{in,Aux} \cdot \left(g_{m,Aux} \cdot (1-x_{break})\right)^2} \tag{36}$$

where $R_{in,Main}$ and $R_{in,Aux}$ are the input resistances respectively of Main and Auxiliary devices.

Therefore, it is possible to compute the power splitting factor, i.e. the amount of power delivered to the Auxiliary device with respect to the total input power, by using:

$$\Lambda_{Aux} = \frac{P_{in,Aux(x=1)}}{P_{in,Main(x=1)} + P_{in,Aux(x=1)}} = \frac{1}{\left(\frac{I_{Max,Main}}{I_{Max,Aux}} \cdot \frac{1-\xi}{1-x_{break}} \cdot \frac{g_{m,Aux}}{g_{m,Main}}\right)^2 \cdot \frac{R_{in,Aux}}{R_{in,Main}} + 1} \tag{37}$$

and consequently for the Main device:

$$\Lambda_{Main} = 1 - \Lambda_{Aux} \tag{38}$$

In Fig. 12 is reported the computed values for Λ_{Aux}, as function of OBO and ξ parameters, assuming for both devices the same values for g_m and R_{in}.

Fig. 12 highlights that large amount of input power has to be sent to the Auxiliary device, requiring an uneven power splitting. For example, considering a DPA with 6dB as OBO and a Class B bias condition (i.e $\xi=0$) for the Main amplifier, 87% of input power has to be provided to Auxiliary device, while only the remaining 13% is used to drive the Main amplifier. This aspect dramatically affects in a detrimental way the overall gain of the DPA, which becomes 5-6 dB lower if compared to the gain achievable by using a single amplifier only.

Nevertheless, it has to remark that this largely unbalanced splitting factor has been inferred assuming a constant transconductance (g_m) for both devices. Such approximation is

sufficiently accurate in the saturation region ($x=1$), while becomes unsatisfactory for low power operation. In this case, the actual transconductance behavior can be very different depending on the technology and bias point of the selected active device. In general, it is possible to state that the transconductance value of actual devices, in low power region, is lower than the average one, when the chosen bias point is close to the Class B. Thus, if the bias point of Main amplifier ξ is selected roughly lower than 0.2, the predicted gain in low power region is higher than the experimentally resulting one, being the former affected by the higher value assumed for the transconductance in the theoretical analysis.

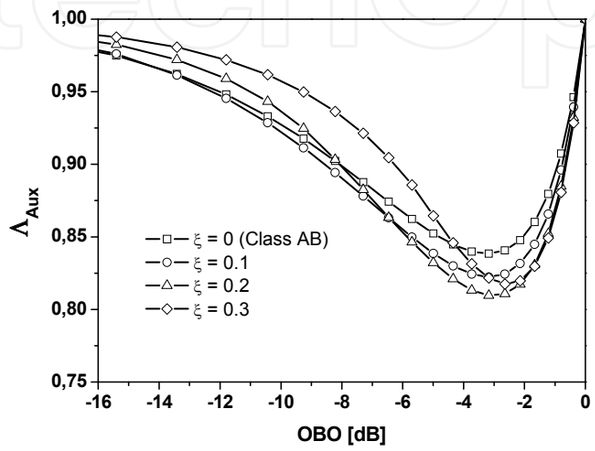

Fig. 12. Λ_{Aux} behavior as a function of OBO and ξ, assuming for both devices the same values for g_m and R_{in}.

From a practical point of view, if the theoretical splitting factor is assumed in actual design, usually the Auxiliary amplifier turns on before the Main amplifier reaches its saturation (i.e. its maximum of efficiency). Consequently a reduction of the unbalancing in the power splitter is usually required in actual DPA design with respect to the theoretical value, in order to compensate the non constant transconductance behavior and, thus, to switch on the Auxiliary amplifier at the proper dynamic point.

3.2. Performance behavior

Once the DPA design parameters have been dimensioned, closed form equations for the estimation of the achievable performances can be obtained. Since the approach is based on the electronic basic laws, it will be here neglected, in order to avoid that this chapter dull reading and to focus the attention on the analysis of the performance behavior in terms of output power, gain, efficiency and AM/AM distortion. The complete relationships can be found in (Colantonio et al., 2009 - a).

The theoretical performance of a DPA designed to fulfill 7dB of OBO and 6W as maximum output power, are shown in Fig. 12. Moreover, the same physical parameters have been assumed for both Main and and Auxiliary devices: $V_k=0V$, $g_m=0.22S$ and $R_{in}=50\Omega$. Finally the drain bias voltage and the Main amplifier quiescent point have been fixed to $V_{DD}=10V$ and $\xi=0.1$ respectively.

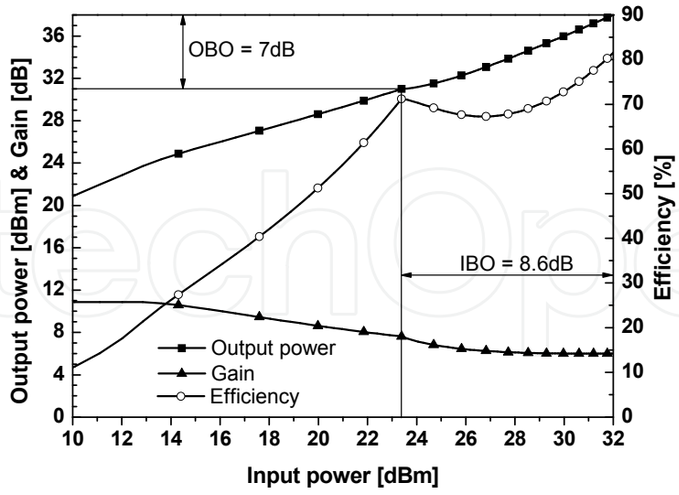

Fig. 12. Theoretical performances of a DPA with 7dB OBO and 6W as maximum output power.

As it appears looking at Fig. 13, the efficiency value at the saturation is higher than the one at the break point. The latter, in fact, is the one of the Main device, which is a Class AB amplifier. The efficiency at the saturation, instead, is increased by the one of the Auxiliary device, which has a Class C bias point, with a consequent greater efficiency value.
It is possible to note as the gain behaves linearly until 13dBm of input power, while becomes a monotonic decreasing function up to about 23.5dBm. Along this dynamic region, the Main amplifier only is working and the variation of the gain behavior is due to the pinch-off limitation in the output current.
In particular, until 13dBm, the Main device operates as a Class A amplifier, since its DLL did not reach yet the pinch-off physical limitation. Then, the Main device becomes a Class AB amplifier, coming up to the near Class B increasing the input power, with a consequent decreasing of the gain. However this evident effect of class (and gain) changing is due to the assumption of a constant transconductance model for the active device. In actual devices, in fact, the value of the transconductance is lower than the average one, when the selected bias point is close to the Class B, as it has been discussed in section 3.1. Consequently, in practical DPA design, the gain, for small input power levels, is lower than the theoretical one estimated by the average g_m value, thus reducing the effect highlighted in Fig. 12.
In the Doherty region, from 23.5dBm up to 32dBm of input power, the gain changes its behavior again. The latter change is due to the combination of the gain decreasing of the Main amplifier, whose output resistance is diminishing, and the gain increasing of the Auxiliary amplifier, which passes from the switched off condition to the proper operative Class C.
The non constant gain behavior is further highlighted in Fig. 12 by the difference between the resulting OBO and input back-off (IBO), resulting in an AM/AM distortion in the overall DPA. In order to deeply analyze this effect, Fig. 13 reports the difference between OBO and IBO for several values of ξ.

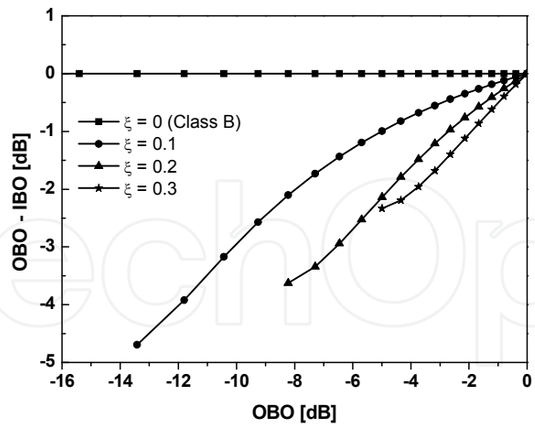

Fig. 13. Theoretical difference between OBO and IBO for several values of ξ.

In order to proper select the Main device bias point ξ to reduce AM/AM distortion, it is useful to introduce another parameter, the Linear Factor (LF), defined as:

$$LF = \frac{1}{1 - x_{break}} \cdot \int_{x_{break}}^{1} \left[P_{out,DPA}(x) - \left(x^2 \cdot P_{out,DPA(x=1)} \right) \right] dx \tag{39}$$

The Linear Factor represents the variation in the Doherty region of the DPA output power, with respect to a linear PA having the same maximum output power and represented in (39)(39) by $x^2 \cdot P_{out,DPA(x=1)}$. Thus LF gives the simplified estimation of the average AM/AM distortion in the Doherty region.
Consequently, the optimum bias condition should be assumed to assure LF=0. Obviously this condition, if it exists, can be obtained only for one ξ, once the OBO has been selected.

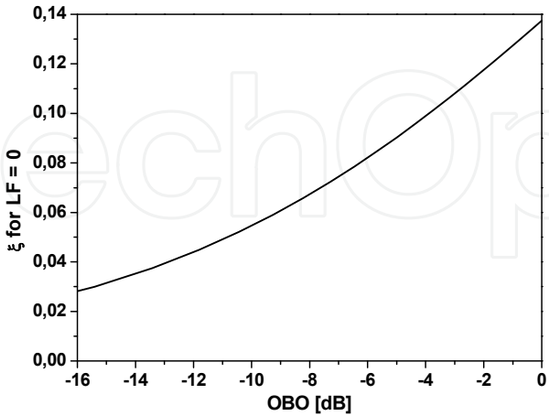

Fig. 14. Values of ξ assuring LF=0, as function of the OBO.

Fig. 14 shows the values of ξ, which theoretically assures LF=0, as function of the selected OBO. This design chart provides a guideline to select the proper bias point of the Main amplifier (ξ), having fixed the desired OBO of the DPA.
In order to further clarify the DPA behavior, Fig. 15 shows the fundamental drain currents and voltages for both Main and Auxiliary devices. These behaviors can be used in the design flow to verify if the DPA operates in a proper way. In particular, the attention has to be focused on the Main voltage, which has to reach, at the break point (x_{break}), the maximum achievable amplitude (10V in this example) in order to maximize the efficiency. Moreover the Auxiliary current can be used to verify that the device is turned on in the proper dynamic instant. Finally, the designer has to pay attention if the Auxiliary current reaches the expected value at the saturation ($x=1$), in order to perform the desired modulation of the Main resistance. This aspect can be evaluated also observing the behavior of Main and Auxiliary resistances, as reported in Fig. 17.

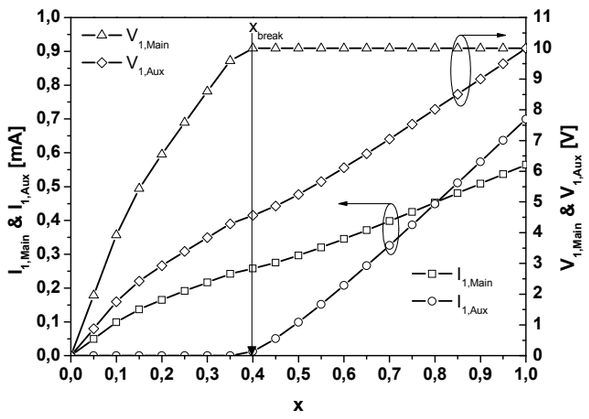

Fig. 15. Fundamental current and voltage components of Main and Auxiliary amplifiers, as function of the dynamic variable x.

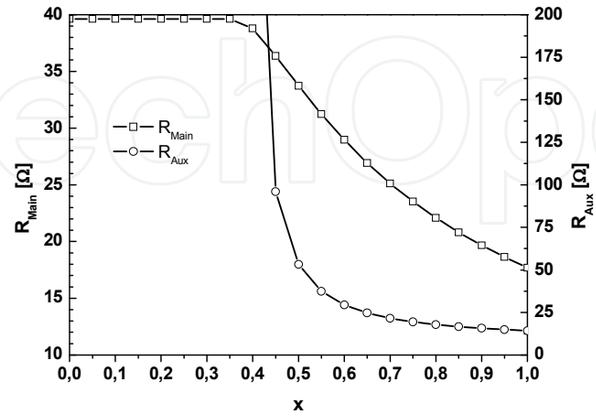

Fig. 17. Drain resistance at fundamental frequency of Main and Auxiliary amplifiers, as function of the dynamic variable x.

4. Advanced DPA Design

In the previous paragraphs the classical Doherty scheme based on Tuned Load configuration for both Main and Auxiliary amplifiers has been analyzed. Obviously, other solutions are available, still based on the load modulation principle, but developed with the aim to further improve the features of the DPA, by using additional some free design parameters.

4.1. DPA Design by using different bias voltage

For instance, the adoption of different drain bias voltage for the two amplifiers (Main and Auxiliary) could be useful to increase the gain of the overall DPA. In fact, in the DPA topology the voltage at the output common node, V_L in Fig. 5, at saturation is imposed by the Auxiliary drain bias voltage ($V_{DD,Aux}$) in order to fulfill the condition $V_L = V_{DD,Aux} - V_{k,Aux}$. Thus, assuming a different bias, i.e. $V_{DD,Main}$ and $V_{DD,Aux}$ for the Main and Auxiliary devices respectively, and defining the parameter

$$\beta = \frac{V_{DD,Main} - V_{k,Main}}{V_{DD,Aux} - V_{k,Aux}} \tag{40}$$

then the design relationships previously inferred have to be tailored accounting for such different supplying voltages.
Therefore, the DPA elements R_L and Z_0 becomes:

$$R_L = \frac{\alpha^2}{\beta^2} \cdot R_{Main}\left(x_{break}\right) \tag{41}$$

$$Z_0 = \frac{V_{DD,Aux} - V_k}{I_{1,Main}\left(\theta_{AB}\right)} \tag{42}$$

where

$$R_{Main}\left(x_{break}\right) = 2\frac{V_{DD,Main} - V_{k,Main}}{I_{M,Main}}\frac{\pi}{\alpha} \cdot \frac{1-\cos\left(\frac{\theta_{AB}}{2}\right)}{\theta_{AB} - \sin\left(\theta_{AB}\right)} \tag{43}$$

Moreover, the Auxiliary and Main devices maximum output currents are now related through the following relationship:

$$I_{M,Aux} = \beta \cdot I_{M,Main} \cdot \frac{1-\alpha}{\alpha} \cdot \frac{1-\cos\left(\frac{\theta_C}{2}\right)}{\theta_C - \sin\left(\theta_C\right)} \cdot \frac{\theta_{AB} - \sin\left(\theta_{AB}\right)}{1-\cos\left(\frac{\theta_{AB}}{2}\right)} \tag{44}$$

Which, clearly, highlights that a suitable selection of the Auxiliary device supply voltage, i.e. $\beta<1$, could imply a lower maximum output current required from the Auxiliary device.
Conversely, the saturated output power of the Doherty (for $x=1$) is still related to both the Main device supply voltage and its maximum output current, i.e.:

$$P_{out,DPA(x=1)} = \frac{1}{2}\left(V_{DD,Main} - V_k\right) \cdot \frac{I_{1,Main}\left(\theta_{AB}\right)}{\alpha} = \frac{1}{\alpha} \cdot P_{out,Main,Max} = \frac{1}{\alpha^2} \cdot P_{out,Main,break} \tag{45}$$

Thus being not affected by the different drain supply voltage adopted for the Auxiliary device.

4.2. DPA Design by using Harmonic Tuning strategies

To further improve the overall efficiency in a Doherty configuration, high efficiency design strategies can be adopted in the synthesis of both Main and Auxiliary amplifiers. For this purpose, harmonic tuning strategies have been proposed (Colantonio et al., 2002).
However, due to the Class C bias condition for the Auxiliary device, thus implying a wrong phase relationships between current (and voltage) harmonic components, the optimum solution for such amplifier is the classical Tuned Load one.
Conversely, for the Main amplifier, which is normally operating in a Class AB bias, the efficiency can be improved by using for instance Class F strategy (Raab, 2001). Such design strategy implies that the second harmonic current component I_2 should be short circuited, while the fundamental (I_1) and the third one (I_3) should be terminated on impedance R_1 and R_3, respectively, to obtain a proper voltage harmonic component ratio (Colantonio et al., 2002):

$$k_3 = \frac{V_3}{V_1} = \frac{R_3 \cdot I_3}{R_1 \cdot I_1} = 0.167 \tag{46}$$

Thus, in a Class F Doherty amplifier (i.e. with Main amplifier in Class F configuration), the proper output harmonic loading conditions have to be fulfilled across the Main device, accounting for the load modulation effect in the medium power region.
In particular, it is possible to compute the theoretical load modulation required for the third harmonic, in order to fulfill (46) accounting for the modulation of R_1. In Fig. 16 is reported the ratio between the values required for R_3 at the end of the low power region ($x=x_{break}$) and at the end of the Medium (or Doherty) power region, i.e. at saturation ($x=1$), as a function of the Main device bias point (ξ) and the selected OBO.

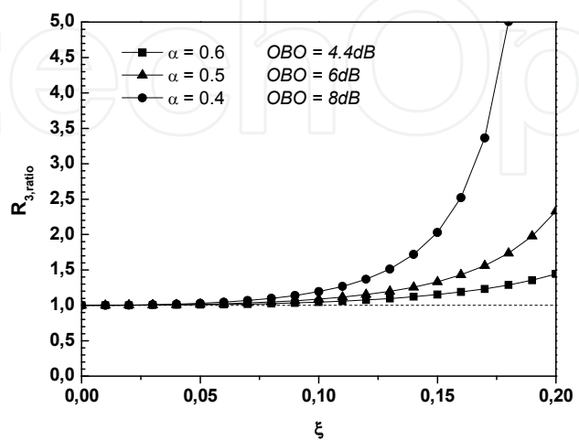

Fig. 16. $R_{3,ratio}$ as function of ξ for different OBO (α) values.

As it can be noted, the $R_{3,ratio}$ (i.e. the degree of modulation required for the third harmonic loading condition) increases with the bias point (ξ) and OBO values (α).
Nevertheless, the modulation of R_3 through the output λ/4 line and the Auxiliary current, critically complicate the design and can be usually neglected if the Main device bias point is chosen nearly Class B condition, i.e. ξ<0.1, being $R_{3,ratio}$≈1.
Under such assumption, it is possible to compute the Class F DPA design parameter as compared to the Tuned Load case.
It can be inferred, referring to Fig. 3, that the output load R_L and the characteristic impedance of the output λ/4 TL become

$$R_{L,F} \simeq \frac{R_L}{1.15} \qquad Z_{0,F} = Z_{0,TL} \tag{47}$$

being R_L given equivalently by (16) or (17) and Z_0 by (21).
Finally, regarding the power splitter dimensioning, it is required a different power splitting ratio, resulting in:

$$\Lambda_{Aux,F} = \frac{1.322 \cdot \Lambda_{Aux}}{1 + 0.322 \cdot \Lambda_{Aux}} > \Lambda_{Aux} \quad \Lambda_{Main,F} = 1 - \Lambda_{Aux,F} < \Lambda_{AB} \tag{48}$$

The expected behavior of the output current and voltage fundamental components for the Main and the Auxiliary devices are reported in Fig. 19, assuming ξ=0.082 and OBO=6dB (i.e. α=0.5).
Similarly, in Fig. 17 are reported the comparisons in terms of output power and efficiency of Class F DPA with respect to Tuned Load DPA, normalized as functions of the input signal x.

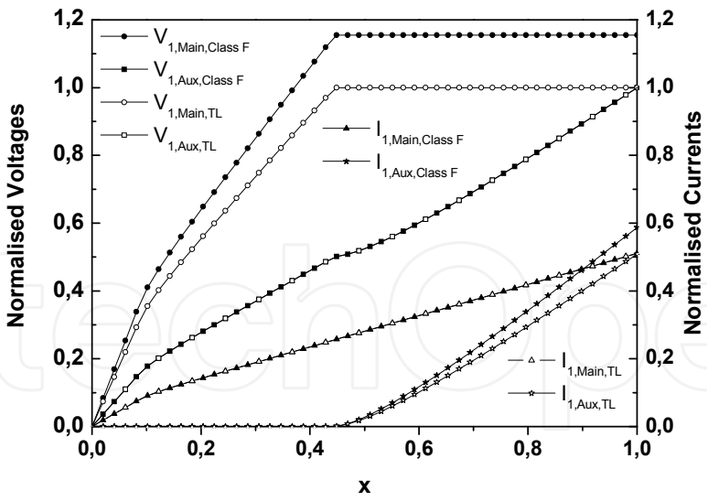

Fig. 19. Theoretical behavior of drain current and voltage fundamental components for Main and Auxiliary devices, assuming Class F or Tuned Load design strategies for Main amplifier.

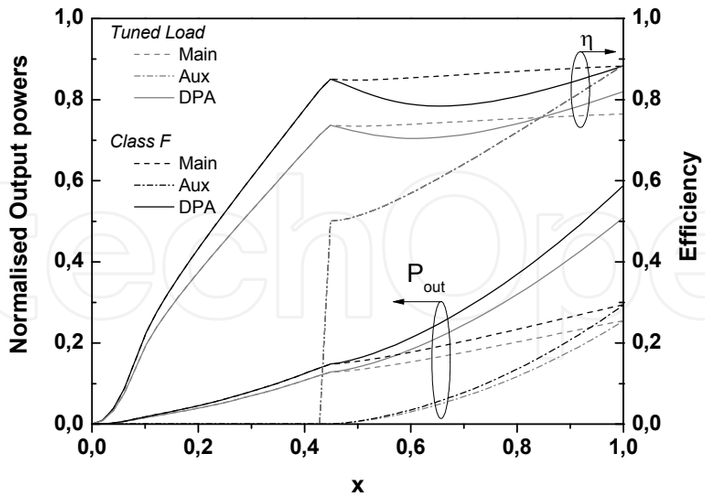

Fig. 17. Expected drain efficiency and output power behaviors for Class F and Tuned Load Doherty amplifiers.

4.3. Multi-way Doherty amplifiers

In order to reduce the Auxiliary device size, while still providing the required current for the load modulation, a different solution is based on the so called Multi-Way Doherty configuration, usually referred as N-Way Doherty amplifier also (Yang et al., 2003 – Kim et al., 2006 – Cho et al., 2007). It is realized by paralleling one Main amplifier and N-1 Auxiliary amplifiers, aimed to acquire an N-1 times larger-sized Auxiliary amplifier, as schematically shown in Fig. 18.

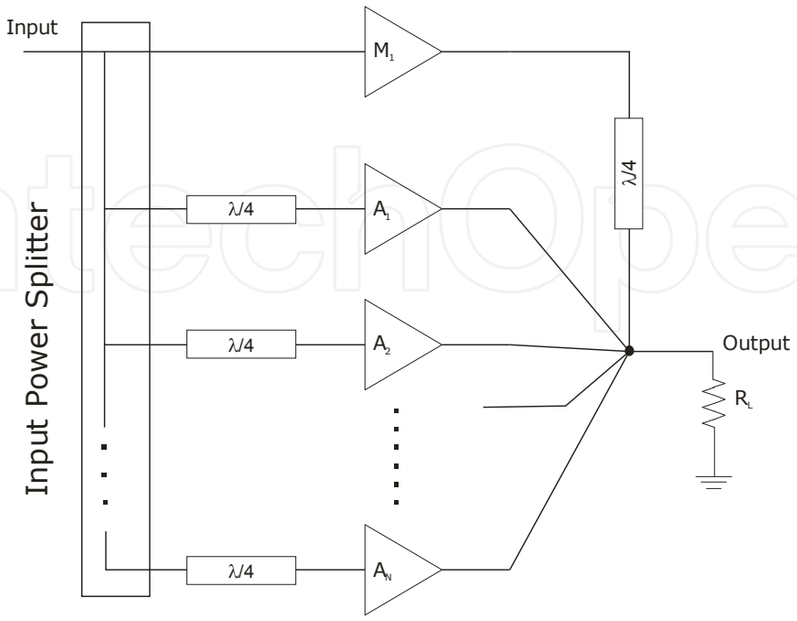

Fig. 18. Schematic diagram of the N-way Doherty amplifier.

With the proposed device combination, it becomes possible to implement larger OBO using smaller devices, resulting in the theoretical efficiency performance shown in Fig. 19.

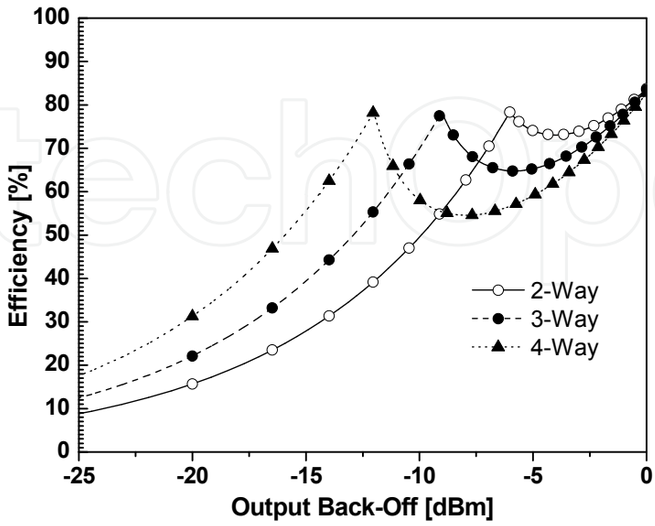

Fig. 19. Theoretical efficiency of the N-Way Doherty amplifier.

4.4. Multi-Stage Doherty amplifiers

The Multi-Stage Doherty amplifier is conceptually different from the Multi-Way configuration, since it is based on a subsequent turning on condition of several Auxiliary devices, with the aim to assure a multiple Doherty region in a cascade configuration, overcoming the reduction of the average value due to the increased drop-down phenomenon in efficiency, especially when larger OBO are required (Neo et al., 2007 – Pelk et al., 2008 – Srirattana et al., 2005).

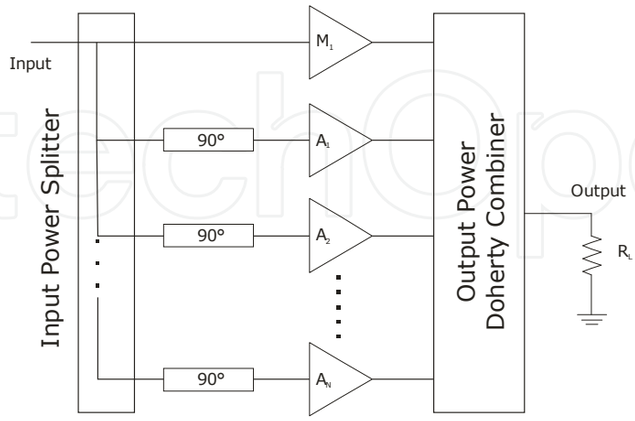

Fig. 20. Theoretical diagram of a Multi-Stage Doherty amplifier.

For this purpose, referring to the theoretical diagram shown in Fig. 23, amplifiers M_1 and A_1 have to be designed to act as Main and Auxiliary amplifiers in a standard Doherty

configuration. Then, when both amplifiers are approaching their saturation, amplifier A_2 is turned on operating as another Auxiliary amplifier, thus modulating the load seen by the previous M_1-A_1 pair, that must be considered, from now onward, as a single amplifier. Such concept is then iterated inserting N Auxiliary amplifiers, each introducing a new break-point, resulting in a theoretical efficiency behavior as depicted in Fig. 21.

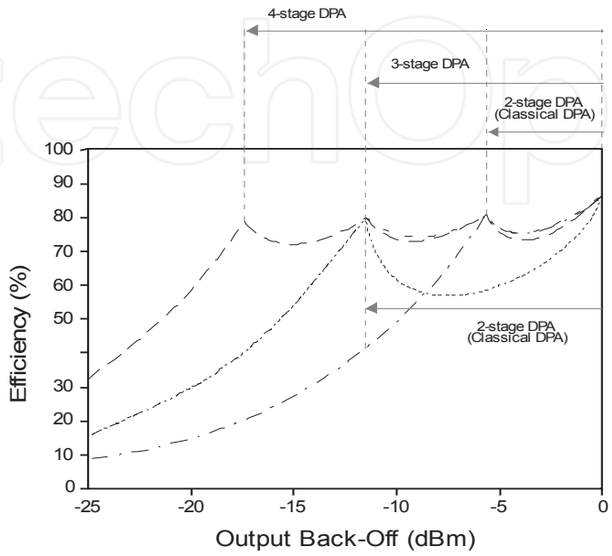

Fig. 21. Theoretical behavior of the efficiency for a Multi-Stage Doherty amplifier.

From the design issues, it is easy to note that the most critical one resides in the practical implementation of the output power combining network, required to properly exploit the load modulation concept for all the cascaded stages.
A proposed solution is reported in (Neo et al., 2007 – Pelk et al., 2008), based on the scheme depicted in Fig. 22, where the relationships to design the output λ/4 transmission lines adopted are given by

$$\begin{aligned} Z_{0,i} &= R_L \cdot \prod_{j=1}^{i} \frac{1}{\alpha_j} \\ \prod_{j=k}^{\frac{i+k}{2}} \alpha_{2j-k} &= 10^{-\frac{OBO_i}{20}} \end{aligned} \tag{49}$$

where $i=1,2,...N$, $k=1$ (for odd i) or $k=2$ (for even i), N is the total number of Auxiliary amplifiers, OBO_i is the back-off level from the maximum output power of the system at which the efficiency will peak (i.e. the turning on condition of the Auxiliary A_i).
The R_L value is determined by the optimum loading condition of the last Auxiliary stage, according to the following relationship:

$$R_L = (1-\alpha_1) \cdot R_{opt,Aux_N} \tag{50}$$

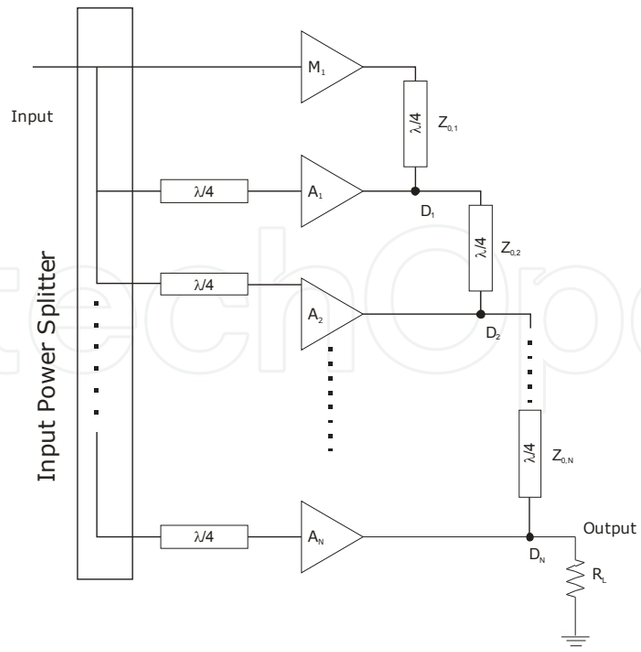

Fig. 22. Proposed schematic diagram for a multi-stage Doherty amplifier.

However, some practical drawbacks arise from the scheme depicted in Fig. 22. In fact, the Auxiliary device A_1 is turned on to increase the load at D_1 node and consequently, due to the $\lambda/4$ line impedance $Z_{0,1}$, to properly decrease the load seen by M_1. However, when A_2 is turned on, its output current contributes to increase the load impedance seen at D_2 node. Such increase, while it is reflected in a suitable decreasing load condition for A_1 (at D_1 node), it also results in an unwanted increased load condition for M_1, still due to the $\lambda/4$ line transformer. As a consequence, such device results to be overdriven, therefore saturating the overall amplifier and introducing a strong non linearity phenomenon in such device. To overcome such a drawback, it is mandatory to change the operating conditions, by turning on, for instance, the corresponding Auxiliary device before the Main device M_1 has reached its maximum efficiency, or similarly, changing the input signal amplitudes to each device (Pelk et al., 2008).
Different solutions could be adopted for the output power combiner in order to properly exploit the Doherty idea and perform the correct load modulation, and a optimized solution has been identified as the one in (Colantonio et al., 2009 - a).

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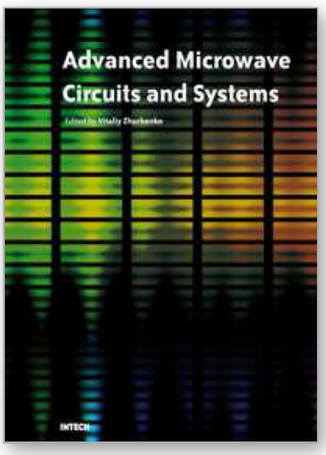

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University Campus STeP Ri
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