Contamination monitoring and analysis in semiconductor manufacturing

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1. Introduction: Contamination on wafers

1.1 Definition of the different type of contamination

Contamination is defined as a foreign material at the surface of the silicon wafer or within the bulk of the silicon wafer. The contamination can be particles or ionic contamination, liquid droplets… The mechanism of contamination of silicon wafer is summarized on figure 1 (Leroy, 1999):

- The source of contamination
- The transportation of the contamination
- The location of the contamination: surface, bulk
- The evolution of the contamination: how to remove it? Does the cleaning remove the contamination? Does the cleaning bring the contamination?

The chemistries of the cleaning solutions which are described within the figure 1 are able to remove particles or metallic contamination. They can also bring both of these contaminants. In this discussion, we just want to underline the source of contamination, and the way to measure it. Another way to consider wafer contamination source is the environment of the wafer (Pic, 2006):

- Contact with the wafer: chemicals, Gases, Ultra pure Deionised Water, resist, ionic implantation, deposition layers, etching process
- Environment for the process: tool, network for gases and chemicals distribution, boxes for wafer handling and transportation.
- General environment: facilities, human, external pollution (traffic, industrial)

Semiconductor devices are sensitive to the contamination, due to different possible root causes: device size reduction, device sensitivities on some process steps, cross contamination induced by chemicals, ultra pure water and gases. The environment is also contributing to the contamination effect on the wafer as tools, transportation boxes, and clean-room. Contamination can be divided in three categories: ionic contamination, airborne molecular contamination (AMC) and particles (defect density).

In this chapter, after a short description of the different contamination impact on wafers, we focus on metallic and anions contamination measurements with some examples. Then the

second part of this chapter will consider the particle monitoring on bare wafers and patterned wafers.

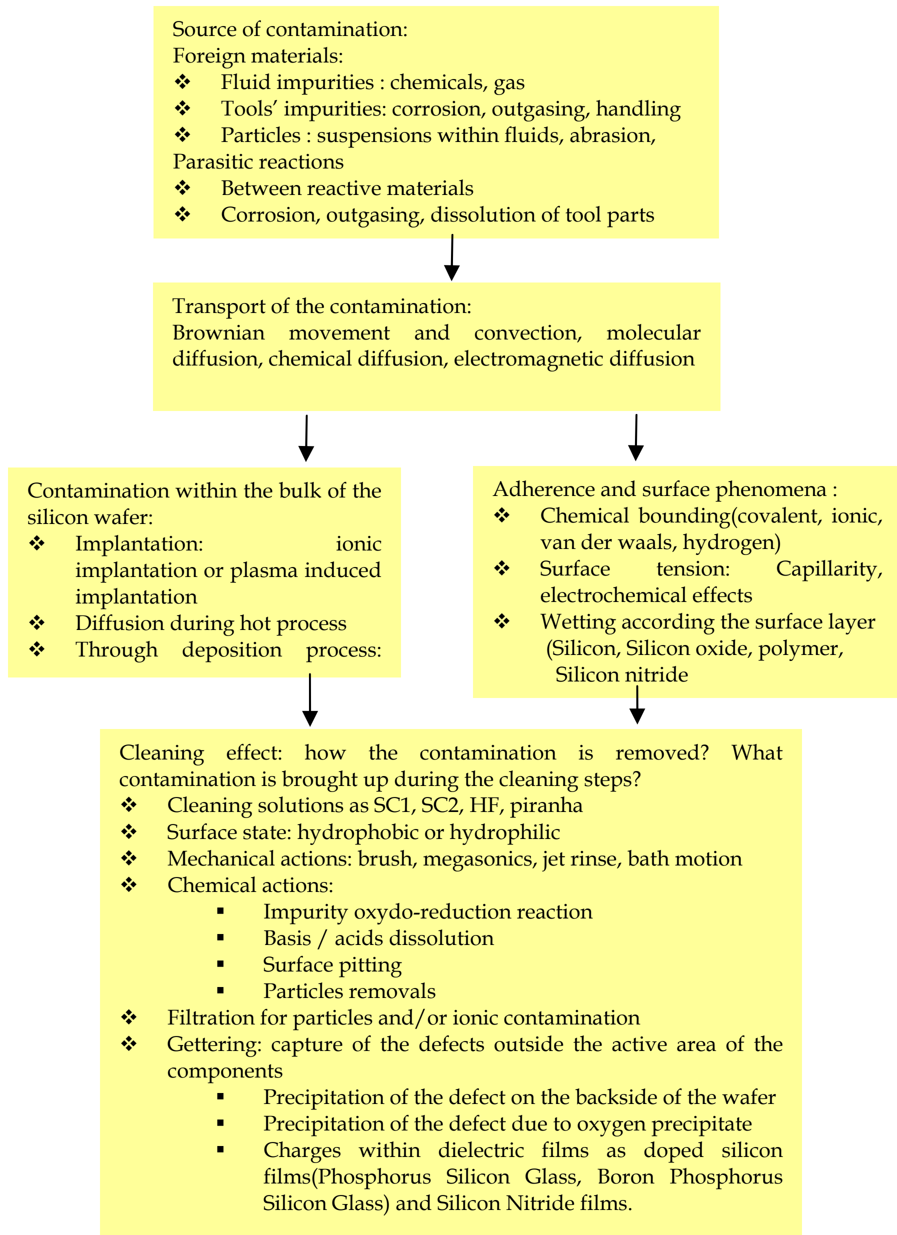


Fig. 1. Contamination workflow: mechanism and questions.

1.2 Contamination impact on wafers

The contamination impacts of the three different contaminants are summarized in table 1

Contamination Classification	Elements	Sources	Wafer effects
Ionic contaminant	Alkaline Na,K	Human pollution Works Chemical and gases	Electrical instability ▪ gate oxide leakage ▪ retention
Ionic contaminant	Transition Metals Ni,Co,Fe, …	Human pollution Works Chemical and gases Networks– tools-process	Gate oxide integrity (GOI) degradation
Ionic contaminant	Dopants Al, P, In, Ga, As, B,…	Process: wet processes, implantation / Works Material out gassing Chemicals and gases	Shift of voltage threshold of the transistor device.
Ionic contaminant & Air molecular contamination	Acids F-, Cl-,CH3COO-,Br-, PO4--,SO4--	Process pollution: etch, wet process, Chemical Vapor Deposition (CVD) Works Material out-gassing Traffic pollution Industrial pollution	Pad corrosion Aluminum corrosion Defectivity on Deep UV (DUV) and Mid UV (MUV) resist Salt deposition on lens, masks, wafers
Ionic contaminant & Air molecular contamination	Bases NH3 Amines	Process pollution: etch, wet process, CVD deposition. Works Material out-gassing Traffic pollution Industrial pollution	Footing on DUV resist Salt deposition on lens, masks, wafers Photolithography activation especially with 193 nm process
Organics	Organics	Process pollution: Wet process and lithography process	Photolithography activation especially with 193 nm process. Eg: contamination with solvent on resist
Particles	Organics	Process Pollution: dry etch polymers, resist strip, wet process, Material out gassing Chemicals and gases	Gate oxide integrity High resistivity contact Deposition on surface, lens degradation Defectivity with opens or shorts on pattern wafers
Particles	inorganic	Process Pollution: dry etch polymers, resist strip, wet process, Material out gassing Chemicals and gases	Gate oxide integrity High resistivity contact Deposition on surface, lens degradation Defectivity with opens or shorts on pattern wafers

Table 1. Description of Contamination source and wafer effects

2. Contamination analysis and monitoring

2.1 Measurement techniques

The analytical techniques for measurements of the different contaminants defined in the table 1 are break down within four categories (Galvez 2006)

- metallic contamination analysis
- Anions impurities analysis with ion chromatography
- Chemical composition analysis as gas chromatography, (GC), Total Organic Compound (TOC) Analyser for Deionized water (DI water)…
- Liquid particle measurement with liquid particle counters for particle size above or equal 0.1 µm diameter for chemicals. Tools for the characterization of the particles size distribution are also interesting, but not in the scope of this presentation.

In this chapter, we focus on metallic contamination in silicon which represents one of the major causes for low yields and poor performance of semiconductor devices. Transition metals in silicon have deleterious effects on device characteristics. Airborne molecular contamination affects key process steps, as gate oxide quality.

Measurement techniques of metallic contamination are divided in two categories:

- Inline measurement technique: direct measurement on the wafer without any sample preparation
- Off line measurement technique: Either the technique, or the sample preparation pre-treatment before measurement, involves the analysis within a laboratory environment.

All these measurement technique have performance defined by parameters as :

- Detection Limit (DL) is the capability to distinguish a signal from the noise of the measurement system. Typically, Signal to Noise Ratio (SNR) is needed to be greater than 3.
- Quantification Limit (QL): It is defined as QL = A x DL, where A is integer number. Its value depends on analytical conditions.
- Surface analysis: the spot size of the analytical technique. Sample preparation as Vapor phase Decomposition (VPD) is able to increase the surface analysis, by etching the contaminants at the surface of the silicon wafer or within the bulk of the oxide film deposited at the surface of a wafer. Then the droplet is either used for analysis on ICP-MS measurement, either dried for TXRF measurement
- Probing depth of the analytical method: the volume of material probed during the analysis
- Time response: delay between the sampling and the analytical response. It depends on the sensitivity requested, as Quantification Limit can be improved by accumulation or concentration steps, the measurement time is increasing.
- Analytical coverage: metallic elements which are detected.

Sample Preparation as VPD is pushing detection limit by one to two order of magnitude according elements, but it has a clear impact on the time response. A compromise has to be found between the different parameters.

The in line measurement techniques are surface analysis as EDX or TXRF or SPV described in table 2. The off-line measurement techniques are installed within laboratory. Surface, film or bulk characterizations can be run on different surface analysis tool as Atomic absorption Spectroscopy (AAS), VPD-TXRF (a tool available for manufacturing environment is already available) , VPD ICPMS, SIMS, Auger, XPS. It is described in table 3 and 4.

In Line Measurement technique	EDX	SPV	TRXF
Physical Principle	Energy Dispersive X-ray Spectroscopy: X Ray of elements contained within samples	Measurement of minority carrier diffusion length linked to lifetime	X-Ray fluorescence of elements at the surface of the sample after excitation with X ray at a grazing angle
Impact on sample of the measurement	None, not destructive	None, not destructive	None, not destructive
Surface analysis	Few nm	1 mm	1 cm2
Probing depth	10E2 to 10E4 nm	10 – 150 µm	1 nm
Analytical coverage	Elements after Na within periodic table	All metals electrically active in bulk All charge in the silicon oxide	Elements after Na within periodic table
Detection limit	Qualitative results as main compounds of particles until composition of one percent, are identified	5 E9 At/cm3	Fe : 5E9 At/cm2
Sample characteristics	Bare wafer/ patterned wafers Need localization of particles for composition characteristics	Bare wafer But need activation. Fe can be identified if measurement pre and post anneal is done	Bare wafer
Results	X ray spectrum of elements contains within the material	Diffusion length, not qualitative except on Fe with P substrate Points/Mapping	Surface concentration Points/ Mapping

Table 2. parameters description of metallic measurement with in line techniques

IC : Ion Chromatography
TXRF : Total X-ray Reflection Fluorescence
SPV : Surface Photo Voltage analysis
AAS : Atomic Absorption Spectroscopy
ICP MS : Inductively Coupled Plasma Mass Spectroscopy
VPD TXRF : Vapour Phase Decomposition TXRF
VPD ICP MS : Vapour Phase Decomposition ICP MS
ppb : part per billion typically ng/g for metallic impurities in chemicals
ppt : part per billion typically pg/g for metallic impurities in chemicals

Off Line Measurement technique	IC	AAS	ICP MS	VPD TXRF	VPD-ICPMS
Physical Principle	Variable Retention Time of anions on column	Wavelength absorption specific according elements	Mass Spectrometer coupled to an Inductively Coupled Plasma source	Same as TXRF with VPD preparation for integration of the surface of the wafer	Same as ICPMS with VPD preparation for integration of the surface of the wafer
Impact on sample of the measurement	Destructive as the liquid containing the liquid is analyzed	Destructive as the liquid containing the metallic elements is analyzed	Destructive as the liquid containing the metallic elements is analyzed	Destructive as the liquid containing the metallic elements is analyzed	Destructive as the liquid containing the metallic elements is analyzed
Surface analysis	sample preparation	sample preparation	sample preparation	Bare wafer	Bare wafer
Probing depth	None	None	None	1 nm to 1 µm	1 nm to 1 µm
Analytical coverage	Anions: F-,Cl-, NO3-,PO4--, and acetate	All elements, mainly Alkaline as Na,K	All elements within periodic elements	Elements after Na within periodic table	All elements within periodic elements
Detection limit	Few ppt depending on sample preparation	Few ppt depending on sample preparation	Few ppt depending on sample preparation	Fe: 10E7 At/cm2	Fe: 10E7 At/cm2
Sample characteristics	Chemicals, extraction from materials Air Molecular Contamination	Chemicals, sample preparation needed with matrix removal for better sensitivity	Chemicals, sample preparation needed with matrix removal for better sensitivity	Bare wafer with native oxide or thicker oxide with sample preparation by HF Vapors dissolution of Silicon dioxide	Bare wafer with native oxide or thicker oxide with sample preparation by HF vapors dissolution of Silicon dioxide
Results	Concentration of contaminants within solution in ppt or ppb	Concentration of contaminants within solution in ppt or ppb	Concentration of contaminants within solution in ppt or ppb	Average value of metallic contamination on wafer	Average value of metallic contamination on wafer

Table 3. parameters description of metallic measurement with off line techniques part 1

Off Line Measurement technique	SIMS	XPS	Auger
Physical Principle	Ar Sputtering and Ionization of Species within Sample, Mass analyzer	X Ray photoelectron spectroscopy of chemical compounds, bounding of species impacts response	Auger electron emission characteristic of the species within the sample.
Impact on sample of the measurement	Destructive as sputtering of Sample	Not always destructive	Not always destructive
Surface analysis	> 10 µm2	15 µm	8 nm spot size
Probing depth	20 nm to 10 µm	0.4 to 10 nm. Sputtering of the sample is also possible for profiling	0.4 to 10 nm. Sputtering of the sample is also possible for profiling
Analytical coverage	All	All	All
Detection limit	sensitivity changes according to elements : ppb range to ppm	>0.5 % atomic weight	>0.5 % atomic weight
Sample characteristics	Bare wafers with implants, films or patterned wafers if specific macros are forecast, Small samples	Bare/patterned wafers/small sample (KLA file recognition)	Bare/patterned wafers/small sample
Results	Elemental, quantification with standard.	Point or Surface or Elemental composition, chemical maps Chemical state for bounding between elements	Point or Surface or Elemental composition, chemical maps,

Table 4. parameters description of metallic measurement with off line techniques part 2

SIMS : Secondary Ion Mass Spectroscopy
XPS : X-ray Photoelectron Spectroscopy
ppm : part per million, typically µg/g

2.2 monitoring of Main topics: AMC, Chemicals

2.2.1 AMC

Air Molecular Contamination monitoring scheme is based on collection of contamination on beakers, bubblers or directly on wafers. The measurements are then done by IC, or TXRF for measurement on the wafer. The time of collection will be able to enhance the sensitivity. A deposition rate is then calculated.

ITEMS	AMC Monitoring (Molecular acids, bases)	Parameter value
AMC monitoring	Frequency	1/4 weeks
	Method	beakers
	Sampling time	22h
	Analytical Method	IC for beakers TXRF for wafers
	Method	beakers
		Impinger
		deposition rate on bare wafers
control limit unit - pptM (Part Per trillion molar)	F-	1200
	Cl-	400
	NO3-	1900
	NO4-	1400
	PO4(3-)	900
	SO4 (2-)	900
	NH4+ (ppbM)	0.16

Table 5. Description of AMC monitoring

NH4+ has a specific monitoring for litho tools. For example in table 6, results for different location and Litho Tool set show that the value is greater than the action limit. Then the tool is stopped and root cause analyses are done. The measurements have been done with an Ion Chromatography (IC) by Balazs laboratory from Air Liquide Electronics Europe.

Location	[NH4+] in ppbM measured by IC
MUV Tool A	12,80
DUV Tool A	0,55
DUV Tool B	0,85
DUV Tool C	1,60
Clean Room 1	3,05
DUV Tool D	0,28
MUV	< QL
QL in ppb M	0.16

Table 6. Measurement of [NH4+] in different locations

2.2.2 Chemicals

Quality of chemicals and Ultra pure water monitoring depends on the flow of the chemicals through the chemical supply, from the tank to the wafer. For Chemicals, the sampling can be done at the delivery of the products before the central chemical supply (in incoming inspection): the Point of Entry (POE). It can also be done on the process tool, at the point of Use (POU). Chemicals at the POE can be measured by ICPMS. At POU, bare wafers which are processed with a complete recipeare then measured by TXRF. At POU another approach is the sampling of chemicals at POU ICPMS analysis. Results at POE and POU measured by ICPMS are presented in Table 7.

Elements	Element	QL in ppt	Ammonia POE A Tank 1	Ammonia POE A Tank 1	H2O2 POE B	POU SC1 in tool bath	Spécification POE and POU
Sodium	Na	5	17	40	121	63	1000 ppt
Magnesium	Mg	5	12	6	24	NA	1000 ppt
Aluminium	Al	5	62	7	35	66	1000 ppt
Potassium	K	5	12	47	16	NA	1000 ppt
Calcium	Ca	5	41	56	113	93	1000 ppt
Chrome	Cr	5	< QL	< QL	6	< QL	1000 ppt
Manganése	Mn	5	< QL	< QL	< QL	NA	1000 ppt
Fer	Fe	5	7	9	59	53	1000 ppt
Nickel	Ni	5	13	10	< QL	< QL	1000 ppt
Cobalt	Co	5	< QL	< QL	< QL	NA	1000 ppt
Copper	Cu	5	< QL	8	< QL	< QL	1000 ppt
Zinc	Zn	5	< QL	16	17	< QL	1000 ppt
Argent	Ag	5	< QL	< QL	< QL	NA	1000 ppt
Plomb	Pb	5	< QL	< QL	8	NA	1000 ppt

NA: Not analysed / **ppt** : part per trillion, typically pg/g for metallic contamination.

Table 7. Metallic measurements on chemicals at POE and POU

The measurements have been done with an ICPMS by Balazs laboratory from Air Liquide Electronics Europe.

2.3 Sampling and confidence level on monitoring scheme

Monitoring of the semiconductor manufacturing line is done on the product wafers, or on the facilities as ultra pure water, chemicals or gases. Measurements on a product wafer can address impact of metallic contamination on gate oxide from hot, implant processes.

The question related to sampling is “why do we need to monitor defect?” In the case of metallic contamination, it is not such easy. Metallic effects are known, but the analytical tools have time response much slower than for the defect density tools. Then, the monitoring scheme of metallic contamination needs to be think according pragmatic approach. First the line is divided in two parts:

- Front End Of Line : Device construction
- Back End Of Line : Connection with metal line

TXRF, VPD TXRF and SPV measurement technique are used for standard monitoring, but also after maintenance procedure, or any troubleshooting. Decision tree and clear instruction are also needed in order to help manufacturing running the tool properly.
In addition the monitoring of the chemicals, Gas and DI Water before the POU is indicating the quality level of the facilities. This monitoring scheme is summarized in table 8.

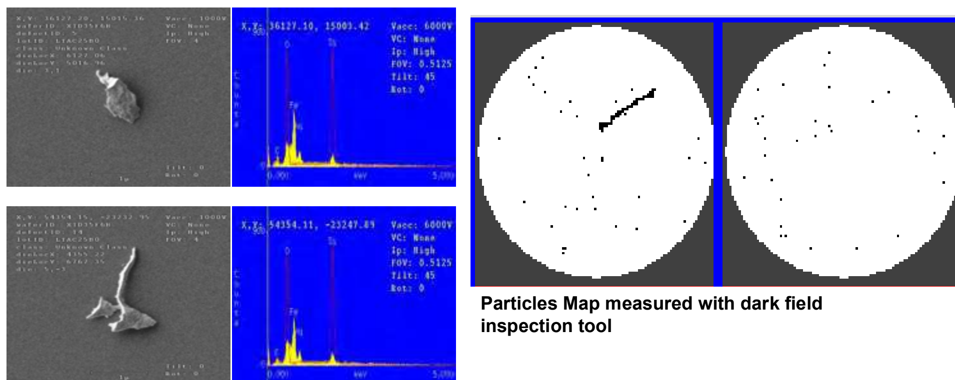
Items	Monitoring	Analytical Tool	Frequency	Process Tool Facilities
FEOL	Standard	SPV TXRF VPD TXRF	Periodic according risk	All, Wet tool, Hot process…
BEOL	Troubleshooting	SPV TXRF VPD TXRF VPD ICP MS	Define within action plan	All, Wet tool, Hot process, Etch…
BEOL	Standard	SPV TXRF VPD TXRF	Periodic according risk	Wet process Cleaning tool
BEOL	Troubleshooting	SPV TXRF VPD TXRF VPD ICP MS	Define within action plan	Wet process Cleaning tool
Chemicals	Standard	ICP MS TXRF	Audit mode	Chemical supply
Chemicals	Troubleshooting	ICP MS VPD ICPMS TXRF VPD TXRF	Define within action plan	Chemical supply
AMC	Standard	IC	Periodic according risk	Clean Room
AMC	Troubleshooting	IC	Define within action plan	Clean Room

Table 8. Monitoring scheme of metallic contamination

3. Impact of metallic contamination through examples

3.1 Metallic in wet chemistry

On a cleaning tool working with continuous flow chemistry process (Sanogo 2008), vibrations have loosened a screw which was maintaining the Vessel as shown in Fig 2. This has been dissolved by the different chemistry of the cleaning process SC1, SC2, HF, before Gate oxide growth. Monitoring measurement with dark field inspection tool on product wafers has identified particles. EDX analysis on these particles has identified Fe and Ni compounds



Particles localized with Dark Field inspection tool and EDX spectrum : Fe, Ni elements identified

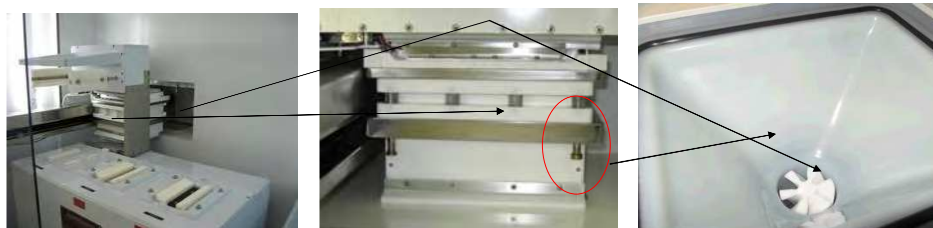
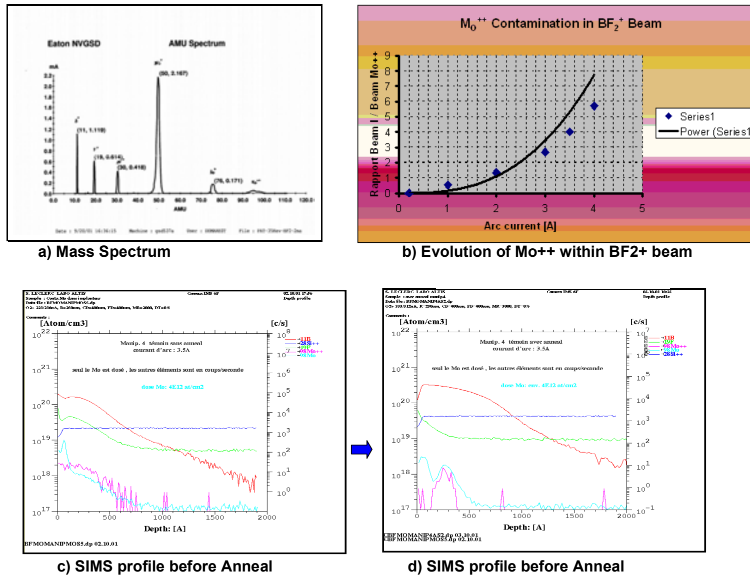


Fig. 2. Metallic contamination on Wet process tool, EDX identification

3.2 Metallic in Implant Process

For an Ionic Implant Tool, the plasma is generated within an Arc chamber in order to do the ionisation of the different species before going trough the mass spectrometer filter for implantation on the wafer. The wall of this Arc chamber can be made within two metals, either Molybdenum, either Tungsten. During the implantation of the BF2 species for the device channel implant, Mo++ has been implanted with BF2 implant (Demarest 2009). For information, AMU of BF2 is 49, and the isotopic value of Mo ++ around AMU 49 is
AMU = 48,5 ==> $^{97}Mo^{++}$ =9,5% and AMU = 49 ==>^{98} Mo^{++}= 24,4%.
W wall material is double cost compared to Mo. The concentration of molybdenum within the bulk has been measured with SIMS technique. The quantity of molybdenum is increasing with higher current as it is needed for increasing implantation doses.



a) Mass Spectrum b) Evolution of Mo++ within BF2+ beam

c) SIMS profile before Anneal d) SIMS profile before Anneal

Fig. 3. Mo Contamination Within Wafer during BF2 implant

3.3 Furnace Contamination

The monitoring of Furnace oxidation process with SPV has been evaluated to catch Na contamination in case the handling procedure would not be followed. In Fig 4, the trace of the finger touching the wafer through gloves is detected (Garroux 2005)

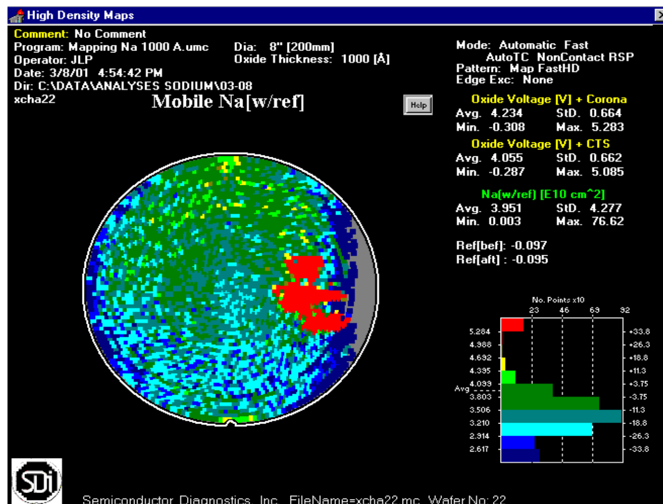


Fig. 4. SPV measurement on bare wafer post oxidation.

4. Defect density on product wafers

Defect density is one of the main detractors of the final test yield in semi-conductor manufacturing, and the impact of the particles on the device functionality is even more critical for sub-micron designs. It is the reason why the investment for defect density measurement increased for the last years: yield prediction through in-line defect inspection is requested to improve yield learning on new product and each node generation.
In this chapter, we will describe the latest tool set available in the manufacturing lines and the detection capabilities of the bright field, dark field and SEM (Scanning Electron Microscope) inspection tools and optical / SEM review tools. The sampling strategy for the defect review and the automatic defect binning are optimised to improve the classification of the defects of interest.
Defect classification accuracy and the defect size influence on chip functionality will be presented through the critical area definition and die to die yield calculation. The methodology for yield prediction through defect density inspection and classification will be described. The confidence level of yield prediction depends on the inspection tool capabilities and sampling strategy, the defect size and killer ratio calculation for each defect type.

4.1 Defect inspection

3 types of inspection tools on product wafers are proposed for defect density analysis:
- Bright field inspection tools: using standard light or UV light for sub micron design inspection. Sensitive to image differences, detect deformed designs as micro masking, embedded or surface foreign materials, scratches, mainly defects providing a good image contrast.
- Dark field inspection tool: using a laser, will detect easily surface defects. Tools covering both dark and bright field inspections mode are now available.
- Scanning Electron Microscope (SEM) inspection tool. This tool compares SEM images to detect small defects (0.1 µm), charge contrast defects (as contact open, line shorts, device leakages), or defects in high aspect ratio structures (Baltzinger et al., 2004; Hong Xiao et al, 2009).

These tools will compare images from one die to an adjacent one. If any difference is detected, the tool will check the image with another die. The die different compared to the other will be considered as defective. For memory products, the sensitivity and throughput of the tool can be improved by comparison of memory blocks inside of the dies. The inspection tools provide defect coordinates on a wafer map. Some tools are able to classify the defects to facilitate the defect density analysis. The sampling for defect analysis review can be more efficient by removing non killer defects, nuisances, detected and classified by the inspection tool.
The choice of one of these tools is driven by the in-line inspection strategy. This strategy is built with the following information:

- Pareto of the defects to be detected
- Information of the final test analysis and failure analysis.
- Manufacturability of the in-line controls (scan time, resources for classification)

Today's recipes are generally 100 % surface scan of the chip to inspect exhaustively all of the active structures of the product. It allows the detection of all type of defects on the different

structures of the chip, but sensitivity of the inspection tools in the array is reduced with random mode inspection. Defect size distribution depends on image filtering, detection threshold, pixel (smallest image size for die comparison) chosen in the recipe. These parameters are adjusted to keep a count of defects affordable for manufacturing inspection. So, the recipe will be built to avoid encroaching and saturation concerns. Focus parameter will be adjusted to catch surface or embedded defects. An example of a defect size distribution is given in the Fig. 5.

General law for the defect distribution is: $D=A/X^n$ (1)

With:

- X is the defect size
- D is the particle count
- A and n are constants (n used to be closed to the value of 3)

A log/log graph will give a straight line where the slope is n.

After wafer inspection, defect map and chip yield is provided. The chip yield or defect count depends on the sensitivity of the recipe. In the case of the previous graph most of defects under 0.3 µm are not detected by the KLA 2135 using the pixel 0.39 µm (random mode). Using the pixel of 0.25 µm allows the detection of defect size of 0.18 µm, but will increase the total of the detected defects on the wafer.

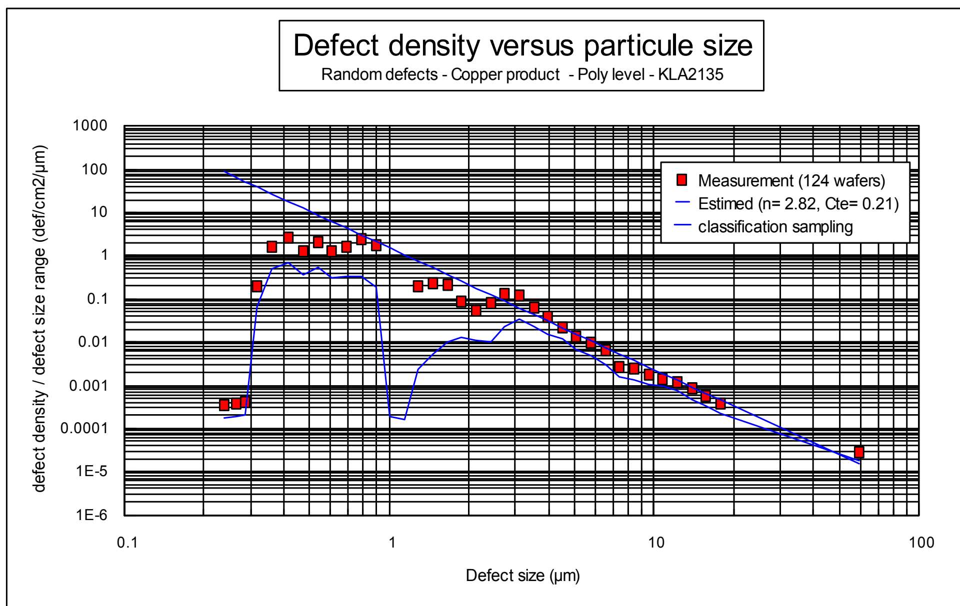


Fig. 5. defect size distribution on 0.18 µm technology

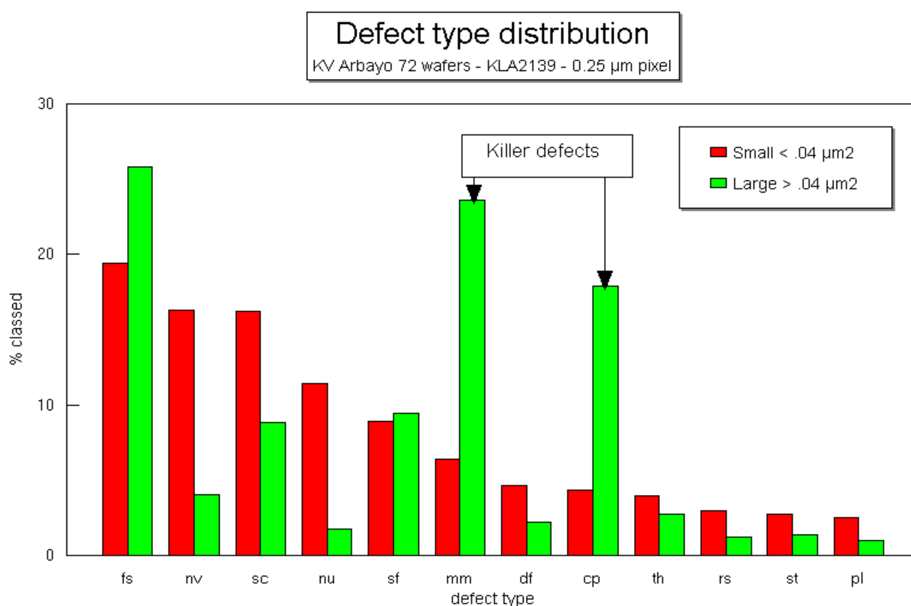


Fig. 6. Ratio of classified defects, comparison with 2 inspection recipes: the killer defects (MM, micro masking and CP, silicon pitting) are under sampled using 0.25 µm inspection recipe (red bars), which detect small defects (under 0.04 µm²), compared to the 0.39 µm recipe (green bars).

The aim of the defect inspection is to detect most of the killer defects. The recipes using smaller pixel size will grow the total defect count mainly with small defects (Fig. 6), which are not the main detractors at final test yield. This will enlarge the width of the defect size distribution and could cause the lost of the defects of interest review. It is the reason why inspection tools are providing today a previous rough binning to improve the efficiency of the defect classification sampling and the review.

4.2 Defect review

Defect review is required to identify defects of interest and to address the root cause of each defect type. The defect review is processed using 2 types of tools:

- Optical review allows the classification of large defects (more than 1 µm). The benefit of optical review is to get pictures of embedded defects. Confocal microscopes provide topological information.
- SEM review allows the classification of smaller defects, but embedded defects will not be systematically redetected, because SEM is sensitive to the surface only. Last generation of review SEM is able to redetect, focus and take automatically a picture of the defects, to improve the throughput of the review. EDS (Energy Dispersive Spectroscopy) can be added to have elemental analysis of particles.

4.3 Defect sampling strategy for defect classification

All the detected defects are not reviewed on optical or SEM tools because the amount of the defect is generally too high for the review tool capacity. So a sampling is applied on the total inspected defects, with the following possible methodologies:

- remove previous inspected layers defects to classify only current level defects
- take only 2 or 3 images of large defects (clusters)
- classify randomly failing dies
- classify largest defects to improve sampling of killer defects
- classify a sampling of proposed the defects binned by the inspection tool

Sampled defects will be automatically classified (ADC: Automatic Defect Classification proposed for SEM or Optical review tools) or manually classified with an operator. The SEM review is more accurate due to its better resolution, but is not able to detect some embedded defects. The measurement of the efficiency of the defect classification (ADC for this example) is given by the following 2 parameters (Chen-Ting Lin et al., 2001):

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Accuracy = Total correctly classified by ADC/ Total classified by the expert (2)

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Purity = Total correctly classified by ADC / Total classified by ADC (3)

Accuracy gives the capability of the classifier to detect a given defect type. Purity gives a measurement of the "noise" of the classification. ADC classification goal is to obtain in general more than 80 % for accuracy and purity. A trained operator achieves more than 90 %. Defined defects classes provided to ADC or an operator has to be consistent with:

- Process root causes of the defect
- Size and possible impact of the defect at final test
- Defect should be easily recognizable by ADC or an operator to get good level of accuracy and purity

4.4 Final test yield prediction from in-line defect inspection data

PLY (Photo Limited Yield) calculation from in-line wafer inspection and defect classification will provide an estimated final test yield of a wafer. The PLY calculation for the defect j for one inspected level is the following (semi-deterministic model):

$$PLY_j = 100*(1 - P_j * C_j * DC / NTC) \quad (4)$$

Where :

P_j : probability of fail of the defect j
C_j : chips classified with the defect j
DC : total defective dies
NTC : total dies on the wafer

PLY of one inspection level is the product of PLY_j of the j defects classified on the wafer. The overall estimated yield is the product of PLY of the inspected levels. The aim of the following part is to discuss about the reliability, the accuracy and the precision of the PLY data. When PLY trend degradation is observed, we need to know the accuracy of the measure and the assumptions taking in account in the calculation to be sure that what is measured is a real process concern.

Probability of fail calculation

When a defect is classified, a probability of fail is associated, depending on the impact of this defect on the chip functionality. Different methods are used for the calculation of this killer ratio. The most frequently used is STPLY (Statistical Test PLY). It is a chip to chip correlation, between failing chips seen with the in line inspection tools and the final test yield (Grolier, 2000). For a given defect type i, the calculated killer factor is:

$$\text{Killer factor} = \text{final test failing chip with the defect i} / \text{total defect i found} \quad (5)$$

Some error on the calculation can be done, because some killer defects not detected with in line inspection tools can match with detected defects without any electrical impact. Some "noise" subtraction is proposed. STPLY allows the probability of fail calculation of all types of semiconductors, memories and logics.

Another method called ETPLY (Electronic Test PLY) is to overlay the PLY defects map and the bit fail map given by the final test of the memory products. This method of killer factor calculation allows a better accuracy than the previous method because there is very few of "random hits", even with an overlay specification of 100 µm. Nevertheless, this method is only applicable for memories (Fig. 7).

The manual classification does not report accurately the size and the impact of the defect on the design. Some classification like small embedded, embedded and large embedded are dependant on the operator; large embedded with a killer factor of 1 is a given size defect or a defect connecting 2 structures. Some defect codes have a killer factor of 0, as Nuisance, Non visible, Discoloration, Fill Shape (Defect in non electrically active area). to give the most accurate predicted yield. The inspection recipes have to be optimised to reduce the amount of such defects. Nevertheless, the size of the defect has a strong impact on the killer ratio (Fig. 8), and the interaction between defect size and product design has been studied to estimate the impact of the defect density on final test yield.

Fig. 7. Bit fail map correlation (electrical fails are green rectangles) with physical defect detected on KLA 2135 post copper CMP Metal 2 and Metal 3

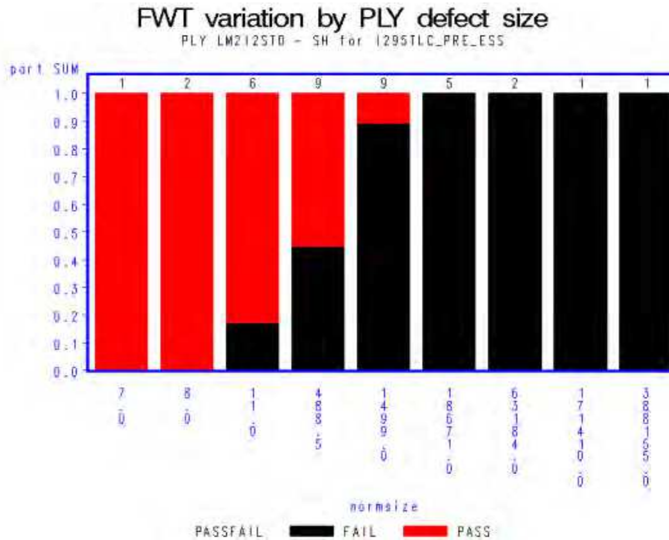

Fig. 8. killer ratio calculation by size (normsize , in µm²) given by STPLY method.

Defect impact on the product: critical area definition

For a given defect density yield models are able to propose a corresponding yield calculation as binomial, Poisson laws (Fig. 9). Nevertheless, these laws are not taking in account the product complexity and device redundancies (Donovan, R. P., 1988). Some corrective factor can be added to improve the predicted yield, but the more precise estimation can be given by software including the design descriptions for all the layers of the product and the modelization of the defect density.

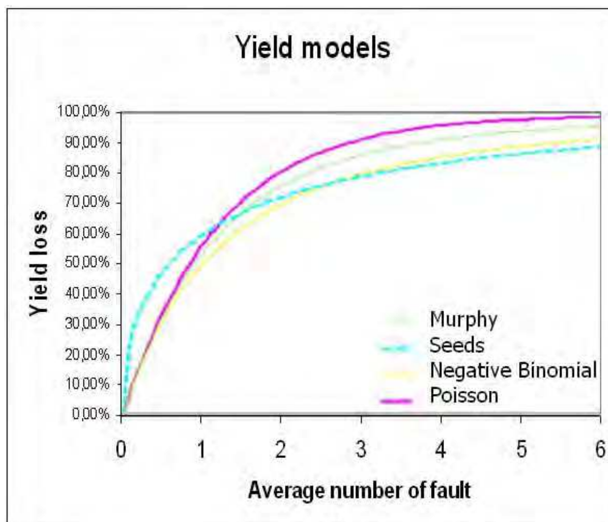

Fig. 9. Yield calculation from different models

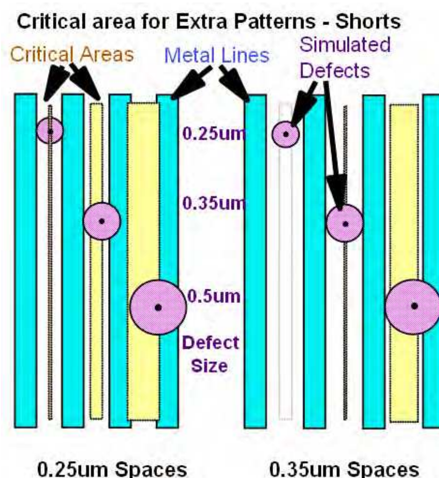

Fig. 10. Blue bars are metal lines. Critical area is the yellow surface. If the centre of a circle particle is inside the yellow surface, the particle will cause a fail (metal short).

This final test yield estimation is based on the critical area calculation (Fig.10). The critical area is the surface where the centre of a particle will cause a failure (Barberan & Duvivier , 1996). The critical area depends on the particle size, the product design and the impact of the particle on the design. As all these information are available, yield estimation can be calculated (Allan & Walton , 1996) with the following law (Fig. 11):

$$Y_{\text{event}} = \exp\left(-\int_{x_0}^{\infty} \mathrm{CA}_{\text{event},i}(x)\mathrm{DSD}_i(x)dx \right)$$

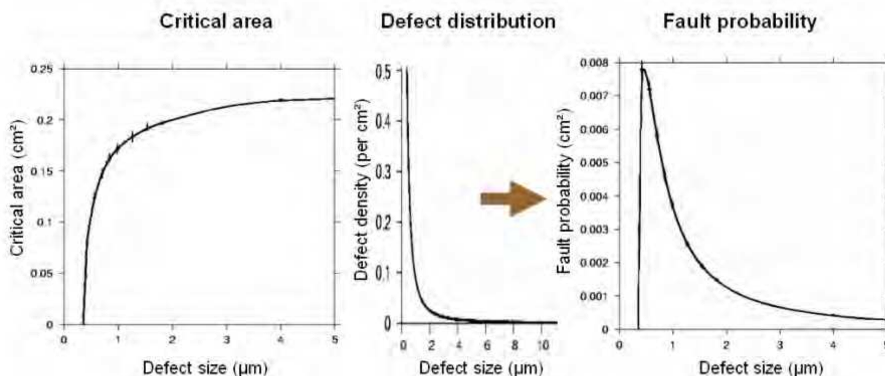

Fig. 11. Defect density $\mathrm{DSD}_i(x)$ and Critical area $\mathrm{CA}_{\text{event},i}(x)$ of a given size x defect will provide a yield loss $Y_{\text{event},i}$ corresponding to the surface under the fault probability curve.

Most critical part of the product design or layers can be highlighted and corrected to improve final test yield (Fig. 12). Redundancies as contacts can also be added.

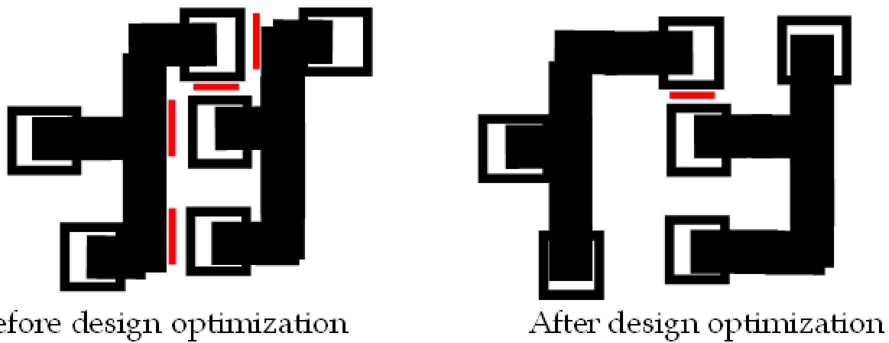

Fig. 12. Critical area reduction with design optimisation

Wafer / lot / defect sampling

The PLY result depends on the sampling strategy. The more defects are classified; the better will be the confidence level on PLY data. This can be modelized with a binomial law (see Fig. 13) as far as we suppose that a defect frequency follows a Gaussian distribution (6):

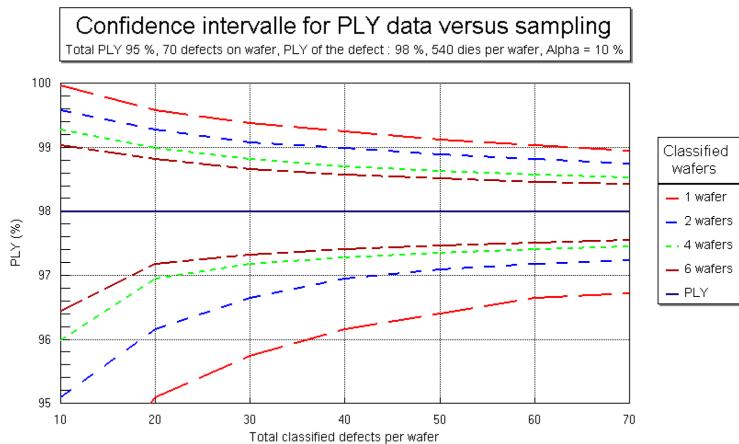

Fig. 13. confidence level of PLY data depending on the defect sampling

In this case, the cumulated wafers data are supposed to have the same defect distribution. This is consistent with the simulation of different defect sampling proposed in 1997 by J-L. Grolier and J. Combronde.

Actual sampling is 25 % of the production lot, 2 wafers per lot, and 50 classified defects maximum per wafers, according to the previous study. At this time, some tool are proposed to define the best sampling depending on amount of defect type, the stability of the process and the required confidence level.

To improve the sampling efficiency and PLY results accuracy, the recipes have to be optimised to reduce the amount of prior level defects, nuisances and non visible defects (false defects ...). Inspection level detection is chosen to detect killer defects. Generally post

STI (silicon trench Isolation) module, PC (poly gate etch), Contact, metal layers are the most common level used for inspection.

Predicted Final Test Yield

At the end, overall PLY calculated with the final test date for each lot will give a prediction of the final test yield induced by the defect density (PLY = multiplication of all the defects yields for all the levels of inspection). The following graph shows the overall PLY calculated at final test and the final test results week by week (Fig. 10). Some errors induced by the overall PLY calculation can occur when lots are not crossing the process flow at the same time. Process issues (CD variations, resistive vias ...) will be estimated with another calculation to give a better final test yield prediction.

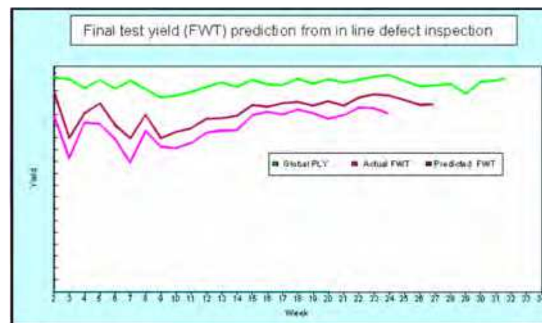

Fig. 14. PLY to Final test yield correlation week by week. PLY was able to detect the down trend weeks 3 and 7, and the yield improvement starting week 10.

Conclusion: Overall PLY accuracy

To get an overall PLY accuracy estimation, killer factors calculated each month with SPLY method can be reported on a graph. A sigma can be estimated for each defect type, as a critical process parameter of the line. In general, the higher killer factors have a lower standard deviation for a given probability of fail calculation (Baltzinger, 2009). For the low killer factor defects, the "noise" impact on the calculation is higher. In this case, the defect density engineer has to understand the root cause of this high variability to improve the level of confidence:

- Inspection recipes
- Sampling and classification accuracy
- Process changes

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