

# Intelligent Communication Module for Wireless Biosensor Networks

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## 1. Introduction

Technological advancement, miniaturisation of electronic devices and progress in ad-hoc network routing protocols and embedded systems have facilitated developments in the field of biosensors and biosensor networks. Biosensor networks are a collection of biosensor units that collect information about biological responses and process it in order to make a decision for a desired outcome. In today's market there is a demand for ultra low power consumption, portability and wireless connectivity from the biosensors for information exchange. This chapter introduces a new paradigm of biosensors which have processing capability with an intelligent and adaptive wireless communication module. The adaptive communication module efficiently reconfigures its hardware components according to the changes in operating environment in order to reduce system power consumption and optimally utilise resources. Due to the intelligent wireless communication module, the biosensor unit becomes a state of the art independent system as well as part of a wireless biosensor network (WBSN).

The WBSNs find applications in areas such as medical parameter monitoring, environmental monitoring, chemical/biological detection, food and water analysis, soil monitoring, security and safety. These applications of the WBSNs potentially cover the current market trends and will significantly contribute to benefits of technological advancement for the community.

The chapter is structured as follows. Section 2 presents intelligent biosensor node, its functionality and design requirements. It also discusses the remote patient monitoring application and lists potential applications of WBSNs. Section 3 proposes to use Ultra Wideband (UWB) impulse radio as a communication module for biosensor nodes. It also discusses the potential problems and possible solutions for the use of UWB impulse radio architecture for biosensor node. Digital UWB impulse radio architecture suitable for biosensors is described in section 4. Section 5 discusses the parallelism requirement analysis, proposes real time reconfigurability algorithm (RTRA) and discusses its design requirements. Section 6 presents the design and implementation of the RTRA. Conclusions are drawn in section 7 followed by references in section 8.

## 2. Wireless biosensor network and applications

A wireless biosensor network consists of a number of biosensor nodes having the capability of communicating with each other in an adhoc network, collecting data, sending them to a

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sink/base station (gateway) and receiving instructions from the sink/base station via a wireless network. The WBSN applications require low to medium data communication rates ranging from a few hundreds of Kbps to a few Mbps over a distance range of 10-30m and are categorized under IEEE 802.15.4a standard for wireless sensor networks (IEEE, 2009). A typical wireless biosensor network scenario is presented in Fig. 1 (a).

A modern biosensor node as presented in Fig. 1 (b) consists of a biosensor unit to sense the biological parameters and convert them into equivalent electric quantities. The low power digital signal processing unit analyses these signal and takes decisions according to the application and conditions. The radio block provides the wireless link for communication between the biosensor node and the central base station as well as other biosensor nodes. Information such as the current parameter measurement, the biosensor status and decisions taken are communicated between the biosensors and central base station. In the modern adhoc WBSNs, the decisions taken by a biosensor node are also dependent on this data communication and condition of the network as a whole. The actuator unit is commanded as per the decisions taken to take various actions.

With the above functionality requirements from the various components of the WBSN, ultra low power consumption is the most critical design requirement as the biosensor nodes are battery operated. Every component of the WBSN node has to be designed for low power consumption as it directly affects the system reliability, efficiency and life. In a typical intelligent biosensor node which comprises of a sensing element, signal conditioning circuits, a processing element and a transceiver for communication, more than 50% of power is consumed by the transceiver, of which 80% is consumed by the receiver section (Karl & Willig, 2003). This makes the design of the communication module and its receiver section very critical for WBSN applications.

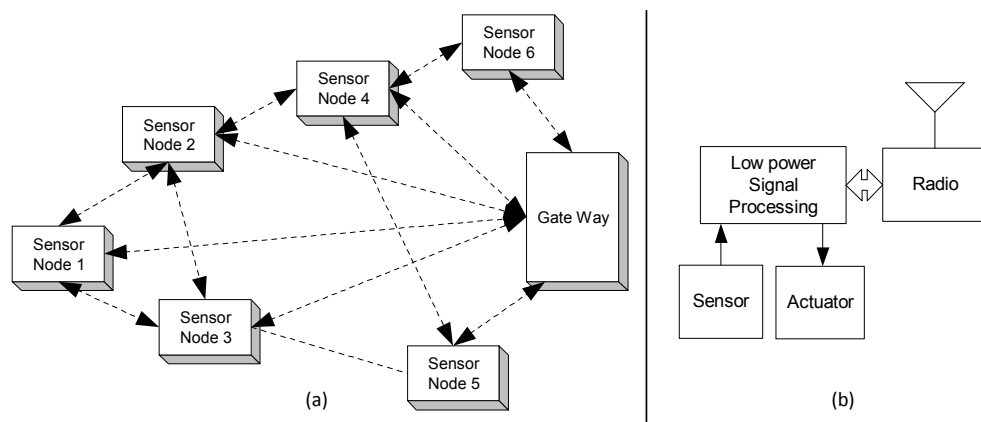


Fig. 1. (a) Typical wireless sensor network scenario (b) Sensor node block diagram

The potential of the biosensor node to sense, communicate, process and act in a WBSN represent a new paradigm for extracting data from the environment and enable reliable monitoring and networking for variety of applications. One of the promising areas of WBSN application is the remote patient monitoring and health care. In this application wearable or implanted miniature biosensors monitor different medical parameters such as heart beat, blood pressure, blood sugar level etc. The data from each body sensor is obtained and sent

over a low data rate wireless link to the central data collection unit at regular intervals of time. This data is then collectively sent for examination via internet or any other long range communication method to remotely placed hospital or medical practitioners. The data is analysed and suggestion can be made regarding medications or the actions to be taken by the medical practitioner. Fig. 2 presents a typical WBSN application scenario for remote patient monitoring.

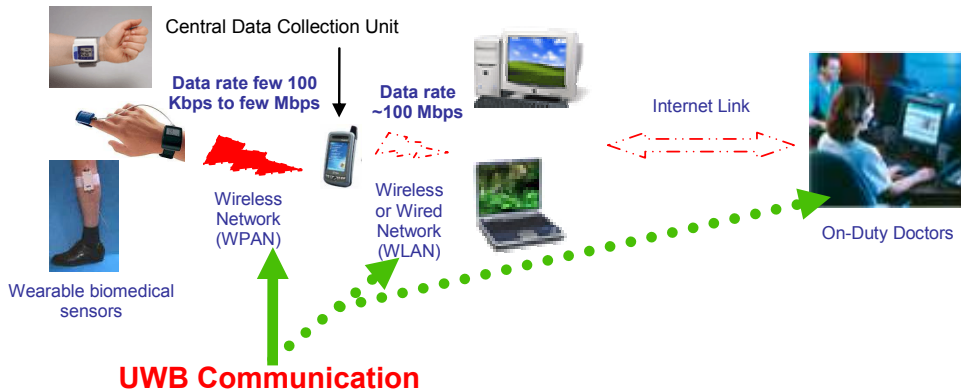


Fig. 2. WBSN application for remote patient monitoring

The remote patient monitoring system will result in a significant reduction in the medical costs, time and efforts, both for patient as well as the medical practitioner. It will improve the efficiency of the medical system and contribute to community wellbeing. Also, it has the potential of low cost implementation and reusability.

In this chapter we propose to use UWB radio for the communication module, as presented in Fig. 2, in the biosensor node due to its low power design and communication potentials which will be discussed in the next section. In addition to the remote patient monitoring system WBSNs with UWB connectivity find applications in a wide range of areas such as:

- Soil monitoring and smart irrigation, which will improve the efficiency of the agriculture industry and save large amounts of water;
- Real time data collection/monitoring for marine and coral research. These WBSNs can be extended to monitor changes in the marine activities and predict unusual weather patterns; and
- Safety of firemen and workers working in extreme conditions by installing bodily biosensors that sense different parameters and communicate to the central unit.

### 3. Ultra wideband radio as a communication module for WBSN

Low power design of a communication module in a WBSN is very critical due to battery operation. At the same time reliable communication, reusability of components and design flexibility are also important factors. UWB technology can be efficiently employed for the communication module in wireless biosensor nodes because of the following features:

- Capability to achieve data rates of few hundreds of Kbps to a few Mbps at 10-30m distance ranges;
- Wide bandwidth of over 8GHz; from 0 - 960MHz and 3.1 - 10.6GHz;
- Unlicensed communication with limited transmit power in above bands

- Potential for location tracking and precision ranging; and
- System-on-Chip implementation of radio facilitating ultra low power digital design, flexibility and scalability (Porcino & Hirt, 2003).

Digital UWB impulse radio proposed in (O'Donnell & Brodersen, 2005), is one of the most suitable architectures for achieving low data communication rates and potentially low power implementation for WBSNs as it is a carrierless communication scheme that reduces analog circuitry in the receiver. The possibility of digital implementation of the UWB impulse radio provides a potential to achieve low power design. However, due to the channel uncertainties, changes in the channel conditions, low transmit power and pulsed nature of UWB communication the digital UWB impulse receiver architectures use significant parallel hardware to ensure correct operation in these conditions. This parallelism results in high power consumption by the UWB receiver. This will deter the UWB receiver from being employed in WBSNs.

Also, as regulation and standardisation of commercial UWB operation is fairly new, different researchers and industries are attempting to propose various methods of making UWB communication work. Majority of the proposed transceiver architectures use parallel architectures as they concentrate on performance and data rates leading to high power consumption. Limited research attempts on power consumption reduction methodologies leads to a potential gap and provides an opportunity of thorough investigation and proposal of a possible solution for power saving. The research conducted for this chapter is carried out in order to fill those gaps and explore this potential. It presents the thorough investigation and analysis of parallelism requirements for different channel conditions and provides a solution for power consumption reduction by incorporating real time reconfigurability of the parallel blocks in the UWB impulse radio receiver. The reconfiguration of the parallel blocks will result in effective utilisation of the hardware, reduction in average power consumption and at the same time maintenance of data error rate performance as a normal receiver.

#### 4. Digital UWB impulse radio

This section presents the design and functionality of the digital UWB impulse radio transceiver architecture. In the UWB impulse radio transceiver the transmitter uses short Gaussian derivative pulses spread over the 0-960MHz frequency band for communication. The receiver uses coherent detection to recover the data and performs three major operations viz. acquisition and synchronisation of transmitter/receiver, tracking and data detection (Chen, 2002), (O'Donnell & Brodersen, 2005).

##### 4.1 UWB transmitter

The UWB transmitter block diagram is presented in Fig. 3. The binary data to be transmitted is spread using a pseudo random noise (PN) sequence in order to provide system processing gain. The length (N) of the PN code depends on the required processing gain. Any PN code can be used for spreading, but barker code is used in this design due to good cross-correlation with the side-lobe values and uniform distribution. One raw data bit is represented as 'N' bits of PN code individually known as a 'chip'. The entire spread data bit is termed as a 'symbol'. Each chip in the symbol modulates the Gaussian derivative pulse using binary phase shift keying (BPSK) modulation. These modulated pulses are repeated at a certain pulse repetition period (PRP) (PRP=128ns for this design). The transmit packet

consists of a preamble for receiver acquisition and synchronisation operation and data bits which is then sent over the wireless channel (Chen, 2002), (O'Donnell & Brodersen, 2005) (O'Donnell, 2006).

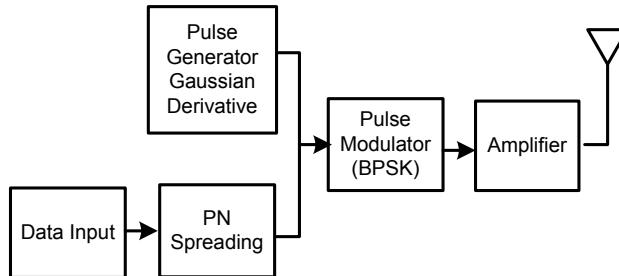


Fig. 3. UWB transmitter block diagram

#### 4.2 UWB Receiver

The analog frontend of the receiver consists of an antenna and amplifier to receive and amplify the signal as presented in Fig. 4. Filtering follows the amplifier, which suppresses interferers in the mobile phone band around 900MHz, frequency modulation (FM) radios and most Very High Frequency (VHF) television signals below 110MHz. A bank of parallel, time-interleaved ADCs, sample the received signal at an effective sampling rate of 2 GHz. The ADC is brought as close as possible to the receiver antenna in order to utilise digital domain processing potential (O'Donnell, 2006).

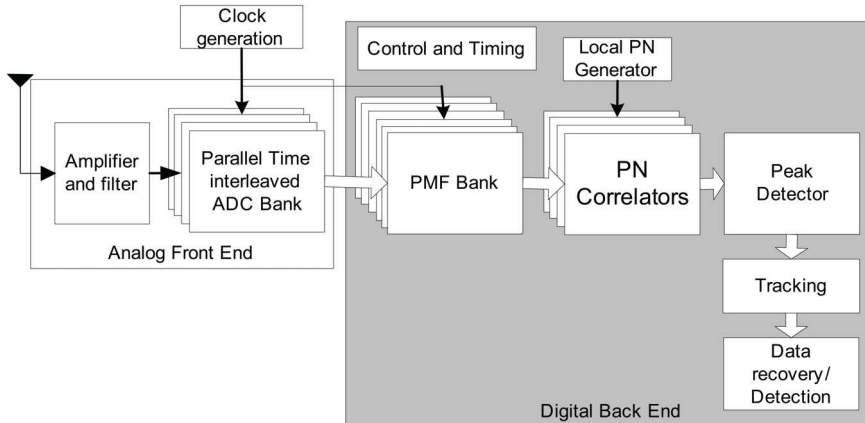


Fig. 4. UWB receiver block diagram

As the bandwidth of the UWB signal is 1GHz, minimum required ADC sampling frequency at the receiver is 2GHz. A single ADC working at 2GHz can be implemented to sample the entire PRP, but its power consumption will be very high. Therefore, a bank of parallel time interleaved 1-bit ADC's, each operating at a much lower frequency is used. This bank consists of 32 parallel ADCs, each sampling the received signal at 62.5MHz to provide an effective sampling rate of approximately 2GHz. As each of the ADC operates at low frequency, power consumption is low. The 1 bit sampling of a 128ns PRP signal at 2GHz

results in 256 bits of the received pulse which are parallel inputs to the digital backend (Chen, 2002), (O'Donnell & Brodersen, 2005) (O'Donnell, 2006).

Clock generation module, bank of parallel digital pulse matched filters (PMFs), bank of parallel pseudo noise correlators (PNCs), peak detector, local PN generator, data recovery and control block together constitute the digital-backend. The digital backend employs a bank of PMFs and PNC to perform acquisition and synchronisation operation followed by tracking and data detection.

Fig. 5 presents the block diagram of the digital backend (Chen, 2002), (O'Donnell & Brodersen, 2005). The banks of parallel PMF's and PNCs perform acquisition and synchronisation operation over the entire preamble. PMF's resolves the time delay in the received pulse to ensure maximum energy capture within the sampling window. Length of the PMF is 128ns corresponding to worst case delay spread of 64ns (O'Donnell & Brodersen, 2005). A single PMF for time delay resolution will need it to operate at sampling frequency of 2GHz which will consume significantly large amount of power and result in longer acquisition time. Therefore, 128 parallel PMF's process the 256 samples of the received pulse simultaneously. Each PMF now operates at pulse repetition frequency (1/PRP) instead of sampling frequency (1/Tsample) due to the parallel operation.

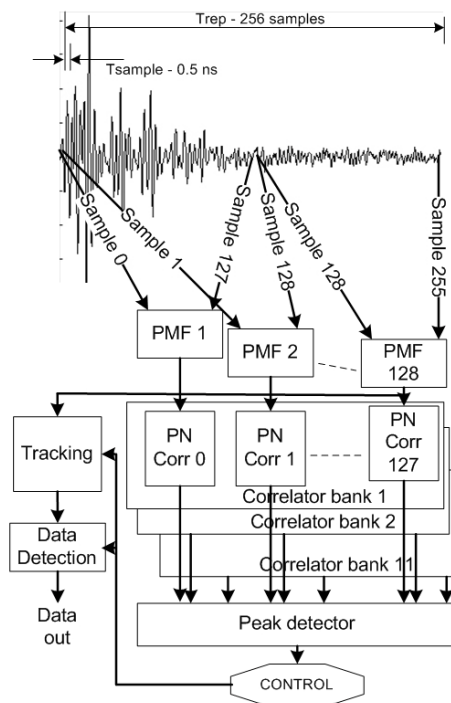


Fig. 5. UWB receiver digital backend (O'Donnell & Brodersen, 2005)

128 PNCs correlate 128 outputs of PMF's, to resolve the PN phase over symbol period. In order to further reduce the acquisition and synchronisation time, 11 such PNC banks operate simultaneously (Chen, 2002), (O'Donnell & Brodersen, 2005). Synchronization is declared once the PMF capturing maximum energy within the PRP and correct PN phase is

detected, by the peak detector. Data detection is then performed with a hard decision, depending on the sign of maximum correlation output.

In the acquisition and synchronisation mode all 128 PMF's and 128 x 11 PN correlators are in operation, where as in data detection, only the one capturing maximum energy is 'on'. Due to this the power consumption in the acquisition and synchronisation mode is high as compared to the data detection.

## 5. Real time reconfigurability algorithm

In order to meet the ultra low power requirement of WBSNs, it is required to reduce power consumption of the UWB receiver during the acquisition and synchronisation mode. In order to achieve this, the number of parallel PMF's and thus the successive PN correlators used in the acquisition mode needs to be reduced.

### 5.1 Parallelism requirement

The parallelism in the digital backend facilitates the receiver to cope with the worst case channel condition and different time delays in the received signal. However it is unlikely that always the channel condition will be worst and the receiver would not require all the parallel hardware for successful acquisition and synchronisation. In an indoor environment the received UWB signal is a collection of different paths reflected from different surfaces (walls, ceiling, floor, furniture etc) constituting multipaths and thus delay spread. The UWB indoor channel delay spread may vary from 20ns-60ns (O'Donnell & Brodersen, 2005) (Cassioli et al, 2002). Also in the non line of sight (NLOS) environment the direct path at the receiver may not be the strongest one. Due to the NLOS nature of the environment, different reflected multipaths and transmitter-receiver separation distance a time delay is observed in the received signal. This time delay is resolved by the PMF bank and is an important factor to be considered while collecting the energy from the received pulse.

According to the parallelism analysis in (Naik et al, 2007), time delay in the received signal controls where the maximum received energy lies within the PRP and therefore determines the number of parallel PMF's required for acquisition and synchronisation operation for a particular channel condition. The channel taps (amplitudes of individual reflected paths) also contribute in determining the energy captured by each PMF.

The analysis simulates the acquisition and synchronisation mode using all 128 parallel PMFs and successive PNCs in operation. Transmit signal is passed through 100 different channel impulses generated using IEEE 802.15.4a channel model (Siwiak, 2004). The time delay is varied from 0ns to 50ns for each channel condition and the PMF number capturing the maximum energy as reported by the peak detector for each condition is determined. This number represents the least number of PMF's required to be in operation for successful acquisition and synchronisation operation for the current operating channel impulse and time delay. The analysis results show that:

- Number of PMF's required for processing the received signal for different channel impulses are different;
- For same channel impulses if time delay increases, PMF reported by the peak detector increases significantly; and
- In very few channel impulse cases and higher time delay values all the 128 parallel PMF's are required for operation.

The real time reconfigurability of the parallel blocks according to the changing channel condition and time delay has the potential to reduce the power consumption during the

acquisition and synchronisation mode without affecting the bit error rate performance of the receiver (Naik et al, 2007).

## 5.2 Real time reconfigurability algorithm proposal and design requirements

The majority of the parallelism of the digital UWB receiver is in the digital backend. The banks of 128 PMFs and  $11 \times 128$  PNCs employed in the digital backend, constitute of more than 80% of its hardware (Chen, 2002). According to the receiver operation presented in section 4.2, the entire bank of 128 PMFs and 11 banks of 128 PNCs each, are in operation simultaneously during acquisition and synchronisation mode (during preamble). On the other hand, in tracking and data detection mode, only three adjacent PMFs and PNCs are in operation. This results in high power consumption in the acquisition and synchronisation mode as compared to the tracking and data detection.

From all the above considerations it can be concluded that, it will be most effective to use as many parallel PMFs and PNCs that are required for receiver operation for the current channel conditions and switch off the remaining ones, for the rest of the acquisition and synchronisation mode. In a very good channel condition only a few PMFs and PNCs would be required for correct receiver operation, therefore, the remaining ones can be switched off to save significant power consumption. This number will increase as the channel condition gets worse. As major percentage of the digital backend hardware will be reconfigured with this strategy, it has the potential to result in significant reduction in the average power consumption. Therefore, reconfiguration of the PMF and PNC banks according to the changing channel condition during majority of the acquisition and synchronisation mode is the most effective reconfiguration strategy.

Fig. 6 presents the block diagram for the proposed real time reconfigurability algorithm (RTRA) architecture. It consists of an estimation block which estimates significant energy received within the PRP and time delay in the received signal for current channel condition. The translation block translates this information into the number of PMF's required and the control block finally generates the enable/disable signals to turn on the required number of PMF's and successive PNCs in the bank and switch off the unwanted ones.

The primary aim of the RTRA is to facilitate average power saving in the acquisition and synchronisation mode of the receiver. The design constraints and important considerations for the RTRA are as follows:

- It should be simple and should introduce least hardware. Its power consumption should be low to justify the power saving;
- The algorithm should perform all the operations in the first few received pulses in order to save as much power as possible in the remaining preamble (acquisition and synchronisation mode); and
- The estimation and translation should be accurate in order to maintain the data detection error rate performance of the receiver.

## 6. RTRA design and implementation

### 6.1 Estimation algorithm

The transmitted signal in an indoor wireless channel undergoes reflections from various objects. Thus, the received signal is a collection of all reflected components at different times, called multipaths. Equation (1) represents the generalised channel response.



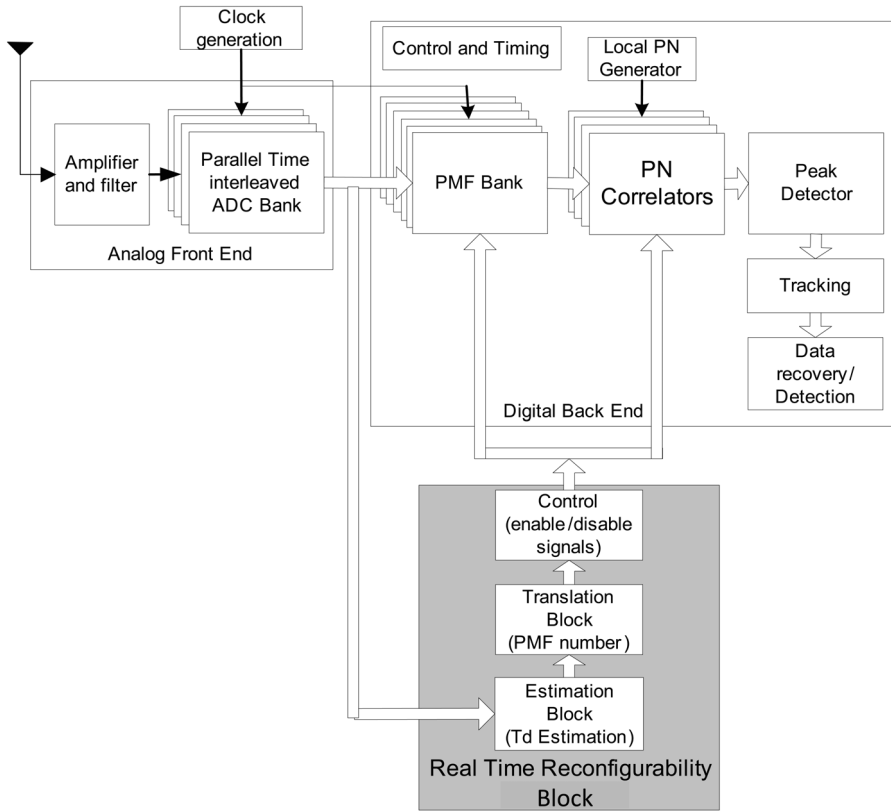


Fig. 6. Real time reconfigurability algorithm architecture

$$h(t) = \sum_{l=1}^L a_l \delta(t - t_l) \tag{1}$$

Where  $a_l$  is the attenuation,  $t_l$  is the time delay,  $L$  is the number of multipaths. In the channel response, values of attenuation and time delay change with respect to time and environment of operation Molisch, (2006). A pulse train of Gaussian 1st derivative pulses of width 3ns and PRP of about 128ns is used. Typical channel delay spread varies from 20-60ns (O'Donnell & Brodersen, 2005) (Cassioli et al, 2002), which means that the 3ns transmitted pulse has reflected components and the total energy received can be distributed over 20-60ns within the PRP. Also, due to time delay, the significant energy in the received signal can lie anywhere within the PRP.

For implementing the RTRA, some sort of channel and time delay estimation needs to be performed in order to obtain the information of significant energy received within the PRP. Traditional channel estimation methods are used for BER improvement. For estimation in this case, the aim is to extract sufficient information from the received signal in order to facilitate parallelism reduction. Implementing traditional, complex channel estimation algorithms would not server the purpose in this case as they require very high sampling

rates, additional pilot symbols and perform channel estimation over the entire preamble. Also, majority of them are implemented for offline processing where signal quantisation is not an issue. However, in our case the received signal is quantized for 1-bit resolution. This factor is one of the big challenges for RTRA implementation.

In the estimation block we propose to estimate the location of the last significant energy sample number within the PRP of the received pulse. This last significant sample information can be used to estimate the PMF capturing the maximum energy. This information can be obtained from the first few received pulses and used for translation.

As the received signal is sampled by 1-bit ADCs, the input data for the digital backend is a 256-bit long vector with each bit representing one sample in the received pulse. The last significant sample number estimation becomes as simple as determining the last sample which is '1' within the 256-bit long pulse sample vector and its sample number. For this we propose to use a priority encoder algorithm, which will take the 256-bit vector as input and output 8-bit last significant sample number.

In order to validate this estimation method, received signal pulses for 100 different channel impulses are obtained and last significant sample number is obtained for each case without any quantisation. Later, these received signals are quantized by 1-bit ADC and last significant sample number is estimated for each case using the 256-bit priority encoder algorithm. Fig. 7 presents the last significant sample number determined for no quantisation case and that determined by the priority algorithm after quantisation.

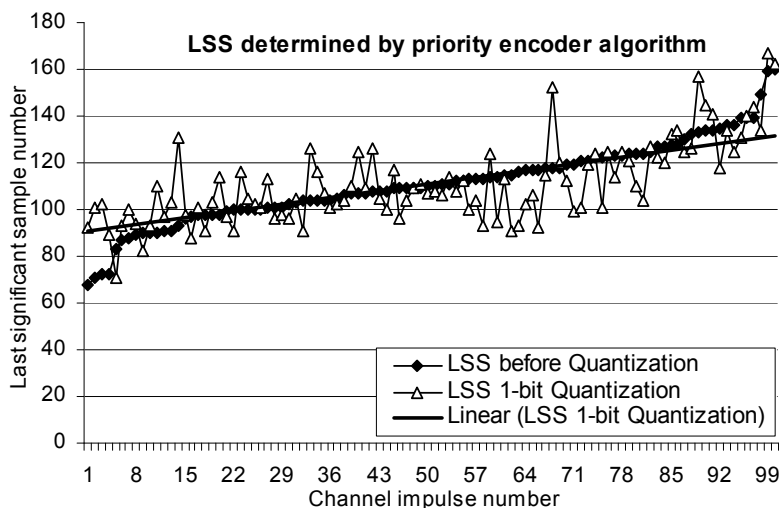


Fig. 7. Last significant sample results for priority encoder algorithm for 1 bit input

It can be seen in Fig. 7 that the last significant sample estimation for 1-bit quantisation by priority encoder algorithm resembles very closely to that with the one without quantisation for majority of the cases. The difference between the last significant sample number values is mainly due to quantisation. The priority encoder can be very easily implemented with less hardware and its processing is fast and simple. The small error between actual and estimated last significant sample numbers can be easily compensated in the translation block.

## 6.2 Translation and control algorithms

Translation is the process in which the last significant sample information obtained from the estimation block is translated to number of parallel PMFs required for the acquisition and synchronisation operation. For an effective translation, number of PMFs estimated by RTRA ( $T_{pmf}$ ) should be equal to or more than the PMF reported to capture the maximum energy in a normal receiver ( $pmf_{ref}$ ), for the same channel condition. If  $T_{pmf} < pmf_{ref}$ , then the translation method is said to fail and can cause an error in data detection. However, the probability of data detection error depends on the closeness of  $T_{pmf}$  to  $pmf_{ref}$ , due to the energy capture principle.

In translation of the last significant sample information to number of PMFs required for acquisition and synchronisation operation, we assume that the last significant sample lies in the centre of the PMF capturing the maximum energy. This ensures that the translated number of PMFs actually cover the part of the PRP where significant energy is received. Translation method 1 (TM1) is defined by Equation (2) where LSS is the last significant sample.

$$\begin{aligned} &\text{if } LSS \leq 64 \text{ then, } T_{pmf} = \frac{LSS}{2}; \\ &\text{if } LSS \leq 191 \text{ then } T_{pmf} = LSS - 64; \\ &\text{else } T_{pmf} = 128 \end{aligned} \quad (2)$$

In order to validate the translation method, the transceiver is modeled in simulation environment. PMF numbers reported by the peak detector after acquisition and synchronisation operation for a normal receiver are determined for 100 different channel impulses and time delay varying from 0-50ns. Later, for each of these channel impulses and time delays, estimation is performed using priority encoder and translation is performed using the translation methods. Percentage of failure cases, the figure of merit used to validate the translation methods is the percentage of channel impulses in which  $T_{pmf} < pmf_{ref}$ . Fig. 8 presents the percentage failures cases for the translation methods.

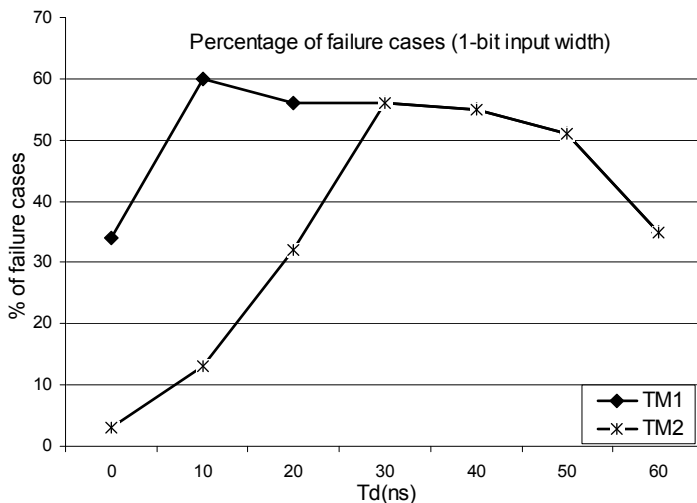


Fig. 8. Percentage failure cases for translation methods (TMs)

It can be seen from Fig. 8 that translation method 1 results in approximately 50% failure cases for most time delay values. However, individual simulations show that  $T_{pmf}$  values are very close to  $pmf_{ref}$ , which reduces probability of data detection error. Nevertheless, such a high percentage of failure cases for lower time delay values from 0-30ns, may lead to high data detection errors, as significant energy within the PRP may not be captured due to low value of  $T_{pmf}$ . However, for higher time delay values, this does not have such an effect as the chances of losing significant energy is reduced due to higher values for  $T_{pmf}$ . Average relative power saving percentage after reconfiguration is estimated assuming that 100% power is consumed when all 128 PMFs are 'on' and is presented in Fig. 9. It shows that the average relative power saving percentage varies from 90% to less than 10% with increasing time delay.

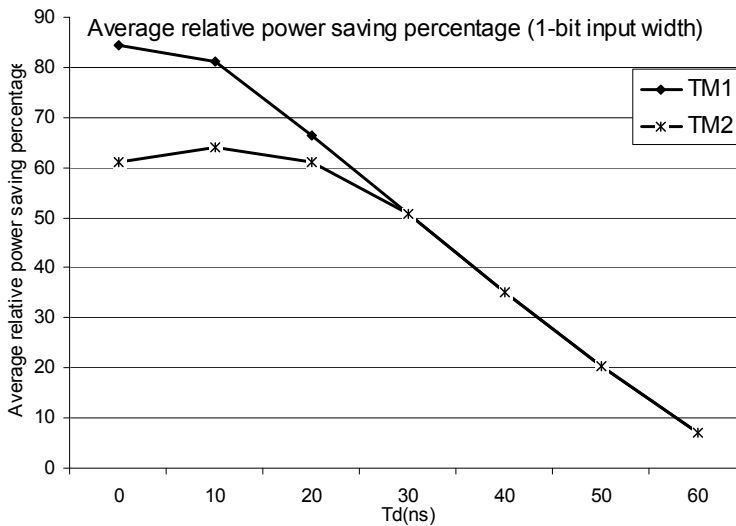


Fig. 9. Average relative power saving percentage

In order to reduce the percentage of failure cases for lower time delay values in translation method 1, translation method 2 uses a guard band of 32 PMFs and is defined by Equation (3)

$$\begin{aligned} &\text{if } T_{pmf_1} \leq 32; \text{ then } T_{pmf_2} = T_{pmf_1} + 32; \\ &\text{else } T_{pmf_2} = T_{pmf_1} \end{aligned} \quad (3)$$

With the guard band, the percentage failure cases are reduced for lower values of time delays, as seen in Fig. 8. However, this improvement comes at a cost of reduced average power saving, as seen in Fig. 9. Also, probability of data detection error is considerably reduced for lower time delay values.

In order to validate the maintenance data detection error, 5000 sample data bits are used. The data detection error before reconfiguration and after reconfiguration is estimated. Fig. 10 presents the percentage data detection error comparison. The results of this analysis show that the proposed RTRA performs better than normal receiver with 0.5% reduction in the detection error for time delay values of 0-20ns, a marginal increase of 0.6% in detection

errors for time delays of 30-40ns and same detection error for remaining time delays. Therefore, translation method 2 maintains the data detection error. The small increase in data detection error for certain cases can be easily compensated in the error detection and correction block of the receiver.

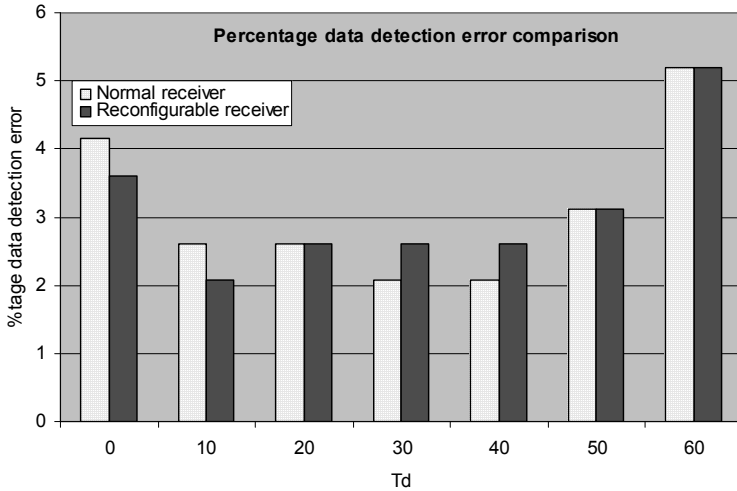


Fig. 10. Percentage data detection error comparison

The percentage data detection error comparison provides enough evidence that the proposed estimation and translation methods can efficiently reconfigure the UWB receiver digital backend and maintain the data detection error rate of the normal receiver. Once translation is done the control block generates enable/disable signals to switch off the unwanted PMFs and PNCs.

### 6.3 RTRA hardware design

The acquisition and synchronisation mode hardware, which include the PMF and PNC banks, constitutes of 80% of hardware of the receiver digital backend (Chen, 2002). The major percentage of this hardware is the PMF bank. Power efficient hardware design for a single PMF is presented in (Naik & Singh, 2007) is designed to suit the stringent low power design requirements.

In order to simulate the acquisition and synchronisation mode operation of a normal receiver and that with RTRA, a bank of 128 PMFs is implemented with each PMF having an enable signal. A 256-bit input buffer stores the received input samples from the ADC bank. Each PMF in the bank processes consecutive windows of 128 samples each, which are one sample apart. When all the 128 PMFs are enabled, this PMF bank implementation represents normal receiver operation. Fig. 11 presents the block diagram of the PMF bank implementation for the normal receiver. It also presents the RTRA blocks that are added to the normal receiver in order to reconfigure the PMF bank.

For the RTRA, a 256:8 bit priority encoder is implemented as the estimation block, which results in 8-bit last significant sample number. The translation methods presented in equations (2) and (3) are implemented using digital combinational and sequential logic. The translation block results in a 7-bit  $T_{pmf}$  value.

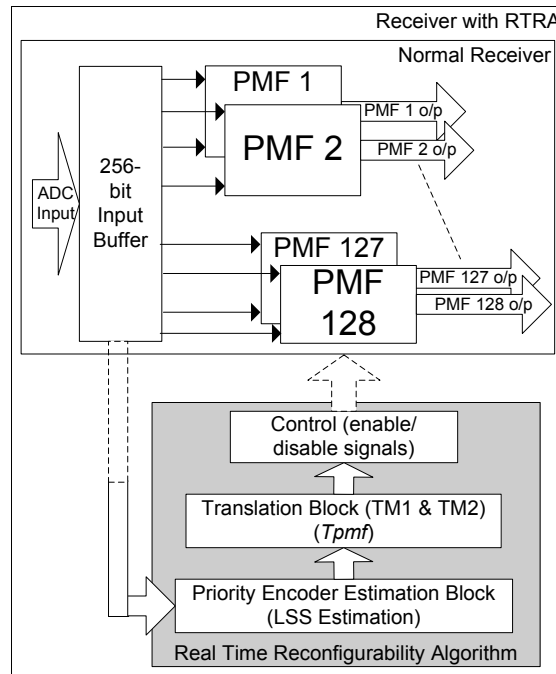


Fig. 11. PMF implementation bank for normal receiver and that with RTRA

Finally the control block is a decoder which decodes the 7-bit  $T_{pmf}$  value and generates 128 enable/disable signals which then enable/disable the PMFs according to the changing channel condition.

The PMF bank for acquisition and synchronisation operation for a normal receiver and that with RTRA, as presented in Fig. 11, is implemented using the semi-custom design flow using ST-Microelectronics 90nm technology. Both the designs process received data samples at the same pulse repetition frequency. Fig. 12 presents the post place and route view of the reconfigurable PMF bank for the UWB receiver with RTRA. Table 1 presents the hardware implementation results and the comparison of normal receiver to that with RTRA. The power consumption results are obtained by performing a simulation based power analysis with the input signal for different channel conditions and time delays.

It can be observed in Table 1, that the number of instances, nets, wire length and core area for PMF bank with RTRA implementation for reconfigurable receiver increases as compared to the normal receiver PMF bank due to additional hardware for the RTRA implementation. Due to the simplicity of the estimation, translation and control algorithms of this additional hardware results in a 3.75% increase in area.

The power consumption results show a 25.16% reduction in the core power consumption and 23.76% reduction in the average power for receiver with RTRA over the normal receiver for the test input data. As 90nm process technology is used, leakage power is high and dominates total average power consumption.

These two designs were also implemented on an Altera Stratix II Field Programmable Gate Array (FPGA) device to verify the power saving. A significant 28.57% reduction in the

average current consumption was observed by the PMF bank with RTRA for reconfigurable receiver as compared to that for the normal receiver. The FPGA implementation results correspond with those of the ASIC implementation.

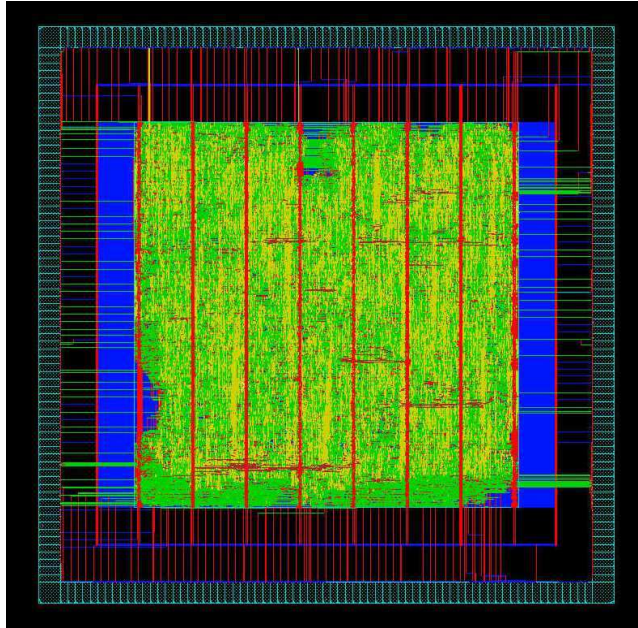


Fig. 12. PMF bank and RTRA post place and route view

Parameter	Normal Receiver	Receiver with RTRA	Relative Comparison
Number of Instances	1202852	1234395	2.55% ↑
Number of Nets	855647	872565	1.93% ↑
Total wire length (μm)	9792686	10495531	6.69% ↑
Area (μm <sup>2</sup> )	2517148	2611764	3.75% ↑
Core Power (mW)	181.72	135.99	25.16% ↓
IO power (mW)	10.67	10.67	↔
Avg power (mW)	192.38	146.67	23.76% ↓

Table 1. Hardware implementation results and comparison

## 7. Conclusion

This chapter presented a new paradigm of biosensors which have processing capability with an intelligent and adaptive wireless communication module. The adaptive communication module efficiently reconfigures its hardware components according to the changes in operating environment in order to reduce system power consumption and optimally utilise resources. The chapter presented several significant applications of wireless biosensor networks which hold enormous potential to benefit the community. It also identified that

low power consumption is one of the critical design parameters for biosensor node design due to battery operation and UWB communication is one of the most suitable technologies to be used for communication.

Further the chapter presented the potential challenges of parallel hardware and high power consumption in the UWB receiver architecture and proposed a real time reconfigurability algorithm to address that. The real time reconfigurability algorithm senses the current operating condition and intelligently reconfigures the receiver hardware to optimal size in order to reduce the average power consumption. The results show approximately 25% power saving in the receiver's digital backend with the implementation of the real time reconfigurability algorithm for ASIC as well as FPGA implementations. At the same time the reconfigurability maintains the data detection error rate as the normal receiver. This significantly contributes in reducing the overall system power consumption and makes UWB transceiver a better candidate to be used in the biosensor unit for WBSN applications. Thus the proposed novel intelligence in the communication module of the biosensor unit is one of the important steps in the development of a sophisticated and smart biosensors and WBSN.

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A biosensor is defined as a detecting device that combines a transducer with a biologically sensitive and selective component. When a specific target molecule interacts with the biological component, a signal is produced, at transducer level, proportional to the concentration of the substance. Therefore biosensors can measure compounds present in the environment, chemical processes, food and human body at low cost if compared with traditional analytical techniques. Bringing together researchers from 11 different countries, this book covers a wide range of aspects and issues related to biosensor technology, such as biosensor applications in the fields of drug discovery, diagnostics and bacteria detection, optical biosensors, biotelemetry and algorithms applied to biosensing.

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