All-Optical Quaternary Logic Based Information Processing: Challenges and Opportunities

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Additional information is available at the end of the chapter

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1. Introduction:

Science and Technology is providing people all over the world with much better ways of communicating than ever before, and the winds of change have whipped up the desire to exchange more of everything from messages to movies. The field of computation and signal processing is growing day by day [1-7]. In last three to four decades, the philosophy, science and technical prospects enriched the scientific communities a lot. Massive parallelism, speed of operation, increased spatial density attracts in many ways the scientists, researchers and technologists. Very Large Scale Integration (VLSI) technology has revolutionized the electronics industry and established the 20th century as the computer age. But, VLSI technology is approaching its fundamental limits in the sub-micron miniaturization process. Therefore an alternative technological solution to the problem of high speed information processing is needed, and unless we gear our thoughts toward a totally different pathway, we will not be able to further improve our information processing performance for the future. Conservative and reversible logic gates are widely known to be compatible with revolutionary computing paradigms. At the same time the Multi-valued logic (MVL) is also positioned as a coming generation technology that can execute arithmetic functions faster and with less interconnect than binary logic [8-48].

In order to overcome the electronic bottlenecks and fully exploit the advantages of optics, it is necessary to move towards networks, where the transmitted data will remain exclusively in all optical domains without optical electrical optical (OEO) conversions. Ultra high-speed optical network is developing rapidly as growing capacity demand in telecommunication system is increasing. In these networks, it is desired to carry out switching, routing and processing in optical domain to avoid bottlenecks of optoelectronic conversions. The dream of photonics is to have a completely all-optical technology. All-optical

switching is an essential technology for transparent fiber optic networks and for all forms of optical signal processing as the optical interconnections and optical integrated circuits is immune to electromagnetic interference, and free from electrical short circuits. In a pursuit to probe into cutting-edge research areas, the development of different ultra-fast all-optical switches has received considerable interest in recent years all over the world for future optical information processing [49-59]. As photon is the ultimate unit of information with unmatched speed and with data package in a signal of zero mass, the techniques of computing with light may provide a way out of the limitations of computational speed and complexity inherent in electronics computing.

The fundamentals of digital signal processing are straightforward. To send something as simple as a phone message or as complicated as a picture, we digitize it by breaking it up into a series of binary bits, transmit the bits, and decode them at the other end to re-create the message or picture. The ones or zeroes in the bits are encoded by turning some signal on or off. In the past, the signal has been electrical, but increasingly it is composed of light pulses. We use a laser to produce the light, and then add information to it with a modulator, transmit it through optical fibers, amplify it if needed, receive it with a photo detector and re-create the message with a demodulator. An optical signal is better than an electrical one, with less attenuation, faster switching, and more signals traveling together. In everyday we have to handle enormous and ever increasing, amounts of information. Binary number (0 and 1) is insufficient in respect to the demand of the coming generation. The application of multi-valued (non-binary) signals can provide a considerable relief in transmission, storage and processing of large amount of information in digital signal processing. Quaternary logic (4-valued) is one type of MVL [60-82].

In this chapter, all-optical scheme for designing some polarization encoded quaternary logic gates (quaternary min and quaternary delta literal) with the help of nonlinear material based interferometric switches have been discussed. Design of all-optical quaternary multi-valued multiplexer and demultiplexer circuits have also been described with the help of these basic gates. For the quaternary data processing in optics, the quaternary number (0, 1, 2, 3) have been represented by four discrete polarized state of light. In optical implementation we can consider the set of Quaternary logic states {0, 1, 2, 3} as : 0= No light, 1 = vertically polarized light ($\updownarrow$), 2 = horizontally polarized light (•), 3 = partially polarized light ($\leftrightarrow$).This chapter is organized as follows. Section-1.1 to 1.3 gives a brief overview of multi-valued logic (MVL) i.e. What is MVL? Why do we need it? How it can be implemented and where MVL can be applied? Section-2.1 describes the basic principle of all-optical interferometric switches which is the cornerstone of all logic based signal processing. Section-2.2 and section 2.3 describes the design and operational principle of some basic all-optical quaternary logic circuits (QMIN, Delta Literal). All-optical circuit for quaternary multiplexer and demultiplexer are described in section-2.4 and section 2.5. Also quaternary T-gate is discussed in section 3. Challenges in design issues that is to be considered for experimentally achieve result from the proposed scheme is mentioned in section section-4. Chapter ends with Conclusions and Future Scopes given in section-5.
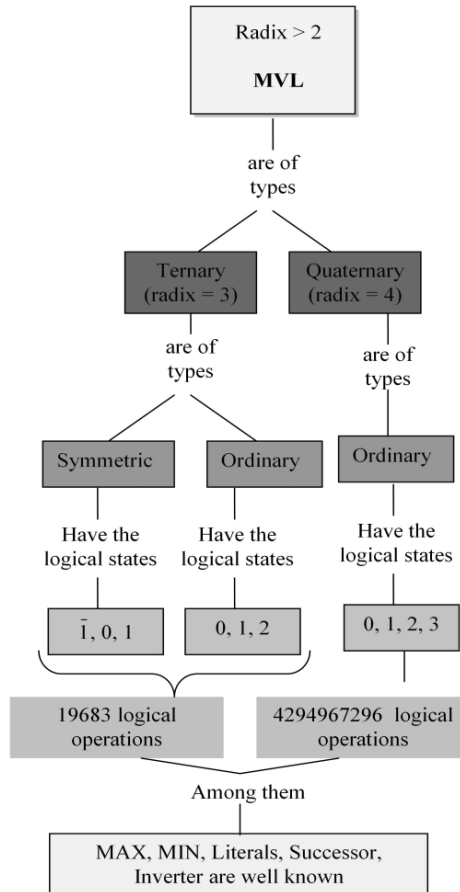
Figure 1. Different field in multi-valued logic.

1.1. What is Quaternary Logic?

Multi-valued logic (MVL) is a non binary logic with radix >2. Binary logic is limited to only two states 'True' (1) and 'False' (0), MVL replaces these with finite and infinite number of values. MVL system is defined as system operating on higher radix than two. In the base-R number system, a numerical value of N-bit data$(a_{N-1}a_{N-2}\cdots a_2 a_1 a_0)_R$; [where $0 \leq a \leq (R-1)$] can be written as [56] :

$$(a_{N-1}.R^{N-1} + a_{N-2}.R^{N-2} + \cdots + a_1.R^1 + a_0.R^0) = \sum_{i=0}^{N-1} a_i.R^i \tag{1}$$

For example Ternary logic (R=3) has three logical states {0, 1, 2} or {$\bar{1}$, 0, 1} [18]. These are known as ordinary ternary and symmetric ternary logic respectively. Quaternary logic (R = 4) has four logical states {0, 1, 2, 3}. Like binary world there are also numbers of basic gates in multi-valued logic world. Depending on the radix and number of variables used, different logic functions can be generated. The numbers of possible functions are [37].

$$f(R,n) = R^{(R^n)} \tag{2}$$

Where R = radix, n = number of variables. In ternary logic of two variable (R = 3, n =2) there are $f(3, 2) = 3^{3^2} = 19683$ possible functions. For quaternary (R = 4, n = 2) there are $f(4, 2) = 4^{4^2} = 4294967296$ logical operations. Hence, huge numbers of logical operation can be possible for higher radix (Fig. 1). Among them, some basic gates are the MAX, MIN, Complement, Cycle or successor, Literals etc [6, 7, 38-41], which is indicated in Fig. 2.

1.2. Why do we need All-optical Quaternary Logic based signal processing?

The most pressing problems in present-day binary systems are interconnection problems, both on-chip and between chip. On chip the difficulties of placement and routing of the digital logic elements which go to make up the complete chip are escalating with increase in capability per chip, and the silicon area used for interconnections may be greater than that used for the active logic elements. Similarly, the difficulties of bringing an increasing number of connections off-chip is promoting -a new consideration of packaging concepts in an attempt to overcome problems which are becoming mechanically, thermally, and electrically extreme. All these factors point to the attraction of raising the information content per interconnection from the present lowest-possible (binary) level. Multiple-valued logic, in which the number of discreet logic levels is not confined to two, has been the subject of much research over many years. The practical objective of this work is to increase the information content of the digital signals in a system to a higher value than that provided by binary operation. To increase the transmission capacity of future communication the present binary system is becoming very critical. A more formal approach would be an n-valued logic which has n different states, each state having a unique identifier. Multi-valued logic (MVL) is defined as a non-binary logic and involves the switching between more than two states. Multi-valued logic can be viewed as an alternative approach to solve many problems in transmission, storage and processing of large amount of information in digital signal processing [22]. The main advantages of multi-valued logic systems and circuits are greater speed of arithmetic operations realization, greater density of memorized information, better usage of transmission paths, decreasing of interconnections complexity and interconnections area, decreasing of pin number of integrated circuits and printed boards, possibilities for easier testing.

In the field of data communication, the quaternary codes are preferred because four-valued (i.e. quaternary) logic signals easily interface with the binary world. They may be decoded directly into their two binary-digit equivalent. Quaternary logic world can easily be interfaced with binary logic in all-optical domain with the help of our suggested DEC and ENC

schemes [57, 59]. The block diagram of this interfacing circuit is shown in the Fig. 3. Here input & outputs are 4-valued and the internal circuitry is binary (radix=2). Decoder circuit converts quaternary input into its binary equivalent. After performing the logical operation in binary system, it is then encoded to its quaternary equivalent by encoder circuit. Hence, it can be said that this scheme requires no major modifications of the existing transmitter, receiver, or transmission link. Quaternary digits are two major types: ordinary quaternary digit (OQD) and quaternary signed digit (QSD) [75-76]. QSD is useful for carry free arithmetic operations [19, 31-35]. Fig. 4 indicates how quaternary and binary are interfaced.
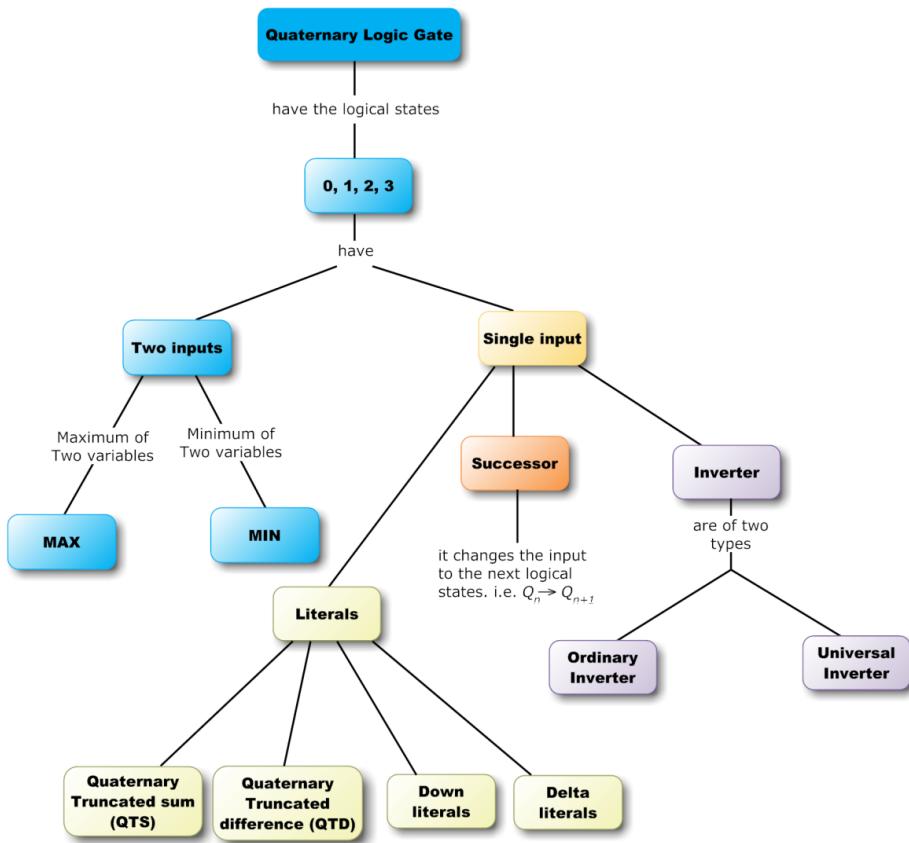

Figure 2. Different field in quaternary logic.

1.3. How All-optical Quaternary Logic can be implemented?

Consideration of different logical states is a challenge. It can be done in different ways and given in Fig. 5. In electronics, efforts have already been made to design four-valued logic

[37-48] with charge couple device (CCD). In I²L circuits 0mA, 10mA, 20mA and 30mAg are four different logical states, in νMOS (neuron-MOS) have the logic levels 0.0V, 1.1V, 2.2V and 3.3V [39], also in CMOS MVL have the logic levels 0 V, 1V, 2V, 3V respectively [37]. Quantum computation and information is the study of the information processing tasks that can be accomplished using quantum mechanical systems. Just as the classical computation is built upon bits, quantum computation also has an analogous concept called qubits. Analogous to classical computation, the operations on qubits are carried out using quantum logic gates. Of late, renewed interest in optical computing has been witnessed due to the emergence of novel photonics structures that includes nano-photonics, silicon photonics, bio-photonics and plasmonics etc. Optical quaternary logical operation is an interesting and challenging field of research for future optical signal processing where we can expect much innovation [58-82]. Polarization properties of light can play significant role here.
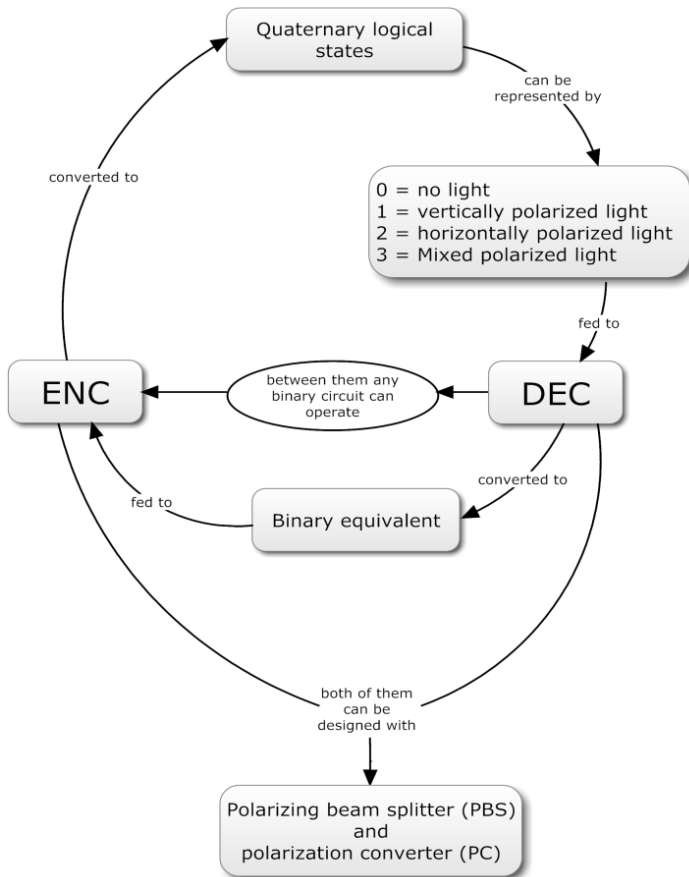

Figure 3. Binary-to-quaternary Encoder and Quaternary-to-binary decoder.

Polarization may be a good choice for representing different logical states in all-optical quaternary (4-valued) logic operations because [7, 15],

- Nature of polarization does not change due to absorption of light like intensity. Therefore the strength or weakness of the beam plays no role in the operation of the devices.

- The sate of polarization can be changed easily by Polarization converter.
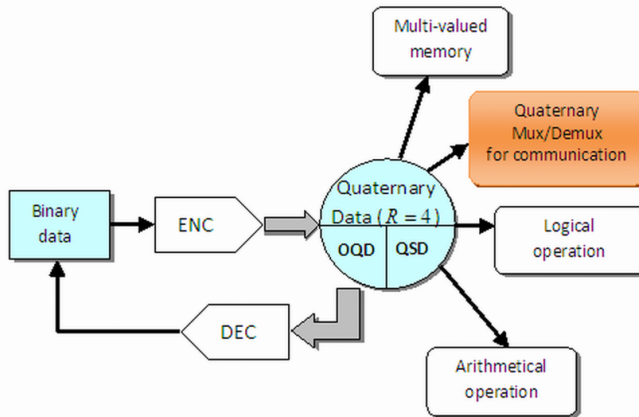
- No photon energy is wasted.

Figure 4. Interfacing Binary and Quaternary world by the help of ENC and DEC.
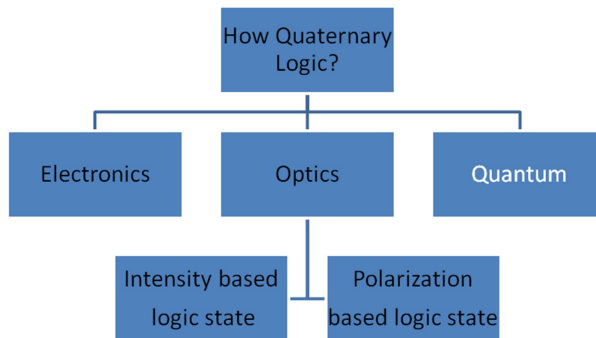

Figure 5. Quaternary (4-valued) logic implementation.

For the quaternary data processing in optics, the quaternary logic states {0, 1, 2, 3} can be represented by four discrete polarized state of light as mentioned below:

0 = No light.

1 = vertically polarized light ($\updownarrow$)

2 = horizontally polarized light ($\bullet$)

3 = mixed polarized light or un-polarized light ($\leftrightarrow$).

2. Designing of Polarization encoded all-optical Quaternary multiplexer / De-multiplexer

Multiplexing and de-multiplexing are two essential features in almost all the signal communication systems, where a lot of information is being handled without any mutual disturbances. The principles and possibilities of designing of all-optical quaternary multi-valued multiplexer and de-multiplexer circuits are described with the help of quaternary MIN and quaternary delta literal gates (Fig. 6). Nonlinear material based interferometric switches can take an important role here. Working principle of Terahertz Optical Asymmetric Demultiplexer (TOAD) based all-optical switch is discussed in Section-2.1. Section-2.2 and Sec-2.3 describes the design and operational principle of some basic all-optical quaternary logic circuits (QMIN, Delta Literal). All-optical circuit for quaternary multiplexer and demultiplexer are proposed and described in Sec-2.4 and sec-2.5 respectively.
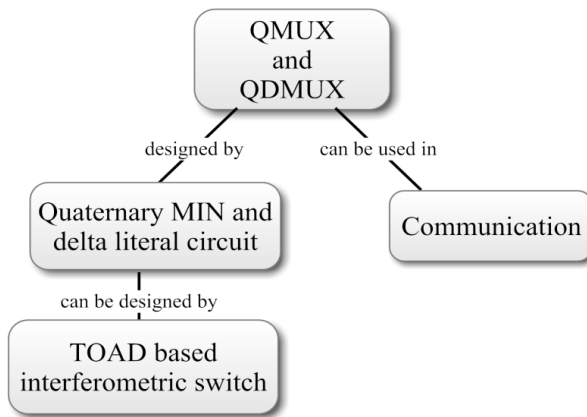
Figure 6. Overview of Quaternary Mux/Demux.

2.1. Interferometer based optical switch:

Interferometric devices for optical processing have been of great interest in the recent years [50-55]. Optical switch using a nonlinear interferometer makes it possible for one optical signal to control and switch another optical signal through the nonlinear interaction in a material. The incoming signal to be switched is split between the arms of the interferometer. The

interferometer is balanced so that, in the absence of a control signal, the incoming signal emerges from one output port. The presence of a strong control pulse changes the refractive index of the medium given by

$$\Delta n \;=\; n_2 I \tag{3}$$

Where Δn is the change in the refractive index of the medium, n_2 is the nonlinear refractive coefficient and I is the intensity of the light incident on the medium. A change in the index adds a phase shift between the two arms of the interferometer, so that the incoming signal is switched over to another output port. This method of switching is based on cross phase modulation (XPM). In much resent years, Semiconductor optical amplifier (SOA) makes a revolution in designing high speed (>100 Gb/s) interferometric switches in all-optical infor-mation processing system. The technology of SOA has been evolving rapidly during the re-sent years and has become mature enough so that it is now key factor in implementation of modern optical communication networks. SOA are commercially available device and have different important properties. Such as, fast and strong nonlinearities, short latency, thermal stability, low power consumption, large dynamic range, short response time, broadband and versatile operation and capability of large scale integration with chip level design.
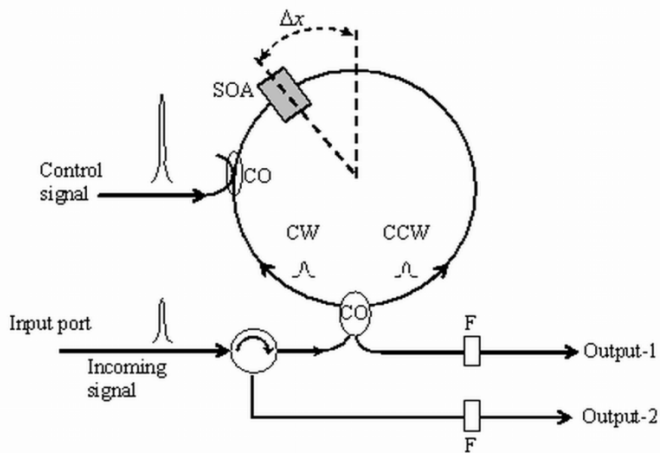
Figure 7. A TOAD based optical switch, where SOA: Semiconductor optical amplifier, CW: Clockwise pulse, CCW: Counter clockwise pulse, CO: coupler, F: Filter which blocks control pulse.

The Fig. 7 is a Sagnac interferometer that uses an SOA offset from the midpoint of the loop and is known as a terahertz optical asymmetric demultiplexer (TOAD). It can operate at frequen-cies in terahertz range [50-51]. There are two couplers; 1) the control coupler provides an input path for the control pulses to enter the fiber loop in order to saturate the SOA, and 2) the input coupler (50:50) where the incoming pulse signal train entering the loop splits equally into

clockwise (CW) and counter clockwise (CCW) pulses. CW and CCW pulses arrive at the SOA at slightly different times as determined by the offset Δx of the SOA from the midpoint of the loop. Another strong light pulse is also injected to the loop. It is called control signal (CS). When $CS=ON$, then SOA changes its index of refraction. As a result, the two counter-propagation data signal will experience a differential gain saturation profiles. Therefore cross phase modulation (XPM) take place when they recombine at the input coupler. Then relative phase difference between CW and CCW pulse become $\sim \pi$ and the data will exit from the transmitted port / T-port (output-1 according to the Fig. 7). In the absence of a control signal ($CS=OFF$), the incoming signal enters the fiber loop, pass through the SOA at different times as they counter-propagate around the loop, and experience the nearly same unsaturated amplifier gain of SOA, recombine at the input coupler. Then, relative phase difference between CW and CCW is zero (0). Then no data is found at the T-port. Then data is reflected back toward the source and isolated by optical circulator (CR). The port through which it comes is called reflected port /R-port (output-2 according to the Fig. 7). A filter (F) may be used at the output to reject the control and pass the incoming pulse. 'F' can be polarization filter of band pass filter.

The output power of transmitted port (T-port) and reflected port (R-port) of a TOAD based switch can be expressed as [52-53],

$$P_T(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) - 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \qquad (4)$$

$$P_R(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) + 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \qquad (5)$$

where, $G_{cw}(t)$, $G_{ccw}(t)$ are the power gain of CW and CCW pulse, $\Delta\varphi = (\varphi_{cw} - \varphi_{ccw})$ is the phase difference between CW and CCW pulse, can be expressed as $\Delta\varphi = -\alpha/2 \cdot \ln(G_{cw}/G_{ccw})$. The temporal duration of the switching window (τ_{win}) that depends on the offset position of the SOA in the loop (Δx) is given by $T_{off} = 2\Delta x/c_{fiber}$, where c_{fiber} is the velocity of light inside the optical fiber. More specifically eccentricity of the loop must be less than half the bit period, otherwise the two counter-propagating halves of incoming signal (IS) being processed will not experience the gain dynamics caused by their synchronized control pulses but instead by others resulting in incomplete switching. T_{FWHM} of the control pulse must be as short as possible and ideally less than the switching window so that when CCW pulse is inserted in the SOA the CW pulse already passed through and the SOA gain has started to recover after saturation by the control pulse or else the two components of IS will overlap inside the SOA perceiving its nonlinear properties only partially altered, thus obstructing the creation of the required differential phase shift [52-53].

$$\sigma < T < 0.5\xi < \tau_e < 1.5\xi \qquad (6)$$

$\xi$is bit period. For low switching window eccentricity of the loop (T) should be small. One data when transmit through the switching window, next data cannot pass until the gain recovery of the SOA takes place.

In summary we can say, in the absence of control signal, the incoming signal exits through input port of TOAD and reaches to the output port-2 as shown in Fig. 8(a).In this case no light is present in the output port-1. But in the presence of control signal, the incoming signal exits through output port of TOAD and reaches to the output port-1 as shown in Fig. 8(a).In this case no light is present in the output port-2. In the absence of incoming signal, port-1 and port-2 receives no light as the filter blocks the control signal. Only incoming signal is passed through filter. Truth table is given in Fig. 8(b).The above principle of the switch is used to design basic quaternary logic circuits.
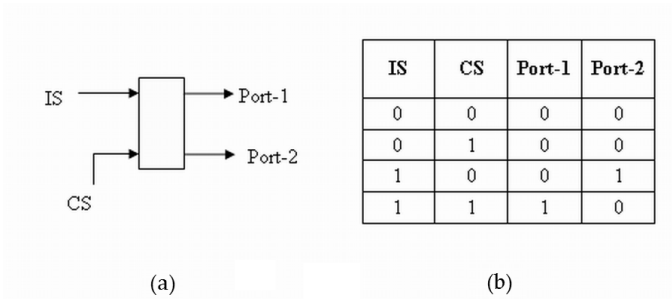
IS	CS	Port-1	Port-2
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0

(a)   (b)

Figure 8. (a) Schematic block diagram TOAD based switch (b) the corresponding truth table.

2.2. All-optical two input Quaternary MIN Gate

Quaternary MIN gate is equivalent AND gate in binary world [6,39]. It is an important multi-valued logic function. The QMIN operation is shown in the equation no (7), the operator $\wedge$ is QMIN operation. Truth table is shown in Table 1.

$$x_1 \wedge x_2 \wedge \cdots \wedge x_n = QMIN\left(x_1, x_2, \cdots, x_n\right) \tag{7}$$

		Y		
X	**0**	**1**	**2**	**3**
0	0	0	0	0
1	0	1	1	1
2	0	1	2	2
3	0	1	2	3

Table 1. Truth Table of Quaternary MIN(x,y).

Polarization encoded all- optical QMIN Gate is shown in the Fig. 9. Here light from inputs X and Y fall into two PBS (PBS$_1$ & PBS$_2$), where it split into two polarized light, one is vertically polarized ($\updownarrow$) and other is horizontally polarized ($\bullet$).Hence, X$_1$ & Y$_1$ are vertically polarized ($\updownarrow$) and X$_2$ & Y$_2$ are horizontally polarized ($\bullet$). Light from X$_2$ and Y$_2$ are fed to two Interferometric switches (here TOAD) S$_1$ and S$_2$ as incoming signal and also their control signals are taken from Y$_2$ and X$_2$ respectively. The lower outputs of S$_1$ and S$_2$ are passed through a PC (polarization converter, which is preferably half wave plate; converts vertically polarized light to horizontal one and vice versa). It is indicated as S$_{1L}$ and S$_{2L}$ respectively in the Fig. 9. X$_1$ and S$_{1L}$ is combined by a BC-1, the combined ray (C$_1$) is connected to another switch S$_3$ as incoming signal. Also Y$_1$ and S$_{2L}$ are combined by BC-2 and the combined ray (C$_2$) is connected to S$_3$ as control signal. The upper output channel of S$_3$ (S$_{3U}$) is feed to BC-3. Again X$_2$ and Y$_2$ are feed to another switch S$_4$ as incoming and the control signal respectively. All the control signals are amplified by EDFA (Erbium Doped Fiber Amplifier). When incoming light signal is incident on wavelength converter (WC) then the wavelength converter (WC) converts the wavelength of incoming signal to wavelength of control signal. The upper output channel of this switch S$_4$ (S$_{4U}$) is connected to BC-3. The combined ray is the final output. Let us describe the operational principles in detail [66].

1. When X=0, X$_1$=X$_2$=0. X$_2$ which act as a incoming signal of S$_1$ and S$_4$ is zero. So S$_{1L}$ and S$_{4U}$ receive no light. So the BC-1 receives no light and hence the output of BC-1 is zero therefore S$_{3U}$ receives no light. Hence the final Output after BC-3 is 0. This result cannot be changed by any value of Y.

2. Similarly when Y=0, Y$_1$=Y$_2$=0 so all the incoming signals of S$_2$ and control signal of S$_4$ and S$_3$ is zero hence S$_{4U}$=S$_{2L}$=C$_2$=S$_{3U}$=0 i.e. receive no light. So the final Output after BC-3 is 0. This result cannot change by any value of X.

3. When X=1($\updownarrow$), X$_1$=1 and X$_2$=0. So S$_{1L}$ & S$_{4U}$ receives no light (as incoming signal of S$_1$ and S$_4$ is absent). And C$_1$=1 ($\updownarrow$) i.e. vertically polarized light.

   - Now as Y=1($\updownarrow$) then Y$_1$=1, Y$_2$=0. So S$_{2L}$=0 (as incoming signal of S$_2$ is absent), C$_2$=1. So S$_{3U}$=1 (as C$_2$ is the incoming signal of S$_3$). So the final Output after BC-3 is 1 ($\updownarrow$).

   - When Y=2 ($\bullet$) i.e. horizontally polarized light, then Y$_1$=0 (no light) and Y$_2$=2. So S$_{2L}$ and hence C$_2$ receives vertically polarized light (1 i.e. $\updownarrow$). Hence S$_{3U}$=1. So the final Output after BC-3 is 1 ($\updownarrow$).

   - Now when Y=3 ($\leftrightarrow$), then Y$_1$=1,Y$_2$=2. So S$_{2L}$=1 (as incoming signal is present but control signal is absent at S$_2$), C$_2$=1. Hence S$_{3U}$=1. So the final Output after BC-3 is 1 ($\updownarrow$).

4. When X is 2 ($\bullet$) and Y is 1 ($\updownarrow$), then X$_1$ & Y$_2$ receives no light. That means here, X$_1$ =0 & Y$_2$ =0 and Y$_1$=1, X$_2$=2. Hence S$_{4U}$=S$_{2L}$=0 (as the control signal of S$_4$ and incoming signal of S$_2$ is absent) and S$_{1L}$=C$_1$=C$_2$=1 i.e. vertically polarized light. So S$_{3U}$=1 as both the incoming and control signal of S$_3$ are present. So the final Output after BC-3 is 1 ($\updownarrow$).

5. When X=Y=2 ($\bullet$) i.e. both of them are horizontally polarized light, then X$_1$ & Y$_1$ receives no light (0) and X$_2$ & Y$_2$ receives horizontally polarized light (2). Hence S$_{4U}$=2 and S$_{2L}$=0

(as both the incoming and control is present of S_4 and S_2) As $Y_1=S_{2L}=0$. So $S_{3U}=0$. So the final Output after BC-3 is 2 ($\bullet$).

6. When X takes horizontally polarized light i.e. 2 ($\bullet$) and Y is partially polarized light i.e.3 ($\leftrightarrow$) then X_1 receives no light (0) and Y1=1, X2=Y2=2. Hence $S_{4U}=2$ and $S_{2L}=0$, $C_2=1$. Again as $X_2=Y_2=2$, then $S_{1L}=C_1=0$ (as both the incoming and control signal are present at S_1). As C_1 is the incoming signal of S_3, hence $S_{3U}=0$. And the final Output 2 ($\bullet$).

7. When X=3 ($\leftrightarrow$), then $X_1=1$ and $X_2=2$. When Y=1, then $Y_1=1$ and $Y_2=0$. So $S_{4U}=S_{2L}=0$ (as the control signal is absent in S_4 and the incoming signal is absent in S_2) and $S_{1L}=1$ (as incoming is present but control signal is absent in S_1). So $C_1=C_2=1$, hence $S_{3U}=1$. So final Output is 1 ($\updownarrow$).

8. When X=3 ($\leftrightarrow$), then $X_1=1$ and $X_2=2$. When Y=2 ($\bullet$), $Y_1=0$ and $Y_2=2$. So $S_{4U}=2$ and $S_{2L}=S_{1L}=0$. So $C_1=1$ and $C_2=0$, hence $S_{3U}=0$. So the final output is 2 ($\bullet$).

9. When X & Y both are partially polarized light i.e. 3 ($\leftrightarrow$), Then $X_1=Y_1=1$ and $X_2=Y_2=2$. So S_{4U} receives horizontally polarized light (2 i.e. $\bullet$) and $S_{2L}=S_{1L}=0$. Hence $C_1=C_2=1$, hence $S_{3U}=1$. So final Output is 3 ($\leftrightarrow$).
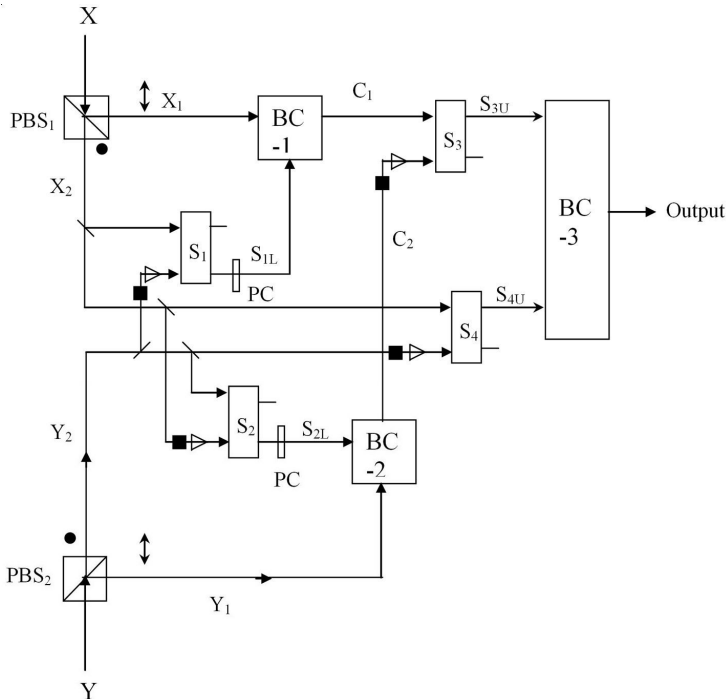

Figure 9. All-optical Quaternary QMIN(X,Y) Circuit. S (Switch): PBS : Polarizing Beam Splitter BC : Beam Combiner PC : Polarization Converter, ► EDFA : Erbium Doped Fiber Amplifier, ■ : WC Wavelength Converter.

2.3. All-optical Quaternary delta LITERALS

Literals are very important function in multi-valued logic based information processing [67]. The truth table of Delta literal circuit [66] is in the Table 2 and the circuit diagram is shown in the Fig. 10. Here, X is the quaternary input, which can take any one of the four quaternary logic states and the output is x^0, x^1, x^2 and x^3 respectively.

Input X	Output			
	X⁰	X¹	X²	X³
0	3	0	0	0
1	0	3	0	0
2	0	0	3	0
3	0	0	0	3

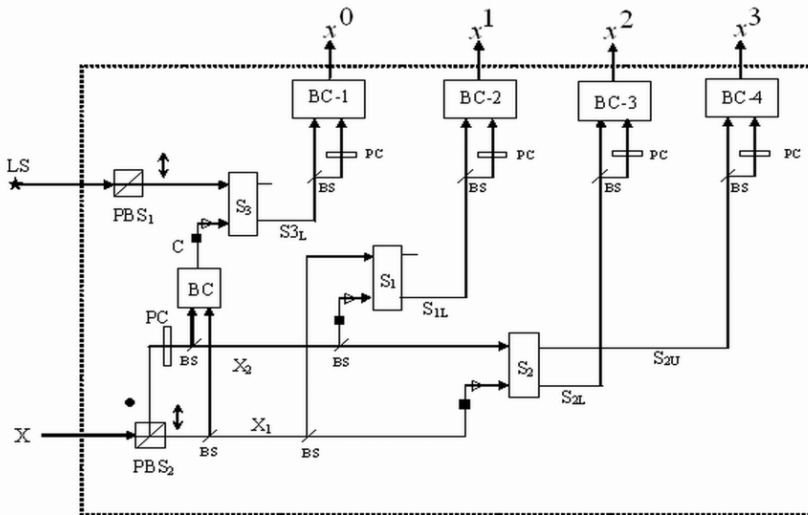**Table 2.** Truth table of quaternary delta Literals.

Figure 10. All-optical Quaternary Delta Literal Circuit.

1. When X=0 (absent of light), X_1 & X_2 receives no light and the other outputs of the switch S_1, S_2 are 0 as they receives no light. Here only vertically polarized light (↕), which comes from LS through PBS_1, falls on S_3. This act as incoming signal. Here as control signal is absent (because of C=0) the light comes out through lower channel of S_3 i.e. through S_{3L}. A part of this directly enters in the beam combiner (BC) and another part is passed through PC, which converts vertically polarized (↕) to horizontally polarized

light ($\bullet$). And hence the output of BC-1 is x^0 receives partially polarized light i.e. 3 ($\leftrightarrow$). Hence the final outputs are x^0=3($\leftrightarrow$) i.e. partially polarized light and others receives no light i.e.x^1=0, x^2=0andx^3=0.

2. When X=1 ($\updownarrow$), then X_1=1, X_2=0 and C=1. So S_{3L}=0 as control signal of S_3 is present and S_{1L}=1 ($\updownarrow$) as control signal of S_1 is absent. Other outputs (S_{2U}& S_{2L}) of the switch S_2 are absent, as the incoming signal of S_2 is absent. So the final outputs arex^0=0, x^1=3($\leftrightarrow$), x^2=0andx^3=0.

3. When X=2 ($\bullet$), then X_1=0, X_2=1 and C=1. So S_{3L}=0, S_{1L}=0 as the incoming signal of S_1 is absent. S_{2U}=0 and S_{2L}=1 ($\updownarrow$), because control signal of S_2 is absent. Hence the final outputs arex^0=0, x^1=0, x^2=3($\leftrightarrow$) andx^3=0.

4. When X is partially polarized light i.e.3 ($\leftrightarrow$), then all the X_1, X_2& C receives vertically polarized light i.e.1. So S_{3L}= S_{1L}= S_{2L}=0 and S_{2U}=1 ($\updownarrow$) as both the incoming and control signal of S_3, S_1 and S_2 are present. So the final outputs arex^0=0, x^1=0, x^2=0and x^3=3 ($\leftrightarrow$).

2.4. Design of All-optical Quaternary Multiplexer (4:1) :

From the truth Table 3 (truth table of QMIN gate) we can say that,

$$\left. \begin{array}{c} 3 \wedge A = A \\ 0 \wedge A = 0 \end{array} \right\} \quad where \; A \in \{0,1,2,3\} \tag{8}$$

Now we design quaternary multiplexer (QMUX) and demultiplexer (QDEMUX) using the basic gates QMIN and Delta Literal, made by switching character of the non-liner material based switch [66].

Control input signal (X)	QMUX Output (Y)	QDEMUX Outputs			
		Y_0	Y_1	Y_2	Y_3
0	A	A	0	0	0
1	B	0	B	0	0
2	C	0	0	C	0
3	D	0	0	0	D

Table 3. Truth Table of Quaternary Multiplexer (QMUX) and Demultiplexer (QDEMUX).

Multiplexing means many into one. A multiplexer is system dealing with many inputs and only with single output. A quaternary multiplexer with n-control inputs can be used to route one of 4^n data inputs (it may be any one of the four logical states) to the output. Fig. 11

is the design of 4:1 all-optical quaternary multiplexer. Here four inputs A, B, C and D [which can be any one of the 4-logical state i.e. 0(no light), 1($\updownarrow$), 2 ($\bullet$), 3 ($\leftrightarrow$)] are connected to four 2-input QMIN gates (QMIN$_0$, QMIN$_1$, QMIN$_2$, and QMIN$_3$). Other input of the QMIN is fed from one of the Delta Literal outputs (i.e. x^0, x^1, x^2 and x^3) respectively as shown in Fig. 11. These inputs of QMIN are act as a select line.
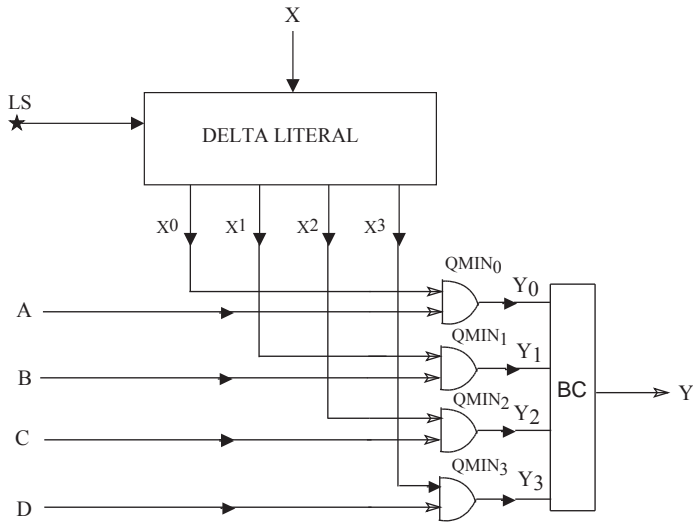

Figure 11. All optical Quaternary 4:1 Multiplexer (QMUX).

1. When X (delta literal input) is zero i.e. with no signal (0), then x^0 receives the logical state 3 ($\leftrightarrow$) i.e. partially polarized light and others outputs of the delta literal (x^1, x^2 and x^3) receive no light (0) as discussed in earlier section. As x^0 is connected with QMIN$_0$, then according to the equation no 7, only QMIN$_0$ is active and others QMIN gates (QMIN$_1$, QMIN$_2$ and QMIN$_3$) are inactive. Hence the corresponding input A is at the output i.e. Y_0 = A. and Y_1 = Y_2 = Y_3 =0. Hence after combining in BC we receives Y = A at the outputs.

2. When X is vertically polarized light i.e. 1 ($\updownarrow$), then only x^1 receives the logical state 3 ($\leftrightarrow$). & x^0 = x^2 = x^3 =0 (no light). As x^1 is connected with QMIN$_1$, then according to the equation no (2) only QMIN$_1$ is active and QMIN$_0$, QMIN$_2$ and QMIN$_3$ are inactive. Hence Y_1 = B & Y_0 = Y_2 = Y_3 =0 and at the final output we receives Y = B.

3. When X is horizontally polarized i.e. 2 ($\bullet$), then only x^2 receives the logical state 3 ($\leftrightarrow$). And x^0 = x^1 = x^3 =0 (No light). Hence only QMIN$_2$ is active and QMIN$_0$, QMIN$_1$ and QMIN$_3$ are inactive. Hence Y_2 = C & Y_0 = Y_1 = Y_3 =0 and at the final output, we receives Y = C.

4.   When X is partially polarized light i.e. 3 ($\leftrightarrow$), then only x^3 receives the logical state 3 ($\leftrightarrow$). And $x^0 = x^1 = x^2 = 0$ (no light). Hence only $QMIN_3$ is active and others $QMIN_0$, $QMIN_1$ and $QMIN_2$ are inactive. Hence Y_3 = D & $Y_0 = Y_1 = Y_2 = 0$ and combining, at the final output we receives Y = D. The truth table of this circuit is shown in the Table 3 (second column).

2.5. Design of All-optical Quaternary Demultiplexer (1:4):

A quaternary demultiplexer has the opposite function of QMUX. Here one input data is passed to one of the outputs according to the selection of the control. Fig. 12 is the design of 1:4 all-optical quaternary demultiplexers. Here one Input A is fed to every four 2-input QMIN gate as one input light (light from A is split by three beam splitters (BS) and fed to four 2-input QMIN gates) and other input of the QMIN is fed from one of the Delta Literal outputs (i.e. x^0, x^1, x^2 and x^3) respectively. These inputs of QMIN gates act as select line. This circuit act like same way as multiplexer circuit i.e. one QMIN is active (depends on the selection of the control line) and others QMIN gates are inactive. The active QMIN gate passes the input data from A which may be one of the four logical sate. The final outputs are taken from the combination of four QMIN output line (Y_0, Y_1, Y_2 and Y_3) as shown in Fig. 12. The truth table is shown in the Table 3 (third column).
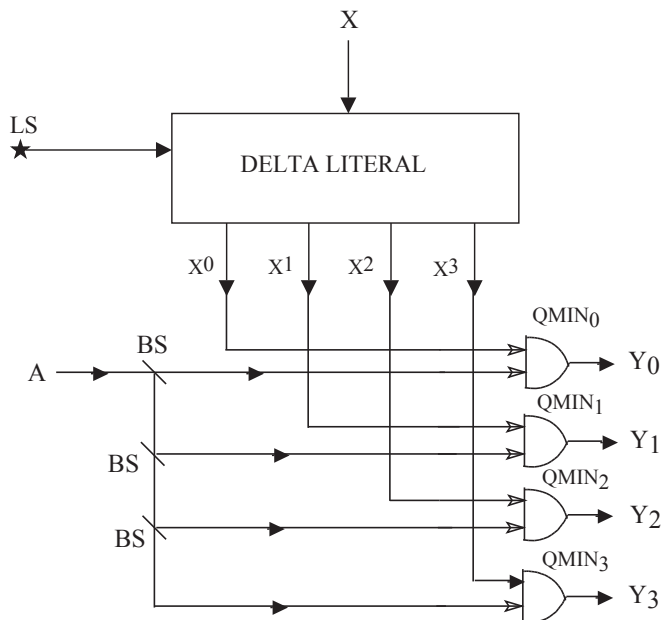

Figure 12. All optical Quaternary 1:4 Demultiplexer (QDEMUX).

3. Quaternary T-gate:

In section 2.4 we have reported all-optical 4:1 all-optical quaternary multiplexer. It is also known as 'T-Gate' [82]. The schematic diagram for quaternary T-gate is shown in Fig. 13. some logic operations are given in table 4.

Name of the functions	Symbol & mathematical expression	Inputs (logical states)				Outputs
		A	B	C	D	
Compliment / Inverter	$\bar{x} = (R-1) - x$	3	2	1	0	⟨3210⟩
Successor	$Suc(x) = (x+1) \bmod 4$	1	2	3	0	⟨1230⟩
Clockwise Cycle	$\widehat{X}_b = (x+b) \bmod 4$	1	2	3	0	$\widehat{X}_1 = ⟨1230⟩$
		2	3	0	1	$\widehat{X}_2 = ⟨2301⟩$
		3	0	1	2	$\widehat{X}_3 = ⟨3012⟩$
Counter Cycle	$\widehat{X}_{bc} = (x-b) \bmod 4$	3	0	1	2	$\widehat{X}_{1c} = ⟨3012⟩$
		2	3	0	1	$\widehat{X}_{2c} = ⟨2301⟩$
		1	2	3	0	$\widehat{X}_{3c} = ⟨1230⟩$
Literal	${}^a x^b = \begin{cases} (R-1) \text{ if } a \le x \le b \\ 0 \quad \text{otherwise} \end{cases}$	0	3	3	0	${}^1 x^2 = ⟨0330⟩$
		0	3	3	3	${}^1 x^3 = ⟨0333⟩$
		0	0	3	3	${}^2 x^3 = ⟨0033⟩$
Truncated Sum	$X \boxplus a = \begin{cases} (X+a) \text{ if, } X < (R-1) \\ (R-1) \quad \text{otherwise} \end{cases}$	1	2	3	3	$X \boxplus 1 = ⟨1233⟩$
Truncated difference	$X \boxminus a = \begin{cases} (X-a) \text{ if, } X \ge a \\ 0 \quad \text{otherwise} \end{cases}$	0	0	1	2	$X \boxminus 1 = ⟨0012⟩$
Threshold literals (up)	${}^U a(x) = \begin{cases} 1 \text{ if } x \ge a \\ 0 \text{ else} \end{cases}$	0	1	1	1	${}^U 1(x) = ⟨0111⟩$
		0	0	1	1	${}^U 2(x) = ⟨0011⟩$
Step literals (down)	${}^D a(x) = \begin{cases} 1 \text{ if } x \le a \\ 0 \quad \text{else} \end{cases}$	1	1	0	0	${}^D 1(x) = ⟨1100⟩$
		1	1	1	0	${}^D 2(x) = ⟨1110⟩$

Table 4. Some well-known one input quaternary logical functions (radix $R=4$) and design process with quaternary T-gate.

The mathematical expression for all-optical quaternary T-gate using MIN & delta literals can be written as:

$$O = \left(A \wedge x^{\langle 3000 \rangle} + B \wedge x^{\langle 0300 \rangle} + C \wedge x^{\langle 0030 \rangle} + D \wedge x^{\langle 0003 \rangle} \right) \tag{9}$$
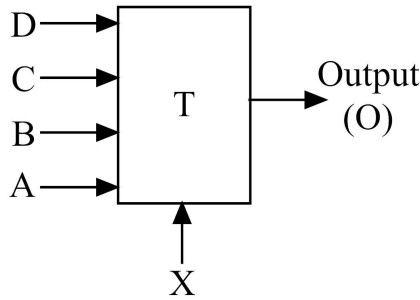

Figure 13. All optical Quaternary T-gate.

Where, '$\wedge$' is MIN operator ($x \wedge y$= minimum of (x, y)) and δ- literals function is $x^a = (R-1)$ if $x=a$, else 0] The four incoming data transmission lines are 'A', 'B', 'C' and 'D' [which can be any one of the 4-logical state i.e. 0 (no light), 1($\updownarrow$), 2 ($\bullet$), 3 ($\leftrightarrow$)] and 'X' is the selection input. By using proper section we can get any data (A, B, C or D) at the output. If X=0, the output is A, when X=1 then the output is B, for X=2 the output is C and when X=3 then the output is D respectively i.e. [82]:

$$T\left(A,B,C,D;x \right) = \begin{cases} A & \text{if } x = 0 \\ B & \text{if } x = 1 \\ C & \text{if } x = 2 \\ D & \text{if } x = 3 \end{cases} \tag{10}$$

This T-gate can successfully used for designing any quaternary circuits. So it is called 'universal' element of quaternary logic. Some quaternary logical operations with T-gate is shown in Table 4. Here inputs of T-gate A, B, C, and D are shown in colomn-3 of that table 4. X is the select input =$\langle 0123 \rangle$. Here the quaternary multiplexer or T-gate is all-optical in nature. Hence all the quaternary circuits are all-optical.

4. Challenges in designing the polarization encoded all-optical system:

Here, in this proposed scheme, we have proposed and described an all-optical circuit for designing quaternary (four-valued) multiplexer & de-multiplexer with the help of some polari-

zation encoded basic quaternary logic gates (quaternary min and quaternary delta literal). It is important to note that the above discussions are based on simple model. In order to experimentally achieve result from the proposed scheme, some design issues have to be considered. For example, polarization properties of fiber, predetermined values of the intensities, wavelength of laser light for control and incoming signals, introduction of filter, intensity losses due to beam splitters/fiber couplers etc. The output logical states of every ternary circuit can be determined by, stokes vector [S] measurement. Stokes vector can be calculated from the measurement of six intensities ($I_{i,j}$) in the photo detector (PD) by use of a linear analyzer (LA) followed by a quarter wave plate ($\lambda / 4$plate), which is shown in the Fig. 14. The formula for calculating stokes vector is [83]:

$$[S] = \begin{bmatrix} S_0 \\ S_1 \\ S_2 \\ S_3 \end{bmatrix} = \sqrt{\frac{\mu_0}{\varepsilon_0}} \begin{bmatrix} I_{(0,0°)} + I_{(0,90°)} \\ I_{(0,0°)} - I_{(0,90°)} \\ I_{(0,45°)} - I_{(0,135°)} \\ I_{\left(\frac{\lambda}{4},45°\right)} - I_{\left(\frac{\lambda}{4},135°\right)} \end{bmatrix} \tag{11}$$

Where first subscript ('i') index lack or presence of $\lambda / 4$ plate and the second ('j') gives the azimuth of the analyzer. μ_0 and ε_0 is free space permeability and permittivity. Degree of polarization (DOP) is also calculated by the equation:

$$\text{DOP} = \frac{\sqrt{S_1^2 + S_2^2 + S_3^2}}{S_0} \tag{12}$$

The value of DOP can be plotted in Poincaŕe sphere in point 'P' and we found that, for vertically ($\updownarrow$) and horizontally ($\bullet$) polarized light OP=DOP=1 and lies on the equator of the Poincaŕe sphere (at point y and x respectively).
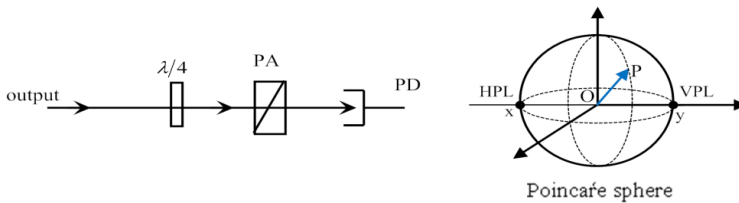

Figure 14. Measurement technique of output logical states.

In high speed data communication (50 GB/s or TB/s) random change of polarization in a short time can produce power fluctuation at the output. So polarization dependent loss

(PDL) degrades the optical signal to noise ratio (OSNR) and also degrades the extinction ratio. PDL of 3 dB could cause 1 dB power penalty [84]. Optical depolarizers can be used to reduce the polarization-induced noise in optical sensing and measurement systems [85]. Again random birefringence in optical fibers induces an unpredictable rotation of the sate of polarization (SOP); this can be adjusted by using polarization controller and PM fiber. Intrinsic cross talk between two polarization states, imperfection of polarized tracking after transmission link etc may cause polarization mode dispersion (PMD). This may cause the delay among the different states of polarization. The effects of PMD are expected to be similar to those of other approaches that have been studied in the literature [86]. Optical amplifiers degrade the signal-to-noise ratio (SNR) of the amplified signal because of spontaneous emission added to the signal during its amplification (ASE). The OSNR-errors arise in this process. For polarized signal PHB will cause ASE polarization orthogonal to the signal polarization. Bruyere et al [87] have shown that the DOP of ASE could exceed 70% in transoceanic links with low PMD. Of course, the most of ASE light does not traverse the entire light path, and then OSNR-errors become less as < 0.6 dB. Polarization related problem discussed above would occur inside the considered circuit. The said problem will not occur in optical communications system once the signal comes out the output. State of polarization may be changed if it is passed through bi-refringent crystals or optically active substances. The significant advantage of this proposed scheme is that the schemes are all-optical in nature and can be easily and successfully be extended for higher order multiplexer and demultiplexer. As an example, for 16:1 multiplexer, 16-select lines can be constructed by two Delta literals outputs and 16-QMIN gates. Now select lines are to be fed to again 16-QMIN gate as first input and the second input is to be taken from the input signals. By selecting proper select line we can transfer any one of 16-input signals to the output. This scheme is easily practicable as the components of our design are technically highly developed and widely used in optical communication. The proposed scheme will work with other 2x2 Interferometric switches (like Mach–Zehnder interferometer) also.

5. Conclusions and Future Scopes:

In present day digital signal processing is based on conventional binary number system (radix = 2). It has two logical states 'LOW' and 'HIGH'. Binary logic (or logic for that matter) is NOT a law of nature. The reason why binary logic seems more natural is because we have been more exposed to it. The perspective MVL is more like an extension of binary logic and very conventional, though broader in possibilities. In a wide sense, a signal may be anything that can be observed to have states that change in time and space. In narrow sense, a signal is a physical quantity that can be measured, usually by an electronic device. Signals, as conveyers of information about the state of a system, should be processed to extract and understand the information content encoded. Nowadays, digital systems, and sometimes mixed-signal systems, are prevalent in information transmission, storage, and processing. However, enormous, and ever increasing, amounts of information that can be handled, even in everyday life, focus attention to multiple-valued (MV) logic, which permit more compact

encoding of information within the same amount of digits. Although, having certain considerable demerits, multiple-valued logic is viewed as promising alternatives in many practical solutions. Many contemporary logic design technologies are oriented towards supporting an efficient implementing of various signal processing algorithms. In order to entirely exploit all the available resources, sophisticated methods are required. Humans count by tens, machines count by twos, these sums up the way we do arithmetic today. However, there are countless other ways to count. Challenges and opportunities are wide.

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