
Subsampling Receivers with Applications to Software Defined Radio Systems

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<http://dx.doi.org/10.5772/49959>

1. Introduction

There are currently a large number of different communication standards, due to the widespread acceptance of wireless technologies. As a consequence, there is a tendency to design transceivers for multiple standards [1-8]. A similar problem arises in the test industry, where providers of testing and certification services to the wireless communication industry need multi-standard receivers, in order to reduce the cost in testing equipment.

With the topology of a multi-standard receiver, the placement of the analog-to-digital converter (ADC) within the front-end chain is crucial, as shifting of the analog blocks (filter, mixer and amplifier) to the digital domain increases the flexibility of the receiver. The extreme case is known as the software defined radio (SDR) paradigm [9,10], where the ADC is placed right behind the antenna to directly digitize the radio frequency (RF) signal. For current communication standards, this approach imposes requirements on the ADC beyond the state of the art, where the ADC is limited to 7-8 bits for a sampling rate of 3 GS/s.

Different receiver architectures have been proposed to overcome this problem, such as direct conversion [11], low intermediate frequency (IF) [12], and subsampling [13,14]. In subsampling receivers, the RF signal is sampled using a frequency lower than twice the maximum input frequency, but larger than two times the signal bandwidth. One of the low-frequency replicas resulting from the sampling process, which contains the baseband signal, is then directly digitized.

Flexibility is the main advantage of a subsampling technique when using a sample and hold device (S&H) to produce low-frequency replicas of the RF signal, because most of the signal

processing is done in the digital domain. In addition, it reduces the number of analog building blocks and relaxes the specifications of the ADC. On the other hand, the drawbacks of subsampling are the demanding specifications required for the S&H (wide input bandwidth and low aperture jitter) and high noise, due to folded thermal noise in the band of interest. In order to reduce the folded noise effect, a technique based on multiple clocking is proposed.

Due to the emergence of several coexisting wireless technologies, subsampling techniques can be useful in the implementation of a receiver for multi-band applications [15]. A multi-band receiver subsampling technique may be used in other applications, such as the feedback loop for linearization of dual-band power amplifiers in RF transmitters [16]. In both nonlinear and multi-band cases, the data acquisition involved in the subsampling receiver has additional limitations, because the harmonics (nonlinear case) and other carrier frequencies (multi-band case) are subsampled and may overlap with the signal of interest. Therefore, determination of the valid sampling frequencies in these scenarios is a major challenge. In this chapter, a particular case for dual-band applications in a nonlinear environment is studied, integrating both effects. Possible architectures to optimize the data acquisition resolution are described.

A data acquisition board based on subsampling for high-performance low-cost multi-standard test equipment is presented. With a signal bandwidth of 20 MHz, it achieves an 8.5 bit resolution for a programmable carrier frequency ranging from 0 up to 3.3 GHz and resolutions of more than 8 bits up to 4 GHz. With the proper selection of the center frequency and signal bandwidth, the proposed board can be used to digitize the signal in most of the current wireless standards. This design is intended to be part of a test system, i.e., the input signal of the subsampling receiver is assumed to be filtered and free of interferences.

Finally, an improvement based on multiple clocking techniques is employed to improve the resolution of the presented data acquisition system. By using two consecutive subsampling stages, this approach allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to the folded thermal noise. Considering a signal bandwidth of 20 MHz, the improved data acquisition system achieves an effective number of bits (ENOB) of more than 9 for a programmable carrier frequency up to 2.9 GHz and of 8 up to 6.5 GHz, presenting an improvement of 0.5-1 bit in the resolution.

This chapter is organized as follows: Section 2 reviews the signal representation and definitions for wireless communication signals, while Section 3 reviews the sampling theory. Section 4 describes the theoretical concept of subsampling techniques, detailing their advantages and main drawback of jitter and folded noise. An approach based on multiple clocking is proposed, in order to reduce the effect of folded noise on the resolution. In this section, the typical problems of subsampling techniques are extended to multi-standard and nonlinear applications, and an optimization for receivers in these scenarios is also proposed. Finally, Section 5 describes the implementation of a data acquisition system and presents a comparison with other published multi-standard receivers. Conclusions are described in Section 6.

2. Signal representation and definitions

In current wireless communication links (Figure 1), a complex modulated baseband signal, $s(t)$, containing the useful information can be expressed as:

$$s(t) = A(t)e^{j\varphi(t)} = I(t) + jQ(t) = A(t)\cos\varphi(t) + jA(t)\sin\varphi(t) \quad (1)$$

where $A(t)$ and $\varphi(t)$ are the amplitude and phase of the complex baseband signal, and $I(t)$ and $Q(t)$ are the in-phase and quadrature-phase representation of the signal. This signal is usually up-converted to an RF bandpass signal around the carrier frequency, f_c , to be transmitted through a wireless channel and detected by a receiver and converted back to baseband. The bandpass transmitted signal can be written as follows:

$$\tilde{s}(t) = \Re[s(t)e^{jw_c t}] = \Re[A(t)e^{j\varphi(t)}e^{jw_c t}] = A(t)\cos(w_c t + \varphi(t)) \quad (2)$$

where $w_c = 2\pi f_c$ and the transmitted signal, $\tilde{s}(t)$, is the real part ($\Re[\cdot]$) of the complex envelope of the RF bandpass signal after up-conversion. In practical situations, the bandwidth of the baseband signal is much less than the carrier frequency, f_c .

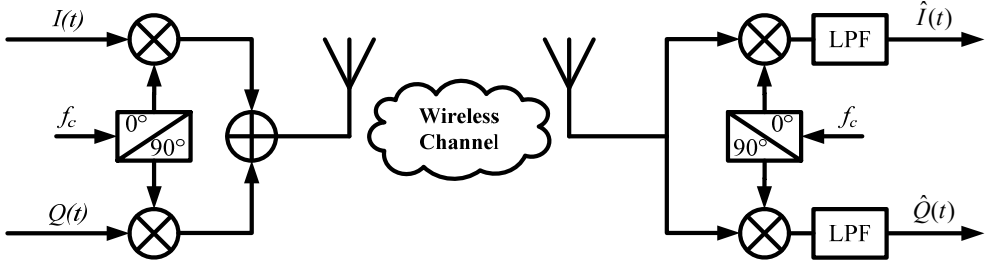


Figure 1. A typical wireless link

The radio channel is modeled as a linear time-invariant system; however, due to the different multipath waves that have propagation delays, which vary over different spatial locations of the receiver, the impulse response of the linear time-invariant channel should be a function of time, t , and the position of the receiver, d . The channel can, therefore, be described by $h(d, t)$.

The bandpass signal at the mobile receiver can be expressed as:

$$\tilde{s}_R(d, t) = \tilde{s}(t) \otimes h(d, t) \quad (3)$$

In the case of a stationary receiver, Equation (3) can be reduced to:

$$\tilde{s}_R(t) = \tilde{s}(t) \otimes h(t, \tau) = \int_{-\infty}^t \tilde{s}(\tau) h(t - \tau) d\tau \quad (4)$$

The received baseband signal can be obtained from a frequency down-conversion and channel equalization of the received bandpass signal as follows:

$$\begin{aligned}
\hat{s}(t) &= (\tilde{s}_R(t)e^{-jw_c t}) \otimes h^{-1}(t, \tau) \\
&= \frac{1}{2} \hat{A}(t) \cos \hat{\phi}(t) + \frac{1}{2} \hat{A}(t) \cos \hat{\phi}(t) \cos 2w_c t - \frac{1}{2} \hat{A}(t) \sin \hat{\phi}(t) \sin 2w_c t \\
&\quad + \frac{1}{2} j \hat{A}(t) \sin \hat{\phi}(t) - \frac{1}{2} j \hat{A}(t) \sin \hat{\phi}(t) \cos 2w_c t - \frac{1}{2} j \hat{A}(t) \cos \hat{\phi}(t) \sin 2w_c t
\end{aligned} \tag{5}$$

The high-frequency components ($2w_c t$) are filtered out using low-pass filters (LPFs), as shown in Figure 1. The in-phase/quadrature-phase (I/Q) component of the received baseband signal can be expressed as:

$$\hat{I}(t) = \hat{A}(t) \cos \hat{\phi}(t) \quad \text{and} \quad \hat{Q}(t) = \hat{A}(t) \sin \hat{\phi}(t) \tag{6}$$

Knowing the transmitted signal, $s(t)$, and the received and equalized signal, $\hat{s}(t)$, one can calculate the normalized mean squared error (NMSE) as follows:

$$\text{NMSE}[\%] = \sqrt{\frac{\sum_{n=1}^N |s[n] - \hat{s}[n]|^2}{\sum_{n=1}^N |s[n]|^2}} \times 100\% \tag{7}$$

where N is the length of the data segment, and $s[n]$ and $\hat{s}[n]$ are the sampled versions of $s(t)$ and $\hat{s}(t)$, respectively.

3. Review of sampling theory

At the receiver end of the communication system, the RF signals are decomposed into their respective I and Q baseband components. A continuous time domain signal, $x(t)$, should be sampled, so that the signal can be reconstructed without losing any information. Using ADCs, the continuous time domain signal is converted to a discrete time domain signal, $x[n]$, through a uniform sampling process taken during the sampling period, T_s ; and, their relation is $x[n] = x(nT_s)$.

Discrete time sampling affects the resolution of the final time domain signal being processed. If we consider a sine wave operating at 200 Hz and the continuous time domain signal representation as shown in Figure 2a, with a sampling frequency of 10 kHz, the sine wave is still visible in Figure 2b. However, the use of a sampling rate of 2 kHz, as in Figure 2c, results in a less accurate representation of the sine wave.

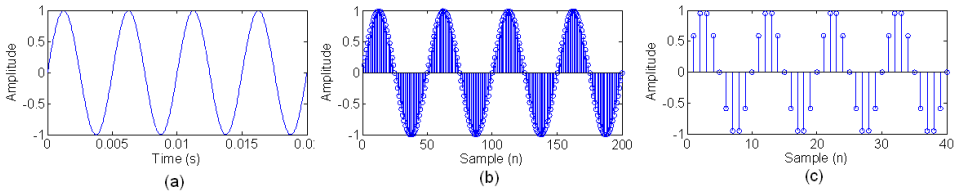


Figure 2. Time domain representation of (a) 200 Hz continuous sine wave (b) sampled at 10 kHz and (c) sampled at 2 kHz

The discrete time signal, $x[n]$, can be viewed as a multiplication of the continuous wave function, $x(t)$, with a train of impulse functions [17]. The sampled version of the signal can be expressed as:

$$x_s(t) = x(t)\delta_T(t) = \sum_{n=-\infty}^{\infty} x(nT_s)\delta(t - nT_s) \quad (8)$$

The impulse train can be further expressed as a Fourier series:

$$\delta_T(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \xrightarrow{\mathcal{F}} \omega_s \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_s) \quad (9)$$

where $\omega_s = 2\pi/T_s$.

Since a multiplication in the time domain results in convolution in the frequency domain, the Fourier transform of the sampled signal, $X_s(\omega)$, in relation to the RF signal's Fourier transform, $X(\omega)$, is:

$$X_s(\omega) = \frac{1}{2\pi} X(\omega) * \left[\omega_s \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_s) \right] = \frac{1}{T_s} X(\omega) * \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_s) \quad (10)$$

Using the convolution property of the impulse function, the simplified version of the impulse-modulated signal becomes:

$$X_s(\omega) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X(\omega - k\omega_s) \quad (11)$$

This shows that the spectrum is replicated every ω_s .

Choosing a sampling frequency for a band-limited signal affects the reconstruction process. A band-limited signal with total bandwidth (BW) is illustrated in Figure 3. For Figure 3a, the sampling frequency, $f_s = 1/T_s = \omega_s/2\pi$, is much larger than the bandwidth; and, perfect reconstruction is possible. Similarly, for the case when $f_s = BW$ as in Figure 3b, the spectra do not overlap or alias over each other; and, the signal can still be decoded properly. However, in Figure 3c, f_s is less than BW , and aliasing occurs over the signal. This aliasing corrupts the information in the signal, making it unrecoverable. The minimum sampling rate (or the Nyquist sampling rate) should be $f_s \geq BW$ in order to correctly decode the signal.

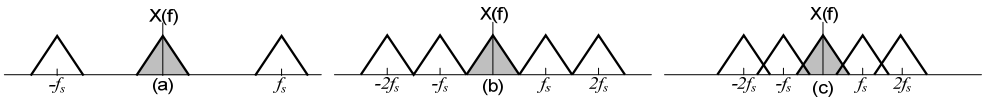


Figure 3. Sampling of a signal using (a) $f_s \gg BW$ (b) $f_s = BW$ and (c) $f_s < BW$

4. Theory of operation

This section introduces the subsampling concept and details the method to select the optimal sampling frequency. Then, the two main limitations of the subsampling based systems, i.e., jitter and folded thermal noise, are described. Finally, the concept of subsampling is extended to nonlinear systems and multi-band applications, describing a method to optimize the performance in terms of noise.

4.1. Concept of subsampling

As mentioned before, moving the ADC closer to the antenna increases the flexibility of the receiver; however, this conversion just after the antenna prohibitively increases the ADC's bandwidth and sampling frequency requirements. Nevertheless, the bandwidth of a bandpass signal is usually a fraction of its center frequency, so that it is possible to subsample the signal (i.e., violating the Nyquist condition), thereby avoiding aliasing between replicas.

Subsampling is the process of sampling a signal with a frequency lower than twice the highest signal frequency, but higher than two times the signal bandwidth. An ideal S&H with a sampling frequency of f_s generates harmonics at $f_s, 2f_s, \dots, mf_s$, where m is an integer. In the case for Figure 4a, a bandpass RF signal is centered at f_c , while the m^{th} closest harmonic generated by the S&H and lower than f_c is k , where $k = \text{floor}(f_c/f_s)$. The replicas of the signal that are generated by the S&H exist at $-mf_s + f_c$, while the mirrored versions replicas exist at $(m+1)f_s - f_c$. Figure 4b shows these replicas, and the signal replica within the 0 to $f_s/2$ range (centered at $f_i = f_c - kf_s$) can be used to extract the original RF signal.

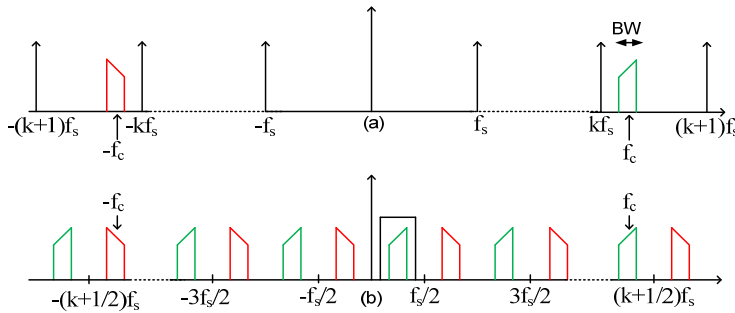


Figure 4. Illustration of the concept of subsampling: (a) frequency domain representation of the RF bandpass input signal along with the subsampling frequency and S&H harmonics and (b) signal replicas following subsampling process when selecting $f_s = (f_c - f_{ij})/k$ and $f_s > BW$

4.2. Selecting the sampling frequency

This section provides the method to select the optimal sampling frequency (f_s) for a given signal bandwidth (BW) and carrier frequency (f_c). Usually, the minimal sampling frequency is determined by the Nyquist theorem: $f_s > 2(f_c + BW/2)$. However, for a bandpass signal, a

sampling frequency lower than the Nyquist frequency can be selected if Expression (12) still holds [14]:

$$2(f_c - BW/2)/(m-1) > f_s > 2(f_c + BW/2)/m \quad (12)$$

where m is the number of replicas of the signal spectrum in the range $[0, f_c - BW/2]$ and lies between 1 and $\text{floor}((f_c + BW/2)/BW)$. An appropriate value is $f_s = 4f_c/m_{\text{odd}}$, which produces a replica at $f_s/4$. Using an odd integer m_{odd} ensures that the signal is at $f_s/4$, while m_{even} generates the low-frequency alias of the signal at $3f_s/4$.

An example that illustrates the convenience of sampling at $4f_c/m_{\text{odd}}$ can be observed in Figure 5, which shows the output spectrum when an input signal at 1070 MHz is sampled at the f_s of 475.56 MHz (Figure 5a). Figure 5b shows the effect of selecting a non-optimal sampling frequency of 480 MHz; in such a case it can be seen how the second-order harmonic of the input signal is subsampled to 220 MHz, and falls closer to the subsampled fundamental at 110 MHz. Therefore, sampling at $4f_c/m_{\text{odd}}$ results in a larger subsampling frequency bandwidth and relaxes the filtering requirements after the S&H. As f_s , f_c and f_{if} are all directly related, there are bandwidth and frequency tradeoffs when selecting the subsampling frequency.

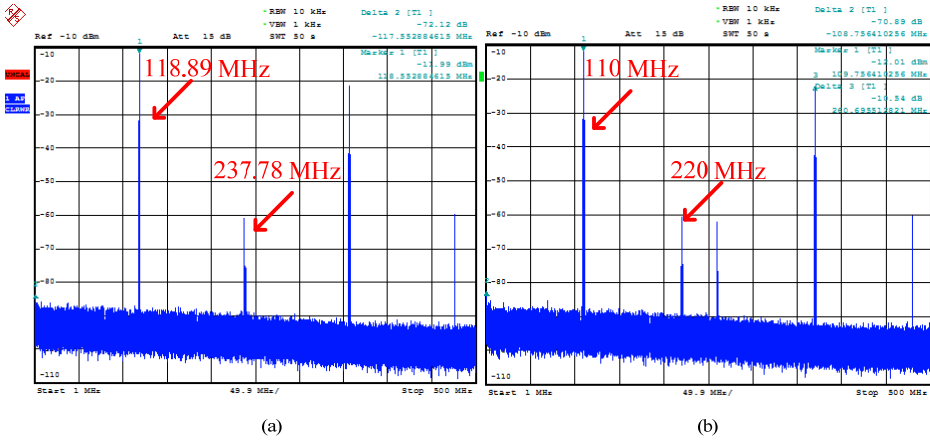


Figure 5. Output spectrum of the subsampler when a 1070 MHz RF signal is subsampled at the f_s of (a) 475.56 MHz ($m_{\text{odd}}=9$ and $f_{if}=118.89$ MHz) and (b) 480 MHz ($f_{if}=110$ MHz)

4.3. Main non-idealities of a subsampling system

A general scheme for a subsampling receiver is shown in Figure 6. It should be mentioned that this receiver is very simple, especially if compared to conventional heterodyne architecture. However, as the S&H processes high-frequency signals, its requirements are much more restrictive than those expected from the signal bandwidth. The main non-idealities to be considered in the S&H are jitter and folded thermal noise, which are described in Subsections 4.3.1 and 4.3.2.

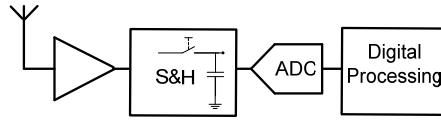


Figure 6. Subsampling receiver scheme

4.3.1. Jitter

Clock jitter is an important limitation in data acquisition systems at high signal frequencies, leading to sampling time uncertainty. Jitter is the deviation of the reference edges of the clock signal with respect to their ideal position in time. In this chapter, we consider this deviation as a random noise. As shown in Figure 7, a random error, τ_n , from the nominal sampling time instant, t_n , causes a random error, $\varepsilon_r(n)$, in the amplitude of the sampled signal [18]. This effect can be seen as an addition of noise to the output signal, resulting in a degradation of the output signal-to-noise ratio (SNR).

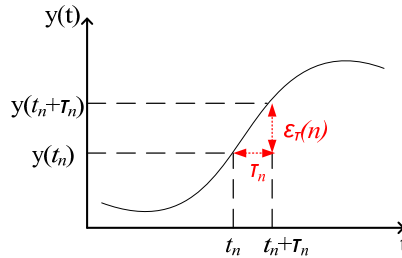


Figure 7. Concept of jitter

The amplitude error (v_{error}) is proportional to the derivative of the input signal [19]:

$$v_{error} = \Delta t \frac{dv_{in}}{dt} \quad (13)$$

With a jitter value of Δt .

For a sine wave of frequency f_{in} and amplitude A_{in} , the maximum error is [19]:

$$v_{error_max} = \Delta t A_{in} 2\pi f_{in} \quad (14)$$

There are two main sources of jitter noise: the phase noise associated with the clock reference, and the aperture jitter of the S&H. The aperture jitter of an S&H implemented with a MOS (metal oxide semiconductor) transistor is signal dependent, as the transistor threshold voltage depends on the input signal. There are two primary mechanisms that cause jitter in the system clock: the thermal noise, and the coupling noise. The latter can be caused by crosstalk and/or ground loops within, or adjacent to, the area of the circuit. Special care has to be taken in the design of the power lines in the data acquisition board, as described in Section 5.1.

In a first-order approach, these two sources of jitter noise can be considered as uncorrelated Gaussian stochastic processes: each one with a particular standard deviation. With Δt_{rms} as the standard deviation (or root mean square) of jitter, which usually defined as a percentage of the sampling period, the sampling error in Expression (13) can be rewritten as [19]:

$$\sigma(v_{error}) = \Delta t_{rms} \sigma(dv_{in} / dt) = \Delta t_{rms} 2\pi f_{in} \frac{A_{in}}{\sqrt{2}} \quad (15)$$

where $\sigma(.)$ is the standard deviation.

Therefore, the resulting SNR on the sampled signal is [19]:

$$SNR_{jitter} = 20 \log \left(\frac{A_{in} / \sqrt{2}}{\Delta t_{rms} 2\pi f_{in} \frac{A_{in}}{\sqrt{2}}} \right) = -20 \log(\Delta t_{rms} 2\pi f_{in}) \quad (16)$$

Note that the SNR is degraded when the input frequency increases.

This approximation is true if $2\pi f_{in} \Delta t_{rms} \ll 1$; otherwise, the general expression for the SNR, due to the uncorrelated random jitter noise for a sinusoidal input signal, can be expressed as follows [18,20]:

$$SNR = 20 \log \left(\begin{cases} 1 / 4\pi^2 f_{in}^2 \Delta t_{rms}^2 : 2\pi f_{in} \Delta t_{rms} \ll 1 \\ 1 / 2(1 - e^{-2\pi^2 f_{in}^2 \Delta t_{rms}^2}) : otherwise \end{cases} \right) \quad (17)$$

The expression of SNR for $2\pi f_{in} \Delta t_{rms} \ll 1$ is valid for all jitter distributions, while the other SNR expression only applies to a random jitter with a Gaussian distribution ($N(0, \Delta t_{rms})$) [18]. Moreover, small jitter noise can be regarded as approximately sampled additive white Gaussian noise (AWGN); whereas this assumption is not valid for large jitter.

In the particular case of subsampling, jitter noise is an important limitation, due to the high input frequencies that are processed. Thus, in order to validate this theoretical study, jitter noise is simulated using typical values for subsampling based receivers, i.e., input frequencies in the GHz range, sampling frequencies around 500 MHz (which is a typical limit for high-resolution commercial ADCs, as is described in Section 5.1) and a 20 MHz signal bandwidth, because it is a typical value for many communications standards and is used to experimentally characterize the data acquisition board proposed in Section 5.1.

Using these values, jitter noise has been simulated as a stochastic process (using MATLAB) with the average equal to zero and the standard deviation equal to Δt_{rms} . Figure 8a illustrates the maximum admitted jitter (X-axis) to obtain a concrete SNR (Y-axis) for three different input frequencies (1, 2 and 4 GHz) sampling at the optimal frequency (from equation $f_s = 4f_c / m_{odd}$) immediately lower than 500 MHz. In this example, the jitter noise is integrated in a signal bandwidth equal to 20 MHz; and, it can be observed that the SNR decreases around 6 dB each time the input frequency is doubled, as can be predicted by Expression (17).

This traditional method, based on Expression (17), to obtain the SNR as a function of clock jitter and signal frequency has some limitations, such as the assumption of a full-scale scenario. Although this situation may happen in some applications, the input signal energy is most commonly spread over some bandwidth. In these cases, it is more realistic to study the jitter effect from the spectrum domain. Since the spectrum of jitter is very difficult to measure directly [19], the most common method to study its effect is the measurement of the phase noise, which is the most widely employed parameter to compare between different clock sources and oscillators.

Phase noise is defined as the frequency domain representation of the phase modulation of the clock signal due to jitter. Since the clock signal is a sine wave of frequency f_s [19]:

$$v_{clock} = A \sin(2\pi f_s(t + \Delta t(t))) = A \sin(2\pi f_s t + \phi(t)) \quad (18)$$

where $\phi(t)$ is the phase noise in the time domain. Assuming $\phi(t)$ has a small variation around zero, Equation (18) can be written as [19]:

$$v_{clock} \cong A \sin(2\pi f_s t) + A \cos(2\pi f_s t) \phi(t) \quad (19)$$

The second term of Expression (19) is the additive noise due to phase modulation. Since the phase noise appears multiplied by a cosine in the above time domain expression, the spectrum of the phase noise in the frequency domain, $\Phi(f)$, is convolved with the noise-free clock and appears as sidebands around its center frequency. This noise is usually represented as $L(f)$ (single-sideband phase noise power spectrum) and is equal to the noise power spectral density per Hertz at the frequency of $f_s + f$, normalized by the clock or oscillator signal power, $A^2/2$. It is single-sideband, because only one side of the noise power is taken into account; hence, it includes only half the noise energy. Thus [19]:

$$\begin{aligned} L(f) &= 10 \log \left(\frac{1}{2} \Phi^2(f) \right) \\ \phi(f) &= \sqrt{2 \cdot 10^{L(f)/10}} \end{aligned} \quad (20)$$

$L(f)$ is measured in dBc/Hz.

Figure 8b shows an example of phase noise for a clock frequency equal to 1.9 GHz, which is in the typical frequency range for the S&H clock source in the implemented systems, as is detailed in Section 5.1. These experimental measurements show a phase noise of around -95 dBc/Hz, -110 dBc/Hz and -125 dBc/Hz at 100 Hz, 1 KHz and 10 KHz, respectively. From Expression (18), the relationship between $\phi(t)$ and jitter is [19]:

$$\phi(kT_s) = 2\pi f_s \Delta t(kT_s) \quad (21)$$

This is equivalent to referencing jitter to the clock period. In the frequency domain, where the clock phase noise is most commonly represented, it is then equal to the clock jitter scaled by $2\pi f_s$ [19]:

$$\Phi(f) = 2\pi f_s \Delta T(f) \quad (22)$$

Therefore, we have the following expression to obtain the total jitter from phase noise [19]:

$$\Delta t_{rms} = \frac{1}{2\pi f_s} \sqrt{\int_0^\infty \Phi^2(f) df} = \frac{1}{2\pi f_s} \sqrt{2 \int_0^\infty 10^{L(f)/10} df} \quad (23)$$

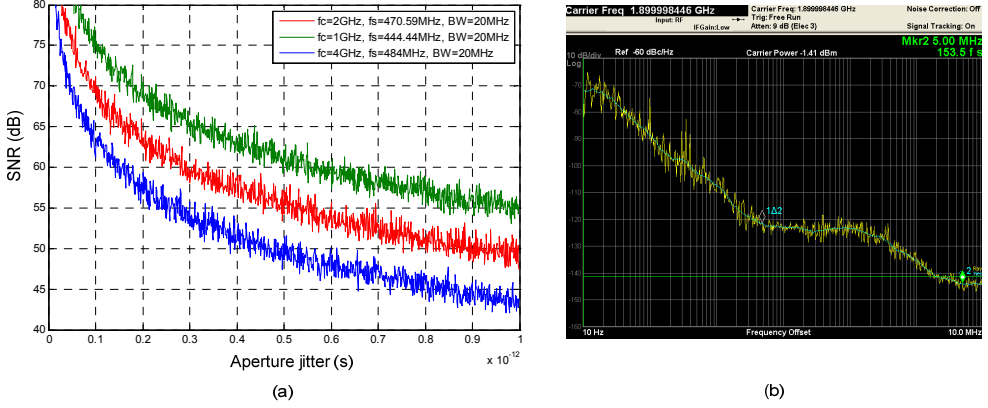


Figure 8.

4.3.2. Folded thermal noise

The other main non-ideality of the systems based on subsampling is the folded thermal noise. With the S&H modeled as shown in Figure 9a [18], this thermal noise is introduced by the switch and has a power spectral density (PSD) equal to $S_{in}(f) = 4kTR_{on}$, where k is the Boltzmann constant, T is the absolute temperature and R_{on} is the on-resistance of the switch. This noise is AWGN and is folded in the band of interest by the subsampling process, as is described in this section (Figure 9b [7]).

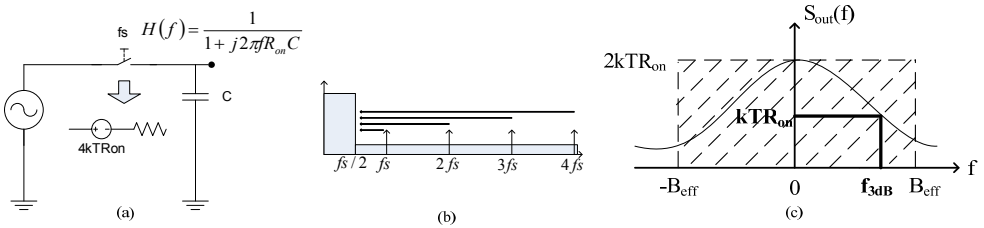


Figure 9. (a) Model of the S&H, (b) thermal noise folded in the band of interest and (c) effective noise bandwidth

R_{on} and C model a low-pass (LP) filter (Figure 9a) with a transfer function of $H(f) = 1/(1 + j2\pi f R_{on} C)$, whose 3-dB cutoff frequency is equal to $f_{3dB} = 1/(2\pi R_{on} C)$. Considering the one-sided representation of $S_{in}(f)$, the output PSD is [18]:

$$S_{out}(f) = S_{in}(f) |H(f)|^2 = 2kTR_{on} \frac{1}{1 + 4\pi^2 f^2 R_{on}^2 C^2} \quad (24)$$

The total noise power (with a two-sided representation) is:

$$P_{out} = \int_{-\infty}^{\infty} S_{out}(f) df = \frac{kT}{C} \quad (25)$$

For modeling purposes, the output noise can be considered to be a Gaussian thermal noise filtered by a brick-wall filter with a bandwidth equal to B_{eff} (i.e., noise bandwidth, see Figure 9c) [18]:

$$B_{eff} = \frac{1}{4R_{on}C} = \frac{\pi}{2} f_{3dB} \quad (26)$$

Therefore, the power noise can be rewritten as follows [18]:

$$P_{out} = \frac{kT}{C} = 2kTR_{on} \cdot (2B_{eff}) \quad (27)$$

On the other hand, the SNR in $[-B_{eff}, B_{eff}]$ is defined as [14]:

$$SNR = \frac{P_s}{N_i + (m-1)N_o} \quad (28)$$

where P_s is the signal PSD, and N_i and N_o are the in-band and the out-of-band noise PSDs, respectively. As $2B_{eff} = mf_s$ if $m=1$, the Nyquist theorem is met, and the SNR is not affected by the folded noise. On the other hand, if $m>1$, and assuming $N_i = N_o = N$:

$$SNR = \frac{P_s}{mN} = \frac{P_s}{N(2B_{eff} / f_s)} \quad (29)$$

The out-of-band folded noise, therefore, reduces the SNR by a factor $2B_{eff}/f_s$, with the entire wideband noise being folded inside the band of interest. From Expression (29), we can observe how the noise decreases around 3 dB when the sampling frequency is doubled.

It is convenient to select the largest sampling frequency among the set of possible sampling frequencies set by the digital signal processing block specifications. This is considered as the optimal sampling frequency (from equation $4f_c/m_{odd}$).

This effect was corroborated experimentally, as shown in Figure 10. This figure illustrates how the folded noise increases when a lower optimal sampling frequency is employed for an input signal centered at 1473 MHz.

A limitation of the data acquisition systems based on subsampling is the maximum sampling frequency, which is determined by the ADC's specifications and is around 400-500 MHz for commercial ADCs with large enough resolution.

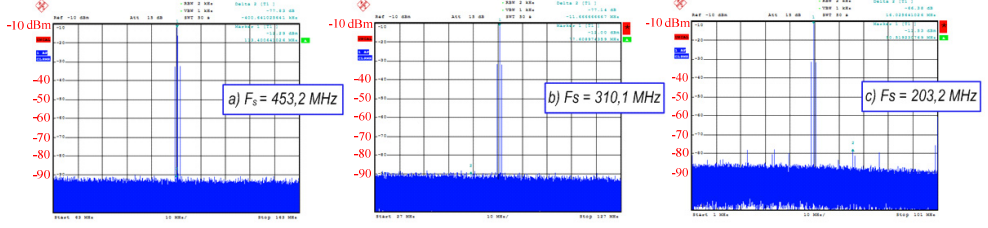


Figure 10. Thermal noise effect depending on the sampling frequency

In order to reduce the folded noise effect, a method to improve the resolution has been proposed [8], employing two consecutive subsampling stages. The use of two subsampling processes allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to the folded thermal noise [8].

Figure 11 shows two different alternatives for the implementation of a subsampling based receiver. Figure 11a illustrates the scheme for a unique subsampling process that was implemented in [7], while Figure 11b illustrates the scheme with two different clocks, as proposed by [8].

Assuming the noise of both S&Hs in Figure 11 are uncorrelated, the output PSD due to the white noise of the S&Hs in Figures 11a and 11b are, respectively [8]:

$$P_{N(a)} = \frac{2B_{eff1}}{f_s} N_1 + \frac{2B_{eff2}}{f_s} N_2; \quad P_{N(b)} = \frac{2B_{eff1}}{f_{s1}} N_1 + \frac{2B_{eff2}}{f_{s2}} N_2 \quad (30)$$

where N_1 and N_2 are the noise power introduced by $S\&H_1$ and $S\&H_2$, respectively, with B_{eff1} and B_{eff2} as their respective noise bandwidths.

We can observe how the second term only depends on N_2 in Figure 11b, because of the signal is filtered at IF in both cases, using a bandpass filter. In fact, an additional advantage of using a higher sampling frequency is that the requirements of the bandpass anti-aliasing filter are relaxed. This is illustrated in Figure 12 [20], where we can observe how the nearest unwanted replica is placed further away from the desired signal when the sampling frequency is increased.

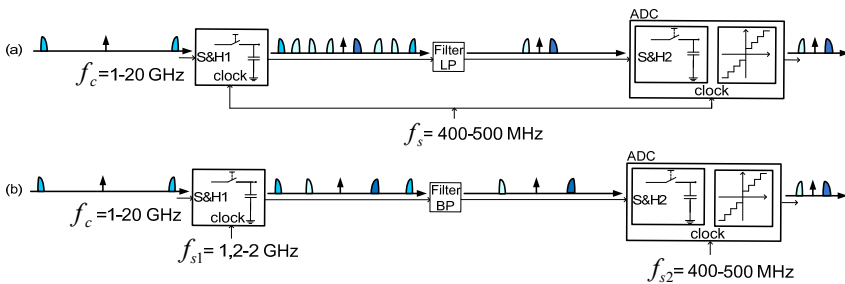


Figure 11. Clocking schemes for (a) a unique clock source and (b) two clock sources

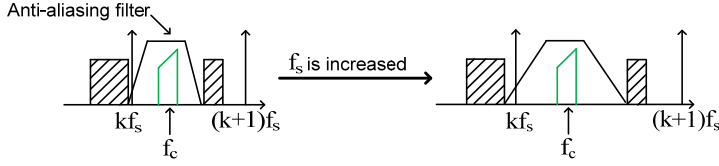


Figure 12. Bandpass anti-aliasing filtering requirements in subsampling

Thus, there is no folding of N_1 during the second sampling process. Therefore, the SNR improvement obtained with this sampling frequency plan is given by [8]:

$$\frac{SNR_{(b)}}{SNR_{(a)}} = \frac{P_s / N_{(b)}}{P_s / N_{(a)}} = \frac{B_{eff1}N_1 + B_{eff2}N_2}{\frac{f_s}{f_{s1}}B_{eff1}N_1 + \frac{f_s}{f_{s2}}B_{eff2}N_2} \quad (31)$$

The first S&H processes high-frequency signals, $B_{eff1} \gg B_{eff2}$. In addition, the noise PSDs of both S&Hs can be assumed to be of the same order of magnitude. Expression (31) can then be approximated by [8]:

$$\frac{SNR_{(b)}}{SNR_{(a)}} \approx \frac{1}{\frac{f_s}{f_{s1}} + \frac{f_s}{f_{s2}} \frac{B_{eff2}}{B_{eff1}}} \quad (32)$$

where f_{s1}/f_s is the most influential term in this improvement; the higher the ratio, the better the SNR improvement.

Some drawbacks of the proposed system are higher complexity and higher power consumption than a one-stage subsampling receiver.

4.4. Subsampling in multi-band and nonlinear systems

As previously mentioned, the two main drawbacks of systems based on subsampling are the jitter and thermal folded noise, making system implementation even harder for multi-band or nonlinear applications.

There is a challenge in utilizing subsampling techniques in nonlinear systems, because the replicas of the generated harmonics are folded in the band of interest and may overlap with the desired signals. This issue has been addressed and studied in [21], where a universal formula for bandpass sampling in nonlinear systems was developed. The extension of this approach for dual-band nonlinear systems was employed in [22].

For dual-band applications, the main problem of subsampling is the possible overlapping between the two desired signals in the IF frequency band. Although this drawback has been studied in [23], [22] extended this approach in designing the subsampling based receiver and optimized the system with respect to the typical non-idealities of subsampling receivers, i.e., jitter and folded noise.

4.4.1. Subsampling for dual-band and nonlinear systems

The effect of subsampling a dual-band signal in a third-order nonlinear system is illustrated in Figure 13 [22], showing the spectrum due to in-band intermodulation and cross modulation.

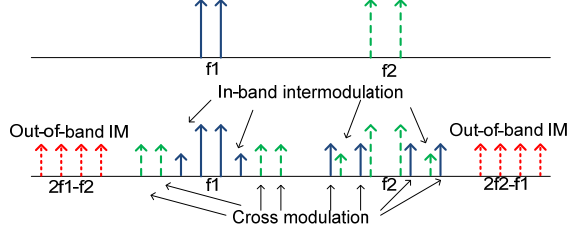


Figure 13. Power spectrum at the input (top) and the output (bottom) of a nonlinear system

On the other hand, when an input signal centered at f_i (Figure 14a) [21] drives a nonlinear system, the output signal of this system may produce multiple spectra centered at integer multiples of f_i (if_i in Figure 14a). Moreover, each spectrum may have different bandwidths. Therefore, if we let two spectra, i and j (with bandwidths B_i and B_j , respectively), be considered, where $j > i$ and $j - i = k$, and f_s is the sampling frequency, there must exist an integer such that [21]:

$$if_1 + n_k f_s \leq jf_1 < if_1 + (n_k + 1)f_s \quad (33)$$

where $n_k = \text{floor}((jf_1 - if_1)/f_s)$. On the other hand, an algorithm to find the range of valid subsampling frequencies for multi-band systems was presented in [23]. The subsampling frequency for a dual-band input spectrum, as shown in Figure 14b, must be chosen to ensure that the two signals do not overlap in the subsampled domain.

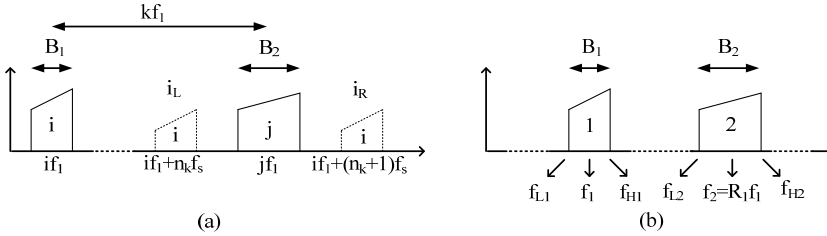


Figure 14. (a) Frequency locations in the sampled output spectrum and (b) spectrum of the dual-band RF signal at the input of the S&H with ratio $R_1 = f_2/f_1$

From the general equations obtained in [23] and considering a dual-band case, the maximum replica order of the lower band (n_1) meets the following equation:

$$n_1 = \left\lfloor \frac{f_{L1}}{f_s} \right\rfloor \leq \left\lfloor \frac{f_{L1}}{2((f_{U1} - f_{L1}) + (f_{U2} - f_{L2}))} \right\rfloor \quad (34)$$

where f_{L1} and f_{U1} are the low and high limits of the lower band, respectively, and f_{L2} and f_{U2} are the low and the high limits of the upper band, respectively. Knowing $f_2 = R_1 f_1$, replica orders of the upper band (n_2) meet the following constraint:

$$\lfloor R_1 n_1 \rfloor \leq n_2 \leq \lfloor R_1 n_1 + R_1 \rfloor \quad (35)$$

Therefore, the eight possible ranges for dual-band applications are listed in the Table 1 [23]:

Case	Range of valid f_s	Case	Range of valid f_s
1	$\frac{f_{U2}}{n_2 + 1/2} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1}, \frac{f_{L2} - f_{U1}}{n_2 - n_1}\right)$	5	$\max\left(\frac{f_{U1}}{n_1 + 1}, \frac{f_{U2}}{n_2 + 1/2}\right) \leq f_s \leq \frac{f_{L1} + f_{L2}}{n_1 + n_2 + 1}$
2	$\frac{f_{U2}}{n_2 + 1} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1 + 1/2}, \frac{f_{L2} - f_{U1}}{n_2 - n_1}\right)$	6	$\max\left(\frac{f_{U1}}{n_1 + 1/2}, \frac{f_{U2}}{n_2 + 1}\right) \leq f_s \leq \frac{f_{L1} + f_{L2}}{n_1 + n_2 + 1}$
3	$\frac{f_{U1} + f_{U2}}{n_1 + n_2 + 1} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1}, \frac{f_{L2}}{n_2 + 1/2}\right)$	7	$\max\left(\frac{f_{U1}}{n_1 + 1}, \frac{f_{U2} - f_{L1}}{n_2 - n_1}\right) \leq f_s \leq \frac{f_{L2}}{n_2 + 1/2}$
4	$\frac{f_{U1} + f_{U2}}{n_1 + n_2 + 1} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1 + 1/2}, \frac{f_{L2}}{n_2}\right)$	8	$\max\left(\frac{f_{U1}}{n_1 + 1/2}, \frac{f_{U2} - f_{L1}}{n_2 - n_1}\right) \leq f_s \leq \frac{f_{L2}}{n_2}$

Table 1. The boundary constraints for the dual band case

Thus, the final sampling ranges are given by the following expression:

$$F = F_{db} \cap F_{imd} \cap F_{cmd} \cap F_{hmd} \quad (36)$$

where F is the intersection of all the valid ranges calculated from Expressions (33) and (34), F_{db} , F_{imd} , F_{cmd} and F_{hmd} are the valid sampling frequency sets for the fundamental signals, intermodulation, cross modulation and harmonic distortion, respectively.

4.4.2. Optimization of multi-standard receiver architecture

In order to optimize the noise performance of a dual-band receiver in a nonlinear scenario, a particular case has been researched [22], where seven input frequencies were selected to study the selective combinations for different dual-band applications. These chosen standards were WCDMA (Wideband Code Division Multiple Access) (V) at 880 MHz, GSM-DCS (Global System for Mobile Communications – Digital Cellular System) at 1.82 GHz, WCDMA (I) at 2.12 GHz, Bluetooth at 2.4 GHz, WiMAX (Worldwide Interoperability for Microwave Access) at 3.5 and 5.8 GHz, and IEEE 802.11a at 5.2 GHz.

Since the main focus is the coverage of a maximum number of standards, it is mandatory that an S&H be placed before the ADC, in order to have enough analog bandwidth. The S&H from Inphi with part number 1821TH has been selected as the reference for this work,

due to its high input analog bandwidth (up to 18 GHz), minimum aperture jitter (50 fs) and a maximum clock frequency equal to 2 GHz.

The first study scenario (Case 1) is based on a high-resolution ADC with a high sampling frequency, in order to reduce the folded noise effect. With this focus in mind, the selected ADC was a 12-bit ADS5400 from Texas Instruments with a maximum clock frequency of 1 GHz. Using a sampling frequency of almost 1 GHz, it is possible to cover all the dual-band applications, as illustrated in Figure 15a (Case 1) [22], where the meaning of X-axis is illustrated in Table 2 [22]. Using a typical SNR of the ADC of 58 dB as the reference, the theoretical SNR for each dual-band application is calculated from Expressions (16) and (29).

Another option is the use of a higher resolution ADC, such the 14-bit ADS5474 from Texas Instruments (Case 2 in Figure 15a). This device was selected because its maximum sampling frequency is 400 MHz; therefore, the folded noise is only around 4 dB higher than Case 1.

X-Axis	1	2	3	4	5	6
Input Frequency (GHz)	0.88-1.82	0.88-2.12	0.88-2.4	0.88-3.5	0.88-5.2	0.88-5.8
X-Axis	7	8	9	10	11	12
Input Frequency (GHz)	1.82-2.12	1.82-2.4	0.88-3.5	1.82-5.2	1.82-5.8	2.12-2.4

Table 2. Correspondence between dual band applications and axis X

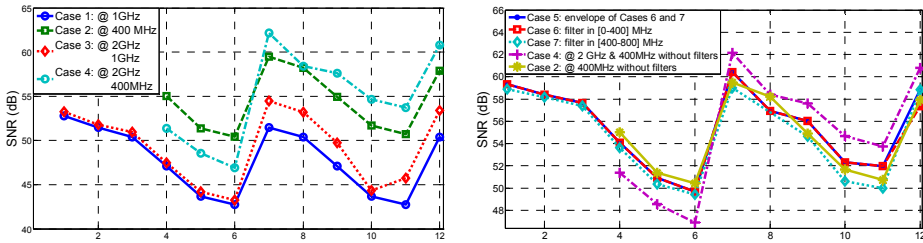


Figure 15. Expected SNR (a) for single and multiple clock architectures and (b) for different architectures based on bandpass filters

In order to improve the SNR without losing flexibility, a two-step subsampling approach is proposed, where the sampling frequency of the S&H is set at around 2 GHz and the sampling frequency of ADC at around 1 GHz (Case 3 in Figure 15a). Although this architecture improves the SNR by approximately 3 dB from Expression (29) in respect to Case 1, it is necessary to implement a second subsampling process; therefore, a new folded noise effect is added.

The last option is the use of a multiple ADC architecture employing the ADS5474 (Case 4 in Figure 15a) and a first sampling frequency of around 2 GHz. Theoretically, the SNR is improved by around 4 dB, in respect to Case 3. In this case, due to the second subsampling process, folded noise effects must also be added.

For the rest of combinations of frequencies, the curves present the same tendency, so that it is possible to cover all the scenarios (Cases 1-4). However, since Cases 2 and 4 provide the best results for the SNR, the next step is the coverage of all the dual-band applications for these cases. The proposed solution is the use of a bank of bandpass filters between the S&H and the ADC. This solution is applied to Case 4, because it has a more flexible architecture, with a higher number of available valid ranges. Using this solution, some harmonics are removed, and the flexibility of the receiver is increased. The solution is based on two bandpass filters with ranges of 0 – 400 MHz and 400 – 800 MHz. The maximum sampling frequency is selected, in order to have both fundamental replicas in each range. The selected filter corresponds to the higher of these two frequencies (Case 5 in Figure 15b [22]).

Another solution is a unique bandpass filter for all the applications (Cases 6 and 7 in Figure 15b). In these cases, it is possible to cover almost all the standards with only one of these filters, without considerably reducing the resolution. In order to maximize the flexibility and the SNR, the optimal architecture is like the one illustrated in Figure 16 [22]. For a more concrete application or more relaxed SNR specifications, a single bandpass filter can be used in order to reduce the complexity of the system.

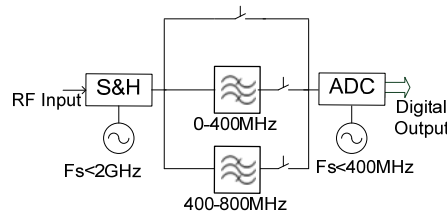


Figure 16. Optimized architecture based on multiple clocks and bandpass filters

4.4.3. Subsampling applications for multi-band and nonlinear systems

A subsampling receiver for multi-band applications is more advantageous than a wideband receiver, because it limits the minimum sampling rate to twice the information bandwidth, instead of twice the Nyquist frequency [24]. The reduced sampling frequency allows lower speed commercial ADCs to be used. Two applications are presented: spectrum sensing for cognitive radio applications, and selective multi-band down-conversion for amplifier linearization.

4.4.3.1. Spectrum sensing in cognitive radios

Wireless spectra are regulated by government bodies and are assigned a fixed frequency slot for transmission. Studies reveal that licensed spectra are highly underutilized and suggest a more efficient and flexible way for spectrum management [25]. Cognitive radio systems aim to reuse these underutilized spectra through dynamic spectrum allocation, which must integrate a wideband / multi-band receiver for scanning these spectra.

A subsampling receiver may allow the cognitive radio to sense different bands to check and see if they are in use. A bank of bandpass filters precedes the input of the receiver to control

any interfering signals that may alias over the signal when subsampling. Figure 17a shows a block diagram of the subsampling receiver architecture proposed in [15], along with its corresponding validation setup (Figure 17b).

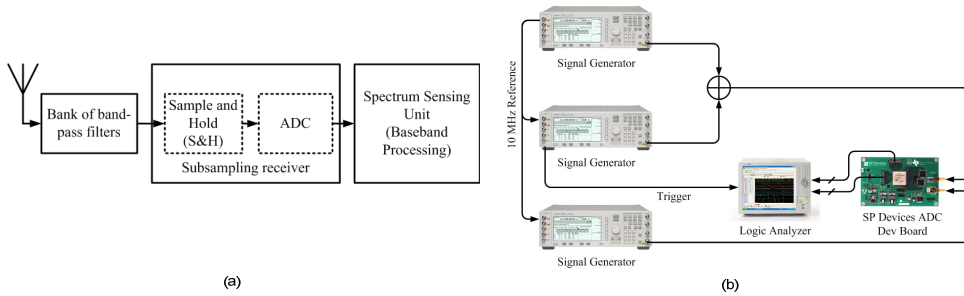


Figure 17. (a) Subsampling based receiver for spectrum sensing in cognitive radio systems and (b) measurement setup for validating spectrum sensing concept using subsampling receiver

As an example for spectrum sensing using a subsampling receiver, two RF bands are selected: the official digital video broadcasting (DVB) band at 698 – 752 MHz, and an unlicensed band at 902 – 928 MHz. With these two bands and using the formula described in the previous section, a subsampling frequency of 255 MHz is selected.

Figure 17b [15] shows the measurement setup used for spectrum sensing. Two signal generators are used to simulate the two RF bands, and the bands are then combined using a power combiner and passed into the receiver. A SP Devices development board and two Texas Instruments' ADS5474 ADCs operating in a time-interleaved manner are used as the subsampling device. A logic analyzer is used to capture the digital data streaming from the ADC board, while another signal generator provides a clock source for the ADC.

A three-channel signal is sent in the DVB band, while a 2-channel signal is sent in the unlicensed band. Different power levels are configured for each channel to simulate different received signals. Figure 18a shows the spectra of these two bands in the RF domain. Figure 18b [15] shows the two bands subsampled using a frequency of 255 MHz. Since the ADCs are operating in a time-interleaving fashion, the differences between each ADC may cause gain mismatches and timing skews [26]. These errors result in attenuated replicas of signals that are being subsampled, specifically at $f_s/2 - f_m$, where f_m is the subsampled signal frequency.

Figure 19 [15] shows the input signals overlaid with their subsampled output after digital demodulation. With the subsampling receiver, the captured signal has approximately a 50 dB signal-to-noise floor.

The technique may be extended to multiple bands, where changing the subsampling clock may allow different RF bands to be demodulated concurrently. In [15], the cognitive radio senses up to 14 bands, sensing two bands at any given time.

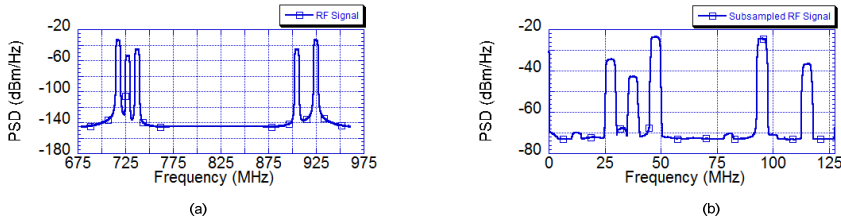


Figure 18. Spectra of (a) the input RF signal to the receiver and (b) the subsampled RF signal for bands (698 – 752 MHz, 902 – 928 MHz) using a subsampling frequency of 255 MHz.

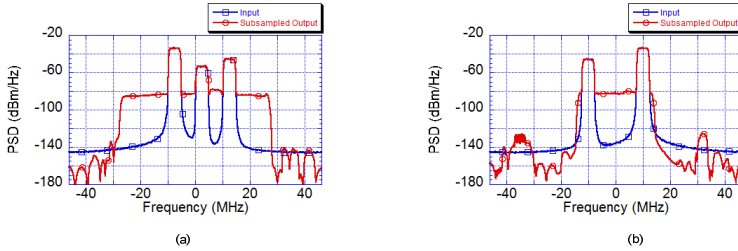


Figure 19. Spectra of the input and filtered output baseband signals for (a) the 698 – 752 MHz band and (b) the 902 – 928 MHz band

4.4.3.2. Subsampling feedback loop for concurrent dual-band power amplifier linearization

The power amplification unit is typically the most inefficient component in wireless transmitters. This is caused by the inverse relationship that exists between efficiency and signal quality based on the signal power being transmitted [27]. At low input power, efficiency is low, and the power amplifier (PA) exhibits linear behavior, which results in good signal quality at the amplifier output. However, operating the amplifier at its highest efficiency state close to the maximum output power causes the gain characteristics to become compressed, and the input-output relationship becomes nonlinear. The nonlinear behavior reduces the in-band signal quality and causes out-of-band spectral regrowth. Nonlinearity is further complicated in a dual-band operation, where the device produces many intermodulation and cross-modulation signals. This inverse relationship causes difficulties for the wireless operator, and typically a linear operation mode is used, so that signal quality is good and that spectral regrowth is minimal and does not cause interference in other channels.

Digital predistortion allows for the operation of signal in the high-efficiency region, while reducing spectral regrowth and improving signal quality [28]. This is performed by analyzing the input and output signals of the PA and generating an inverse behavioral model (predistorter) of the amplifier. The cascade of both the digital predistorter and the PA results in a linear gain at the output for the full power range.

A dual-band PA operating at 880 MHz and 1978 MHz is used to test the subsampling feedback loop for concurrent dual-band linearization [16]. Two communication signals with

5 MHz bandwidths are sent at the center of these bands. The PA is predicted to have a 5th-order nonlinearity; and, all the harmonics, intermodulation and cross-modulation products up to 4 GHz are represented. In addition, a 25 MHz guard band is placed around each band frequency to account for the spectral regrowth that happens during the initial analysis stage.

Since the baseband communication signals are known, only the output signals at each band are needed. The harmonic, cross-modulation and intermodulation signals may be ignored; their only restriction is to not lie inside of the guard band of the signals. The subsampling algorithm outlined in the previous section calculated the minimal subsampling frequency of between 619.7 MHz and 620.1 MHz. Figure 20a shows a simulation of the RF spectra of all the components up to 4 GHz, while Figure 20b shows the subsampled components using a frequency of 619.8 MHz [16].

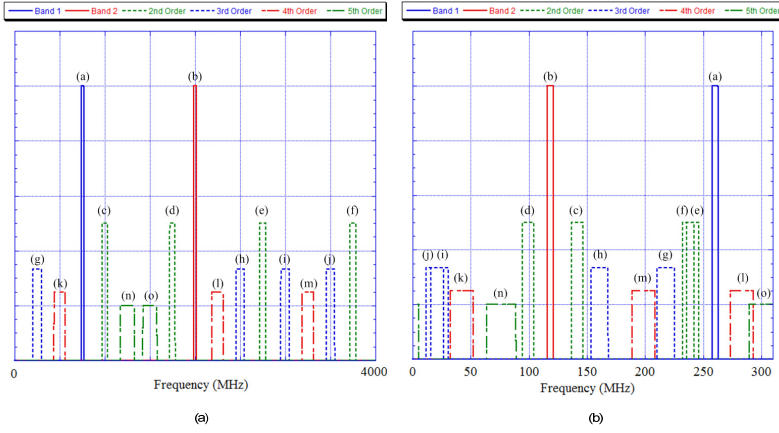


Figure 20. (a) Predicted RF fundamental and harmonics up to 4 GHz and (b) subsampled result using a sampling frequency of 619.8 MHz

The same setup described in Figure 17b is used to generate the dual-band signal and capture the RF output. Figure 21a shows the RF spectra at the output of the PA [16]. Compared to Figure 20a, there is an extra term, p , which is a 7th-order intermodulation product at 436 MHz. The rejection of the i and j terms are due to the design of the PA output matching network. As explained previously, the time-interleaved ADC architecture causes attenuated signal replicas, a_i and b_i . Figure 21b [16] shows the normalized spectra of the subsampled RF PA output. There is attenuation from the upper band signal caused by the limitation of the ADC's bandwidth of 1.4 GHz. The captured time domain signal may be digitally demodulated, filtered and resampled to retrieve the amplifier output of the two bands; and, further post-processing can determine the digital predistortion model.

5. Implemented systems for multi-standard applications

If a multi-standard receiver is implemented by stacking different receivers for different standards into a single receiver, the area and power consumptions are extremely high.

Therefore, a properly designed multi-standard receiver must share hardware resources and use tunable and programmable devices, in order to reduce the area and power consumption, which is a very important approach for battery powered devices. Otherwise, the main constraint for multi-standard applications, such as instrumentation or validation, is the capability of covering the maximum possible number of standards.

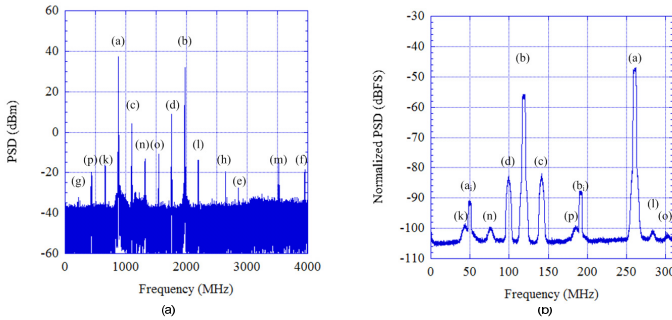


Figure 21. (a) RF spectra at the output of the PA and (b) normalized spectra of the captured subsampled signal using an ADC operating at 619.8 MHz

Multi-standard receivers can implement a narrowband or wideband strategy. A narrowband strategy is implemented by receivers that are designed for some specific standards, while a wideband strategy is implemented by receivers that cover a higher number of wireless standards. Therefore, narrowband receivers may provide a finer optimization for specific standards, and wideband receivers may be considered universal receivers and are used for more general applications.

Multi-standard receivers can be classified by their architectures, i.e., systems based on mixing or subsampling techniques. Although subsampling techniques have some problems, such as the folded thermal noise effect or aliasing in multi-band scenarios, they are very convenient for SDR applications, placing the ADC stage as close the antenna as possible.

5.1. Multi-standard receiver based on subsampling

A data acquisition module for high-performance low-cost multi-standard test equipment is presented in [7]. This work provides high resolution over a large bandwidth with only a low-jitter wideband S&H and an IF ADC by means of subsampling. Using commercial devices on a multilayer printed circuit board (PCB), experimental results show a resolution of more than 8 bits for a 20 MHz signal bandwidth with a center frequency up to 4 GHz, enough to cover the requirements of test systems for most of the current wireless communication standards.

From the theoretical analysis and a set of simulations, the specifications of the main building blocks of the module, i.e., the S&H and the ADC, can be derived. In order to obtain a total resolution larger than 8 bits for a maximum input frequency of 4 GHz and a signal bandwidth of 20 MHz, the main specification for the S&H is an aperture jitter lower than 100

fs. For the ADC, a sampling frequency larger than 400 MHz is selected, in order to reduce the folded noise effect.

After a study of the available commercial ADCs, an external S&H is selected, since the bandwidth of presently available internal S&Hs is limited to approximately 3 GHz for an equivalent number of bits (ENOB) of less than 8 bits. The selected ADC is the E2V AT84AS001. The Inphi 1821 TH is chosen as the S&H, because of its low aperture jitter (50 fs). For the target application, other relevant features of this S&H are its large bandwidth (18 GHz) and its large frequency range (0-6 GHz) for 10-bit linearity. In addition, it is able to sample at an IF of 500 MS/s, which is the maximum sampling frequency for the selected ADC that guarantees a spurious-free dynamic range (SFDR) larger than 60 dBc.

These devices are the main components of the proposed data acquisition system for which a multilayer PCB prototype was designed and fabricated (Figure 22a [7]). Other components, such as bias tees and low-pass passive filters (Minicircuits LFCN-160), are included between the S&H and the ADC. This design uses a Class 7 board with DE104i FR4 dielectric, six metal layers and microstrip lines adapted to 50 Ω. The rules and expressions employed to adapt the components (designing the dimensions of traces and layers) were obtained from [29].

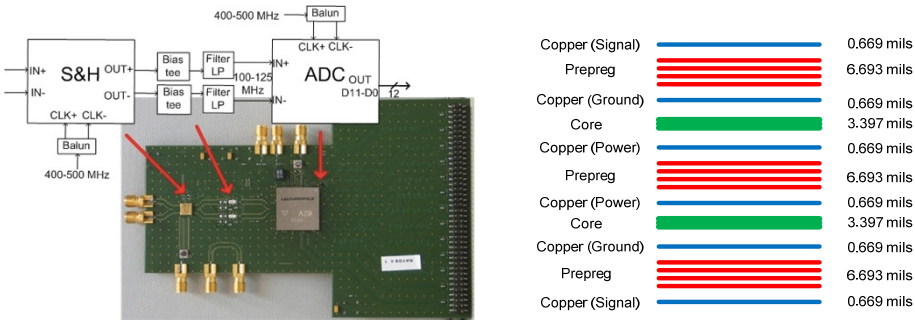


Figure 22. (a) Block diagram and designed PCB prototype and (b) the stack-up implemented in [6]

Employing the external metal layers (1 and 6) for signals, the adjacent metal layers for grounding (2 and 5) and the most internal layers (3 and 4) for power supplies, the resultant stack-up is as shown in Figure 22b.

The circuit is carefully laid out, in order to minimize the jitter effect. The distances between signal tracks, pads and metal layers are carefully chosen, in order to reduce crosstalk and inter-symbol interference, which cause jitter. Other rules followed to reduce jitter are a correct decoupling from the power lines and the so-called picket fences technique, which consists of placing closely spaced vertical interception accesses (vias) between different grounding planes. A distance between vias equal to $1/20$ wavelength is selected.

Finally, this board achieves (for a 20 MHz signal bandwidth) an experimental ENOB of 8.5 bits for a programmable carrier frequency ranging from 0 up to 3.3 GHz. An example of the output spectrum is illustrated in Figure 23a.

In order to reduce the folded thermal noise effect, a new approach using two consecutive subsampling stages was implemented in [8]. The use of two subsampling processes allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to the folded thermal noise.

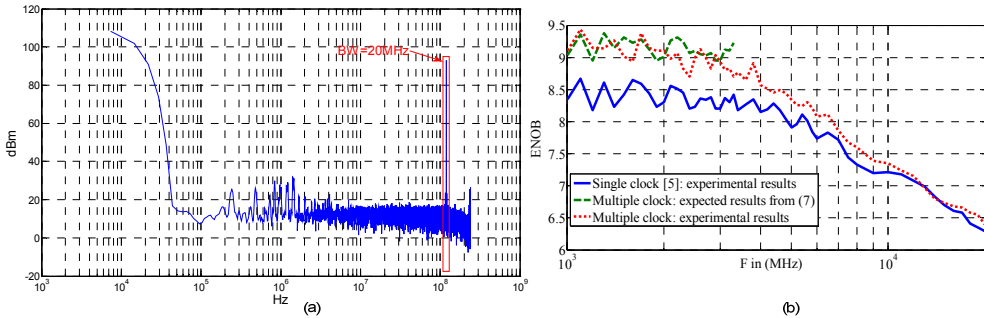


Figure 23. (a) Output spectrum for an input signal at 3 GHz sampled at 480.2 MHz and (b) ENOB versus carrier frequency (20 MHz signal band)

In this work, a sampling frequency of between 1.2 GHz and 2 GHz for the first S&H is selected, obtaining a band-limited signal at the output. After filtering, the resulting signal is subsampled again by a second S&H at 400 – 500 MHz (Figure 11b). However, some drawbacks of the proposed system are higher complexity and higher power consumption than the one-stage subsampling data acquisition system.

Figure 23b [8] shows the ENOB as a function of the carrier frequency up to 20 GHz, for a signal bandwidth equal to 20 MHz. The solid line shows previous results obtained in [7]. The dashed line shows the expected ENOB calculated with Expression (32), which is met, while jitter is not the dominant effect. Finally, the dotted line shows the experimental results obtained in [8].

These experimental results show how the proposed system reduces the effect of the folded noise, increasing the ENOB by 0.5-1 bits in the band of interest. Therefore, it provides an ENOB larger than 9 bits up to 2.9 GHz, 8 bits up to 6.5 GHz, 7 bits up to 12 GHz, and 6.4 bits up to 20 GHz. The results for linearity and power consumption are similar to those obtained in the previous work [7].

5.2. Comparison with other implemented multi-standards receivers

The receiver in [7,8], which is described in Section 5.1 may be an approach to a universal receiver for SDR applications. Other works have also studied multi-standard receivers. However, some of these works were based on mixing techniques, thereby losing part of the flexibility and simplicity provided by subsampling based systems. On the other hand, there were also multi-standard receivers that, although they were based on subsampling, were optimized for a given number of wireless standards, without covering all the applications.

Therefore, there are two main research fields for multi-standard receivers: digitalization techniques (i.e., mixing or subsampling based systems), and band strategies (i.e., wideband or narrowband strategy).

Examples in both research directions are present in the literature. There are examples of works that employ wideband strategies [1,5]. In [5], a receiver front-end is presented for multi-standard wireless applications, which is composed of a wideband amplifier, source followers, passive mixers and transimpedance amplifiers, with an analog bandwidth of up to 3.5 GHz. In [1], a wideband, multi-standard receiver, consisting of a wideband low-noise amplifier (LNA), a highly linear down-converter and a programmable digital baseband that performs decimation and filtering, is proposed. This work can be considered as a universal receiver, covering input frequencies between 0.8 and 6 GHz and based on mixing techniques. Although [1] is a more complex solution than [8], this work has a larger tuning range and other benefits, such as high linearity and low power consumption, because of its implementation in an integrated circuit (IC). Since the receivers of [1,5,7,8] offer wideband solutions, the RF front-end must meet the requirements for each standard; however, the solutions are not optimal for any standard.

Using a narrowband strategy, an alternative multi-standard receiver solution is proposed by [2], separating into two different RF channels, one for 2.4 and 5 GHz wireless local area networks (WLANs) and the other for Global System for Mobile Communications (GSMs). The different channels shared a common programmable baseband. This solution was highly efficient, because every path was optimized to a specific standard. On the other hand, in addition to the limitation of the number of standards, the main drawback of this work was area consumption, because the high selectivity was achieved by the utilization of many inductors.

An example of a solution based on narrowband strategies is shown in Figure 24a [3]. In this receiver, dedicated Bluetooth and Global Positioning System (GPS) links allow connectivity when making a phone call and/or sending or receiving data through a WLAN. The WLAN path connects to IEEE802.11a/b/g/n routers, while the cellular-dedicated channel can switch from one of the GSM bands to UMTS (Universal Mobile Telecommunications System) / WCDMA. Moreover, the selection is provided by off-chip surface acoustic wave (SAW) filters, which relax the linearity requirements.

Other works provided a high level of hardware sharing, where the different specific standards employed a common acquisition and digitalization stages. In [4], a solution for Bluetooth, GSM, UMTS and WLAN was presented, where the last three standards share the same circuitry after the filter bank (Figure 24b), allowing for reuse of some building blocks in the receiver architecture. This maximization of hardware sharing meant minimal area consumption, which was possible because all the considered standards (except Bluetooth) did not need to be covered at the same time, i.e., when an application was active, the others could be switched off, in order to save power.

Data acquisition systems for different communications standards use subsampling techniques, in order to process high-frequency signals with only a few components. In [6], a

subsampling receiver was proposed for three different standards (GSM, UMTS and IEEE 802.11g), which validated these topologies at a simulation level, so that they could be applied to multi-standard radio design. An additional goal of this work was the design of RF and IF filters for the different standards, in order to avoid the aliasing caused by the subsampling process. Moreover, the constraints for the IF filter, the band of which is fixed, was relaxed due to the subsampling process in the first stage.

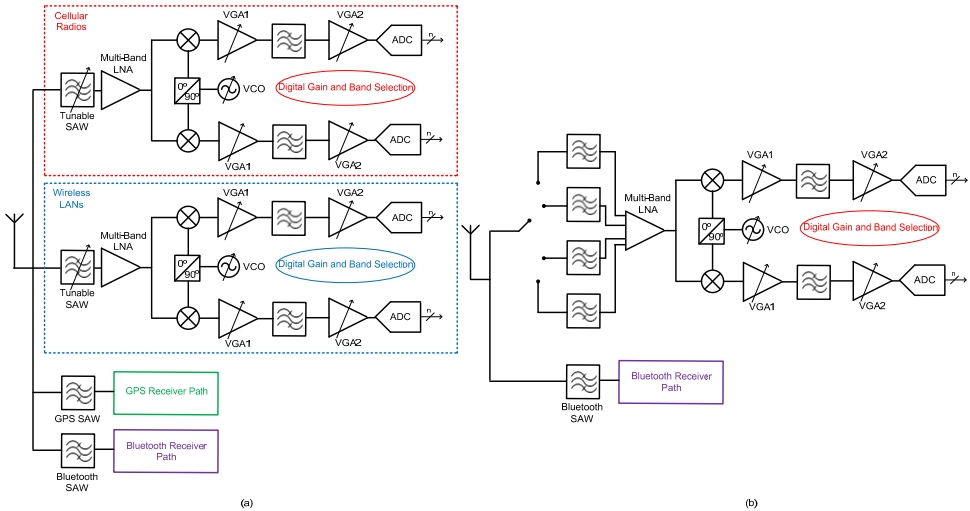


Figure 24. Multi-standard receiver architectures proposed in (a) [3] and (b) [4]

	Standard	GSM 1800	UMTS (I)	Blue-tooth	802.11b/g	802.11a
Standard requirements	Carrier Frequency (MHz)	1805.2-1879.8	2110-2170	2400	2400	5000
	Signal Bandwidth (MHz)	0.2	5	1	20	20
	ENOB (bits)	9	6	11	8	9
	NF (dB)	9.3	4.6	10.7	6.5	18.2
Experimental results of previously published acquisition systems	ENOB [7] (bits)	11.76	9.56	10.36	8.2	7.41
	NF [7] (dB)	6.1	6.5	8.3	8.3	13.1
	NF [2] (dB)	5.2	5.6		5.8	
	NF [5] (dB)	5.8	6	6.5	6.5	
	NF [6] (dB)		7.5		7.2	
	Noise PSD [31] (dBm/Hz)				-131	

	Standard	GSM 1800	UMTS (I)	Blue-tooth	802.11b/g	802.11a
Experimental results of [8]	ENOB (bits)	12.47	9.97	10.86	8.7	8.34
	NF (dB)	3.6	4.4	6.2	6.2	9.3
	Noise PSD (dBm/Hz)	-129.7	-128.8	-126.9	-126.9	-123.8

Table 3. Standard specifications and results

In other published works, the receivers based on subsampling were implemented experimentally for only fixed bands. Thus, low-noise subsampling implementations for the 2.1 GHz band [30] and for 2.4 GHz (IEEE 802.11a/g WLAN standards) [31] have been proposed. In [30], an IC receiver designed in 0.18 μm CMOS (complementary metal oxide semiconductor) was presented, the main goal of which was a tunable LC (inductor, capacitor) filter implementation. In [31], a 0.18 μm CMOS receiver represented the most complete subsampling receiver reference, due to the optimization performed for parameters, such as thermal noise level, jitter-induced noise and nonlinearity. Finally, there were also receivers based on subsampling for ultra wideband (UWB) applications, such the one in [32], which operates in the 3.1 – 10.6 GHz band with low power consumption.

Table 3 [8] shows the specifications for most of common wireless communication standards [2] and the results obtained in some of these previously published works on noise performance. These results are compared with those obtained in [8], in order to observe the benefits of implementation of a multiple clock technique for multi-standard receivers based on subsampling. It can be seen that, when employing the data acquisition system designed in [8], only the ENOB specifications for the IEEE 802.11a standard are not achieved, although they are very close. It should also be noted that some specifications, such the noise figure (NF) for UMTS (I) and IEEE 802.11b/g or the resolution for Bluetooth, are not achieved without the improvement proposed in [8], i.e., when a unique clock source is used [7]. Compared with the other published work, similar results for NF and noise PSD can be observed with respect to [8], showing a larger influence of the jitter (i.e., reducing the resolution with the input frequency) in the work presented in [8].

6. Conclusions

In this chapter, a brief review of sampling theory and the advantages of subsampling techniques in the context of wireless communication transceivers have been presented. In particular, the usefulness and potential of subsampling techniques in the design of a simple and flexible universal receiver are discussed. A data acquisition module for testing wireless receivers based on subsampling has been presented, which covers most present wireless communication standards requirements with only one single board. The main benefits have been presented, and a novel method based on multiple clocking techniques to reduce the folded noise effect has been proposed, obtaining an analytical expression for the

improvement factor in the SNR with respect to a single clock solution. The presented board shows an experimental ENOB larger than 8 bits up to 4 GHz for a 20 MHz signal bandwidth; and, the selected frequency plan with two successive subsampling processes shows the ENOB improved by approximately 1 bit. Measurement results show that the design covers the most important wireless standards (i.e., GPS, GSM, GPRS, UMTS, Bluetooth, Wi-Fi, WiMAX), in terms of tuning frequency, linearity and noise. Another characteristic of the implemented module is its simplicity, with only a few components on a printed circuit board. These results show that, for testing purposes, the subsampling based receiver is a viable alternative to other typical frequency mixing based receiver architectures, with enhanced reconfigurability and programmability.

Moreover, the subsampling concept has been extended to multi-band and nonlinear systems, where there is an additional problem with the harmonics and different channels that may be folded in the band of interest. In this chapter, the challenges and issues on finding the valid subsampling frequencies in multi-band and nonlinear systems are discussed. For this scenario, the noise performance of a dual-band multi-standard receiver has been optimized, proposing different architectures based on multiple clocking techniques. Finally, two different applications (spectrum sensing in cognitive radios and a subsampling feedback loop for concurrent dual-band power amplifier linearization) are proposed and characterized experimentally, in order to demonstrate the functionality and capability of subsampling techniques for multi-band and nonlinear environments, reducing the cost and the complexity of the receiver architectures.

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Acknowledgement

This work was supported in part by the Andalusian Regional Government (under the program entitled “Programa de Incentivos para el Fomento de la Innovación y el Desarrollo Empresarial de Andalucía”) and the Andalusian Technological Corporation (CTA) and in part by the Andalusian Regional Government, under projects MUPHY and TIC-6323-2011, respectively. The authors also acknowledge Alberta Innovates - Technology Futures (AITF), the Natural Sciences and Engineering Research Council of Canada (NSERC), and the Canada Research Chairs (CRC) Program for their financial support.

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