Integrated Silicon Microwave and Millimeter-wave Passive Components and Functions

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1. Introduction

The continuous scaling down of device size makes high-speed circuits achievable as a result of the inverse relationship between gate length and transition time. In the same time, passive components like capacitors, inductors, antennas or interconnect transmission lines become a limiting factor to the global integration particularly for functions like filters. For example Wireless communications have increased in a spectacular way over recent years due to the quest of complete transceiver integration (RF/digital/analog blocks) on a same chip in order to meet cost effective. In this context, the reduction of off-chip components is necessary. This trend has gradually led to a greater integration of passive components in the back end of line (BEOL) of silicon technologies. Integrated in BEOL (Figure 1) metallization of CMOS or BiCMOS technologies, these devices have to meet requirements in terms of high RF performances, low area and compatibility with silicon substrate such as bulk silicon or SOI (Silicon On Insulator).

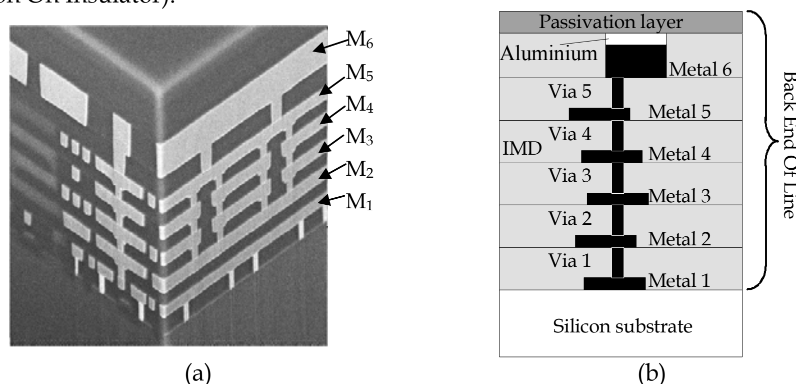

Fig. 1. BEOL with 6 interconnect levels: (a) 3D view, (b) schematic view (IMD=Inter-Metallization Dielectric)

The BEOL is at the origin dedicated to the interconnections of the digital circuits and then the analog circuits. In this context, it was advantageous to use interconnect levels to design passive components.
The difficulty of realizing integrated passive components having strong performance and weak surface in the BEOL, resides in the technological change of the levels of interconnections tightening with a reduction increasingly more important of metals thicknesses and dependent on the increasing integration of the active devices. To overcome this limitation, the use of one or two thick metal layers, which thickness can reach 3 µm, is now implemented in different technologies.
Another important point for BEOL, is the damascene process introduced with copper metallization. Copper is for most of passive components the best conductive material mainly because of its low conductivity; but damascene architecture imposes a copper density usually between 20 % and 80 % due to chemical and mechanical polishing (CMP). To comply with this rule, it is necessary to include small cube of copper typically of 1 μm^3 and called dummies. From an electromagnetic point of view, particularly in millimeter range, dummies can have a strong impact on passive components as function of the design.

2. Capacitors and inductors for RF applications

The recent progress of CMOS technologies makes possible to consider today, an increasingly thorough integration of RF and millimeter waves analog circuits. These circuits require at the same time powerful passive components, and a weak occupied surface. These components are indissociable of the functions like the amplifiers, the mixers, the filters…
Today one of the problems, to answer the need for massive integration and low cost on silicon of a complete electronic system, lies in the number and the performance of the passive L and C components compared to the number of transistors, which these functions require. From microelectronics point of view, they are studied since a long time (Burghartz et al., 1997) taking into account technological evolution and the frequency of operation.

2.1 Capacitors

A capacitor is constituted of a dielectric surrounded by two metal electrodes. Classically the value of the capacitor can be obtained by the well-known relation: $C=\varepsilon S/t$, where ε is the permittivity of the dielectric material, S is the surface of the electrodes and t is the thickness of the dielectric material.
The main parameters that are used to characterize the quality of a capacitor are the quality factor, the resonant frequency and the capacity per unit surface. This last parameter is of great importance for silicon integration as the cost of an integrated circuit is directly dependent on its surface.
Taking into account the basic equation of the capacitor, there are three possibilities to change the capacitor value and particularly to increase its value when necessary. The first one is to change the surface; this can be done easily but will increase the cost of the circuit for big values and consequently large area. The second possibility is to reduce the thickness of the dielectric, but this is more difficult if the thickness reaches few nanometers. Moreover, reducing the thickness can lead to a degradation of the performance of dielectric material and the break down voltage of the material is strongly dependent on its thickness.

Another possibility to increase capacitor value is to use various dielectric materials as those of Table 1 (Mondon & Blonkowskic, 2003 ; Allers et al., 2003; Berthelot et al., 2006; Defay et al., 2006). The last column of Table 1 gives an indication about the capacitor density, but the proposed typical values are dependent of the possible thickness of the dielectric used and the type of capacitor. An attention must be paid to the possible use in high frequency and particularly losses, because some of these materials are not well known in mm range. A last possibility is to occupy the whole thickness of the BEOL. For that purpose, different structures of capacitors are studied as presented in the next section.

Dielectric	Permittivity	Breakdown field (V/nm)	Typical density value (fF/µm²)
SiO_2	4.2	0.1	1
Si_3N_4	7	0.07	2
Al_2O_3	9	0.08	3.5
HfO_2	18	0.06	14
Ta_2O_5	25	0.05	5
ZrO_2	45	0.04	35
$SrTiO_3$	150	0.01	10

Table 1. Main dielectrics used to realize capacitors and typical density value of planar MIM capacitors.

When a capacitor will be chosen an important parameter is its value. The more its value is bigger, the more the resonance frequency presents a low value. In an other words, it is quasi impossible to obtain large capacitor values working in frequency above few GHz. This is due to losses and to inductive behavior of metallic part of the capacitor which limit its performance. Thus for mm-wave application, low capacitor values are required and can be obtained with one of the most used shape described in the next section.

2.1.1 Different capacitors type

A. MIM capacitors

(a) (b)

Fig. 2. Schematic view of a MIM capacitor: (a) cross-section, (b) 3D view

The Metal Insulator Metal (MIM) capacitor is a planar capacitor as shown in Figure 2. The advantage of this capacitor is its simplicity to design and to realize, but it requires an intermediate metal level Mnbis as shown in Figure 2(a). To respect metal density rules different kind of electrodes can be used (Figure 2(b)). This will reduce the capacitance per unit area. To increase the capacitor value, it is possible to design one capacitor in the last level and another in the next to last level (Chen et al., 2002) of the BEOL.

B. Finger capacitors

Finger capacitors are derived from MIM capacitor and use all metallic levels of the BEOL. The main advantage is to increase the capacitance density. This kind of structure allows to increase capacitance density of about 30% as compared to MIM capacitor (Subramaniam et al., 2005 and 2007). They are constituted of interdigital or crossed metal fingers. They need a lot of via to connect all fingers. They are more difficult to check and a large attention is required to the position of the access points.

C. 3D and Trench capacitors

Trench capacitors were developed to increase the capacitance per unit area. The basic principle of this capacitor is to realize a vertical MIM capacitor as shown in Figure 3 with 4 metal levels (Jeannot et al., 2007). The obtained result gives a capacitance approximately 10 times higher than for planar MIM, but with a more complex process. An interesting structure is given by (Büyüktas et al., 2009) where they have design and realized trench capacitor in the front-end part (near active component). They have tested they capacitor up to 10 GHz.

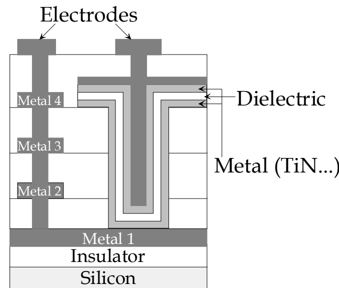

Fig. 3. Principle of 3D capacitor

2.1.2 Modeling and performances

The model of a capacitor is easier to develop if the context is not taken into account. From a perfect capacitor, it is necessary to complete the model by first taking into account dielectric losses. This can be done usually by adding a conductance in parallel with the inductance. In RF and millimeter waves, the influence of electrodes must be included in the model. At high frequencies, electrodes act like a lossy inductor. In fine, for an integrated capacitor it is necessary to take into account at minimum, coupling phenomenon with the substrate. Whatever the shape of the capacitor, the substrate under the lower electrode has a great importance on the behavior of the capacitor. Coupling between the lower electrode and the substrate can change all the parameters of the capacitor. (Arnould et al. 2004).

This lumped model of Figure 4 is the more commonly used. In this model, the series branch comprises the nominal capacitance of the dielectric (C_p), the losses in the dielectric (R_p), the resistance (R_s) and inductive behavior (Ls) of the metal electrodes. C_{ox}, C_{si} and R_{si} represent the complex capacitance to the substrate due to electrodes. C_{ox} is the substrate to top and bottom electrode capacitance. R_{sub} and C_{sub} are the frequency dependent substrate resistance and capacitance, respectively.

This model refers first to planar MIM capacitors. In fact, for the other structures of capacitors it can be change and some components of this model can be removed in accordance with the physical design of the capacitor. For example, if the first metallic layer

of the BEOL is a ground plane, the part taking into account the substrate can be removed. Distributed models has been studied (Cai et al., 2004; Lee et al., 2006-1) and give interesting results, but are more complicated and not used in microelectronic design kit.

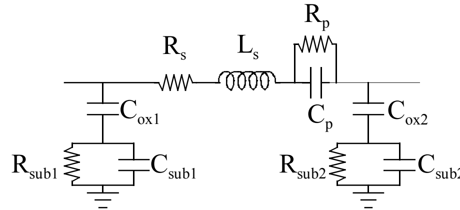

Fig. 4. The more commonly used electric model of capacitor

The factor of merit traditionally used is the quality factor. For a measured component, it is calculated after parameters extraction from the model. The quality factor depends mainly on the value of the capacitor and on losses. But the inductive effect of the electrodes limits its maximum frequency of use. Figure 5 shows a typical Q factor with the main parameters influence.

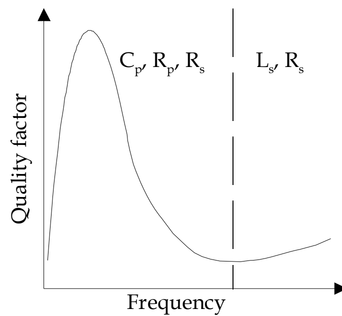

Fig. 5. Typical quality factor versus frequency and parameters influence

An important parameter to take into account when a capacitor is designed, is the position of the access lines with regard to electrodes. This is of great importance to reduce the electrodes resistance and to increase quality factor. To give an example, for a MIM capacitor realized in a 120 nm CMOS technology (Figure 2(a)), Table 2 summarize the value of the extracted parameters of the model (Lemoigne et al., 2006) for different shapes of electrodes. The biggest width gives the minimum resistance. This result can be extended to any kind of capacitor.

	W (µm)	L (µm)	C (pF)	R(Ω)	G (S)	L (pH)
C_0	66	66	3.5	4.2	$4.16\ 10^{-4}$	85
C_1	120	66	8	0.7	$4.16\ 10^{-4}$	85
C_2	174	66	11.5	0.1	$4.16\ 10^{-4}$	85

Table 2. Losses comparison for different shapes of capacitor

Finally, the choice of a capacitor having the highest capacitance density while preserving the other capacitor properties (leakage, stability, and reliability) depends on the technological parameters, but also on the frequency. For millimeter wave, capacitors of low value can be achieved with good performances.

2.2. Inductors

As for capacitors, inductors have been studied since a long time. Their performances are always a problem for designers. Integrated inductors can have mainly three forms:
A. Above IC Inductors
Inductors are added on the passivation layer at the end of the process. This technique of manufacture allows a greater freedom on the choice of materials, thicknesses and the shape of the components (Sun et al., 2006). But it is still at a stage of advanced research and not of industrialization for technological constraints.
B. Inductors of the type MEMS
It is an extension of the previous type with more complex structures using Micro Electro-Mechanical Systems (MEMS) and using micro-machining process (Jiang et al., 2000). The obtained components can be suspended in air. However, this type of structure suffers for the moment, of a low mechanical resistance and a perfectible reproducibility
C. BEOL inductors
The last possibility is to design inductors in the BEOL like capacitors. For this component the goals are more or less the same than for capacitors: the best inductor for the minimum occupied surface. They don't need modification of fabrication process and this is the best advantage. But they suffer from a poor quality factor and usually a great occupied surface as compared to the rest of electronic RF-circuit. This kind of inductor will be more detailed.
Advanced microelectronic technologies offer less thick metal layers. This induces an increase of limiting factors like skin effect. A second problem is the low resistivity of silicon substrates, required for latch-up of MOS transistors, which induces resistive losses.

2.2.1. Various inductors shapes

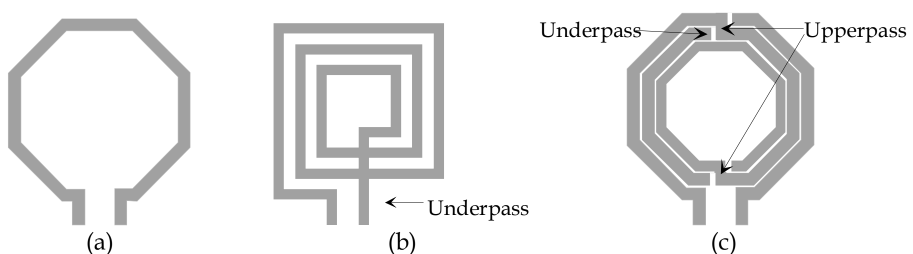

Fig. 6. (a) octagonal one turn inductor, (b) square inductor with one underpass, (c) symmetric octagonal inductor with several underpass and upperpass.

The more common shapes are square or hexagon (Figure 6). Usually hexagon is preferred to remove the right angles that are not favorable to operation with high frequencies. If the inductor value is low, a one-turn inductor can be designed. But for others values a multi-turn inductor is required. It can be designed using all metal layers of the BEOL. An

important parameter when using copper BEOL is the presence of dummies. Some rules must be respected as suggested by (Pastore et al., 2008-1). An important point when designing inductance is to take care to underpass and upperpass, because they can generate more losses due to via. As shown in example of Figure 6, only one turn inductors don't need to use two metal levels and consequently don't need via and upper or underpass.

2.2.2. Modeling and performances

The first integrated planar inductor on silicon was developed in 1990 by (Nguyen et al., 1990). In the same time they have proposed a basic model of Figure 7(a). In 2000, a modified model (Figure 7(b)), more close to fabrication process and geometry of inductor, was proposed by (Yue & Wong, 2000). An other model (Figure 7(c)), taking into account electromagnetic coupling with silicon substrate were developed by (Melendy et al., 2002). But, a wide band model was proposed by (Lee et al., 2006-2), where intrinsic and extrinsic refer respectively to the inductor and to the environment (Figure 7(d)). The choice of a model is greatly dependent of the technology and the shape of the inductor.

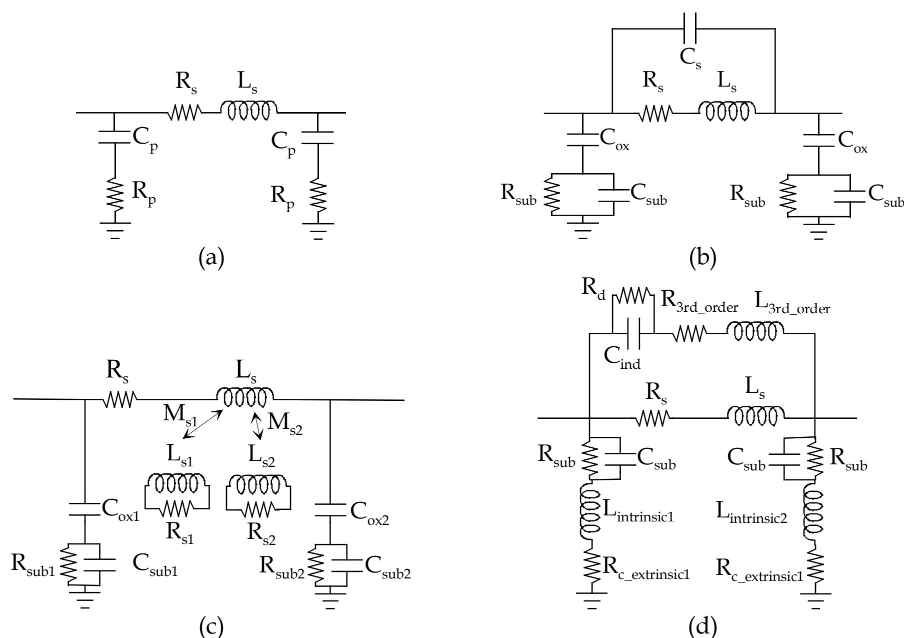

Fig. 7. Models of planar inductors, (a) (Nguyen & Meyer 90), (b) (Yue & Wong, 2000), (c) (Melendy et al.,2002), (d) (Lee et al., 2006-2)

These more or less complex models, must take into account various physical phenomena and geometrical parameters, coming from the design or which can have an influence on the design. The geometrical parameters are: the thickness and the dielectric constant of insulator used in the BEOL, the width of conductors, the spacing between two conductors for a spiral inductor, the inner diameter of the coil, the turns number for spiral shape, vias ensuring the passage from one metal level to an other for inductors using several metal levels. The

physical phenomena are: magnetic coupling between conductors, metallic losses (DC and skin effect in RF), Eddy current effects between conductors and silicon substrate.
If the models of Figure 7 are considered, it is possible to identify with more or less accuracy, the parameters listed below. For example, the components of Figure 7(b) represent: L_s the inductance, R_s ohmic losses in metal, C_s the capacitor between turns and between access points, C_{ox} the capacitor between metal layers and the silicon substrate, C_{sub} the capacitance of the substrate which is often negligible in the field of the radio frequencies as compared to the value of associated resistance R_{sub}.
As for the capacitors, the factor of merit traditionally used is the quality factor. For a measured component, it is calculated after components extraction from the chosen model. The quality factor depends mainly on the value of the inductor and on losses. Figure 8 shows a typical Q factor with the main parameters influence for the model of Figure 7(c).

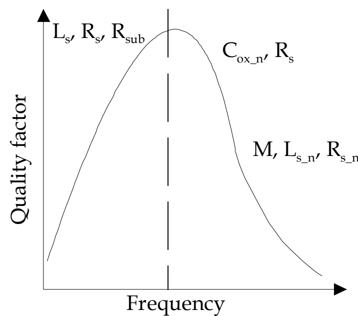

Fig. 8. Typical quality factor versus frequency and parameters influence

2.2.3. High performances inductors

To overcome the limitations induce by traditional BEOL, two possibilities were developed. The first is to use thick copper layers at the last level of BEOL and the second is to use SOI or porous silicon. Several works were done using porous silicon (Royet at al., 2003, Contopanagos & Nassiopoulou, 2007). They have obtained a Q factor of 32 with porous silicon at 3.8 GHz. But one of the best results was obtained by (Pastore et al., 2008-2). They have designed an octagonal symmetric inductors integrated in the hole six levels of BEOL. A high resistivity SOI substrate was chosen and an excellent Q factor of 34 at 4.5 GHz for a current capability of 57 mA/µm at 125°C was obtained.

3. High-Q slow-wave compact transmission lines and potential applications

3.1. State of the art

Conventional transmission lines such as microstrip, coplanar waveguides (CPW) and grounded coplanar waveguides (G-CPW), realized in industrial CMOS processes typically suffer from significant losses and poor quality factors in the RF and millimeter-wave ranges.
Actually, thin-film microstrip transmission lines are suitable for most circuits because of their compact layout. However, due to technology evolution and continuous decrease of the SiO_2 layer thickness, the signal line of the microstrip transmission lines has to be reduced in order to address 50Ω transmission lines, leading to an increase of the metallic losses. In

(Gianesello et al., 2006), integrated transmission lines showing attenuation losses of 0.9 dB/mm at 10 GHz, and 3 dB/mm at 60 GHz have been demonstrated. However, high-impedance transmission lines can not be realized due to a drastic increase of the attenuation loss, and no efficient miniaturization way has been identified.

Coplanar CPW transmission lines could be a good candidate for high-impedance integrated transmission lines. More flexibility in the design of the CPW transmissions lines is obtained by adjusting the gap to the signal line width. However, high losses occur, due to the dielectric loss in the low-resistivity silicon substrate. Attenuation loss of 2 dB/mm have been reported on conventional CPW transmission lines on silicon substrates fabricated through commercial CMOS foundries (Milanovic et al., 1998). Lower losses can be achieved (0.2 dB/mm and 0.6 dB/mm at 20 GHz and 60 GHz, respectively) by the use of a high-cost SOI CMOS technology using a high resistivity substrate (Gianesello et al., 2006). Besides, CPW quarter-wave transmission lines will result in relatively large occupying areas, depending of the working frequency on silicon substrates. Such areas, of course, are not compatible with the miniaturization concept of monolithic integrated circuits.

To reduce dielectric losses, a solution could be to use the grounded G-CPW configuration. Nevertheless, inserting a solid metal shield is not an optimum solution due to the eddy current's losses (Klevend et al., 2001). Moreover, inserting such continuous metal shield significantly reduces the characteristic impedance, thus making it more difficult to achieve transmission line characteristic impedances in the order of 50 Ω.

In order to overpass the limitations of microstrip, CPW and G-CPW technologies, in terms of quality factor and miniaturization, new topologies of coplanar transmission lines with improved performances were investigated. The slow-wave concept has been employed to shorten the wavelength and improve the quality factors of the transmission lines. A new topology of coplanar waveguides with floating strips has been introduced for the design of low-loss compact microwave on-chip systems.

The first coplanar waveguides with floating strips, firstly introduced by Hasegawa in 1977, were realized on GaAs substrates (Hasegawa & Okizaki, 1977). These transmission lines exhibit a slow-wave propagation phenomenon but suffer from high insertion losses. A few years later, the floating strips were placed above the CPW and the structure was named "crosstie overlay CPW" (Wang & Itoh, 1987). However, a large attenuation, mainly due to the large floating strips pattern geometry, was reported in (Hasegawa & Okizaki, 1977-Wang & Itoh, 1987). Indeed, these structures were realized using non-standard processes where the resolution was high enough to show the merits of the structure.

Afterwards, the same shielded coplanar waveguides (S-CPW) topology implemented in a BiCMOS technology has shown very interesting results with better performances (Cheung & Long, 2006).

Moreover, the reported benefits of shielded coplanar transmission lines have been supported by several equivalent circuit models in the literature. The first RLCG equivalent model was proposed in (Wang et al, 2004) to describe the line performance below the resonant frequencies. Later, nonphysical RLCG models for lossy transmission lines developed for simulating the extracted characteristic impedance and propagation constant showed good correlation with TDR measurements (Kim & Swaminathan, 2005). Unlike physical models where the transmission line parameters are correlated with the physical structure, the nonphysical models are extracted directly from the frequency response and, therefore, do not relate to the physical structure of the transmission line. Afterward, efforts

have been put into developing analytical expressions for the shielded transmission lines inductances to describe key performance figures with a good accuracy (Tiemeijer et al, 2007; Masuda et al, 2008). In (Wang et al, 2008), the authors tried to go further by calculating the inductance and the resistance of the shielded coplanar waveguides using the partial element equivalent circuits (PEEC) method. After all, the simplest RLCG model taking advantage of the well established models of grounded and standard coplanar waveguides was described in (Sayag et al, 2008).

3.2. Shielded coplanar waveguides transmission lines description

Figure 9(a) shows the 3D geometric view of the shielded coplanar waveguide transmission lines realized in (Kaddour et al, 2008). The four Copper metal layer 0.35-µm CMOS low-cost technology, as described in Figure 9(b), is used. The S-CPW geometric design parameters are the following: W, G, and Wg are the CPW central conductor, gap, and ground strip widths, respectively. *SL* and *SS* are the floating strip length and spacing, respectively. In order to reduce the transmission line conductive losses, a thick top metal layer is realised. The CPW is made on the 2.8 µm-thick top metal layer (M4) while the floating strips are patterned on the second highest metal layer (M3) with a thickness of 0.64 µm. The distance between the top metal (M4) and the bottom patterned shield (M3) is 1 µm.

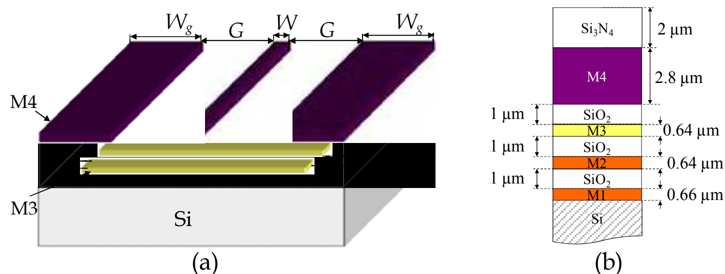

Fig. 9. (a) 3D geometric view of the slow-wave coplanar transmission line with floating metal strips. (b) Four copper metal layers 0.35-µm CMOS technology schematic description.

The patterned ground shield underneath the CPW transmission line acts as a perfect conductor for the electric fields, due to the small strip spacing SS (0.6 µm in the realized devices) compared to the silicon oxide thickness (1 µm). The magnetic field passes through the patterned ground. So, the capacitance per unit length is greatly enhanced, whereas the inductance remains quite unchanged. Therefore the phase velocity is reduced, predicting the slow-wave propagation behaviour. Thanks to the increase of the propagation constant, lower losses per wavelength are measured in S-CPW transmission lines leading thus to improved transmission lines quality factor defined as $Q=\beta/2\alpha$, where α is the attenuation constant, and β is the phase propagation constant.

In (Kaddour et al, 2008), a comprehensive study on the geometric factors affecting the S-CPW key performance figures was provided. Following the design guidelines published in (Kaddour et al, 2008), three sets of S-CPW transmission lines with different geometries were fabricated using the 0.35 µm CMOS technology. Figure 10 is a micrograph of the fabricated S-CPW transmission lines. Geometric specifications of the fabricated transmission lines are shown in Table 3.

The CPW dimensions (W and G) are chosen to reach a characteristic impedance near to 50 Ω with a high slow-wave factor. In order to reduce the conductive losses, the minimal central conductor width *W* is limited to 10 µm. Moreover, it has been demonstrated in (Kaddour et al, 2008) that narrow ground planes could be used to improve the high frequency electrical performances of the S-CPW transmission lines. Therefore, the ground plane width is set to 60 µm, limiting thus the footprint for all the fabricated S-CPW transmission lines. The metal shield is designed using minimized design rules, i.e. minimum allowed metal strip length (SL = 0.6 µm) and spacing (SS = 0.6 µm) in the 0.35-µm CMOS technology. Indeed, simulations carried out in (kaddour et al, 2008) have shown that insertion losses are reduced with the use of a finer ground shield pattern. Thus, the strip spacing should be kept to a minimum to boost the shield effect from the lossy silicon substrate while narrow metal strips should be used to minimize eddy currents.

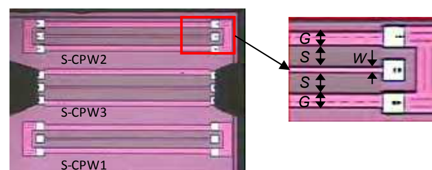

Fig. 10. Micrograph of the fabricated S-CPW transmission lines.

	W (µm)	G (µm)	W_g (µm)	SL (µm)	SS (µm)
S-CPW1	10	100	60	0.6	0.6
S-CPW2	18	100	60	0.6	0.6
S-CPW3	18	150	60	0.6	0.6

Table 3. S-CPW transmission lines geometrical dimensions.

3.3. Shielded coplanar waveguides transmission lines simulations and measurements

Figure 11-a compares the simulated (dashed lines) and the measured (solid lines) effective relative permittivity for the three fabricated S-CPW transmission lines, all simulations being carried out with the 3D Full-wave electromagnetic simulator: HFSS™. A good agreement is obtained between the measurements and the simulations of the S-CPW lines, except for the widest dimensions (G= 150 µm). The slow-wave phenomenon exhibited by the S-CPW transmission lines is highlighted by very high values of the measured effective relative permittivity ($36 < \varepsilon_{r\text{-eff}} < 48$). The higher slow-wave factor is obtained for the wider CPW dimensions (S-CPW3). The measured value is about eight times larger than that of a conventional CPW transmission line on a silicon substrate. This significant increase in the effective dielectric permittivity is very promising for the miniaturization of the overall size of RF components based on transmission lines.

Figure 11-b illustrates the comparison between the simulations (dashed lines) and the measurements (solid lines) of the attenuation constant α expressed in dB per millimeter. The attenuation constant is very low, comparable to state-of-the art results obtained with conventional MMIC transmission lines on silicon.

The quality factor is then derived in Figure 12. It increases with the frequency, and reaches 40 near to 30 GHz for the best case. With these values, the S-CPW quality factor is more than 3 times greater than that of the state-of-the-art conventional CPW transmission lines.

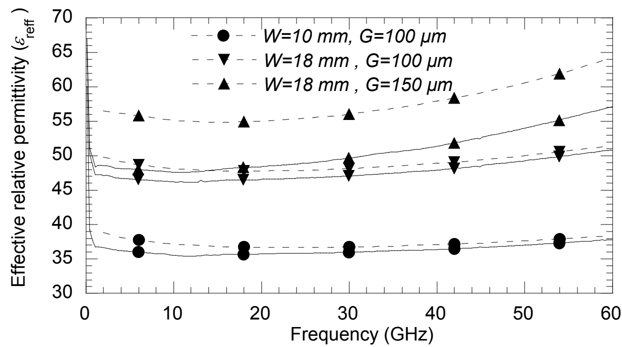

Fig. 10. Comparison of the EM simulated (dashed lines) and measured (solid lines) relative permittivity of the realized S-CPW transmission lines.

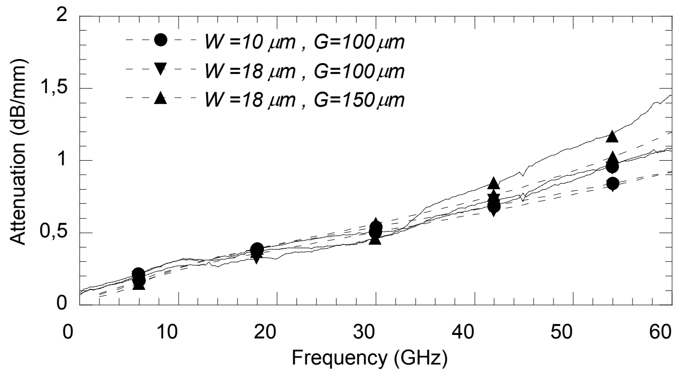

Fig. 11. Comparison of the EM simulated (dashed lines) and measured (solid lines) attenuation of the realized S-CPW transmission lines.

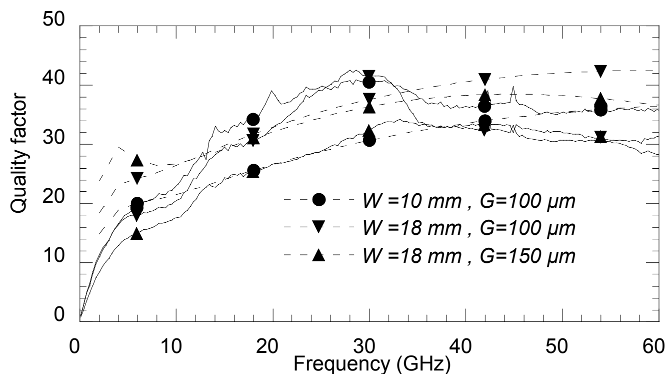

Fig. 12. Comparison of the EM simulated (dashed lines) and measured (solid lines) quality factor of the S-CPW transmission lines.

3.4. Shielded coplanar waveguides transmission lines applications

The measured results clearly show the interest of S-CPW transmission lines for achieving high quality factor and miniaturized transmission lines at millimetre-wave frequencies. Potential applications include several RF passive circuits in the millimetre-wave bands, such as filters, phase shifters, power dividers, and matching networks (Sayag et al., 2008). A simple and general approach for the design of narrow-band bandstop filters is based on an open-circuited stub. Based on S-CPW, two open-circuited stubs with the geometric dimensions W = 10 µm, G = 100 µm and W_g = 60 µm, were fabricated on a CMOS 0.35 µm technology. The micrograph of the S-CPW stubs is shown in Figure 13, with two open-circuited stubs showing lengths of 1.6 mm and 2.7 mm, respectively. The measured $|S_{21}|$ of both stubs is given in Figure 13. The ripples observed in the frequency response are due to the appearance of parasitic propagation modes near to the T-junction. Resonant frequencies occur at 4.4 and 7.5 GHz, respectively, for the long and the short stubs. With these measured resonant frequencies, an effective dielectric permittivity of 40 can be extracted. This value is in good agreement with the measured value in Figure 11. It is important to note, that the same resonant frequencies would be obtained with longer lines realized in a CPW classical technology. Thanks to the slow-wave factor, the length is reduced by a factor near to 3.

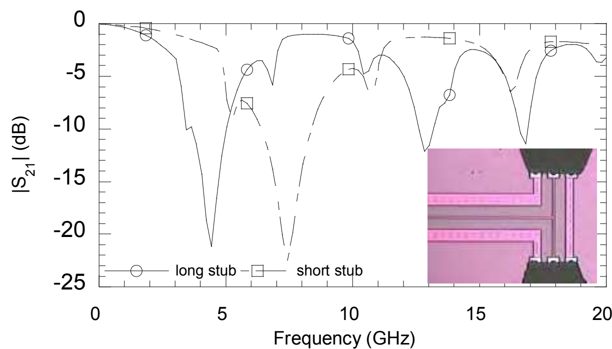

Fig. 13. Measurements of the transmission coefficient modulus $|S_{21}|$ of two stubs realized with S-CPW lines.

4. Integrated antennas and RF mm-wave interconnects

Two main problems can be identified concerning communications inside integrated circuits on one hand and on the other hand concerning 3D integration and communications systems that requires integrated antennas. The main objective is to demonstrate the feasibility of such components and to take into account the specific problem linked to the mm-Wave domain.

The continuous scaling down of transistor size makes high-speed digital and analog RF circuits achievable. In the same time, conventional global interconnect lines become a limiting factor due to their RC signal delay (ITRS 2003). As example, clock distribution networks are going to suffer from skew, jitter, power dissipation and area consumption for future generations of integrated circuits (Mehrotra & Boning, 2001). Alternative interconnect systems such as optical (Miller, 2002), 3D (Souri et al., 2000) or RF interconnects (Kim et al.,

2000) are required to overcome the limits of conventional interconnects. Among the possible solutions wireless interconnects has a great interest because they can be develop without modifying the technological steps. In particular antennas can be design using metal layers of integrated circuit of metal layer used 3D (SOC-SIP) integration.

4.1. Intra chip interconnect

Among possible planar antennas (patch, zig-zag, spiral...(Kim, 2000)), the dipole is chosen for its best compromise between performances and occupied surface.

Figure 14 represents a simplified schema of a pair of copper on-chip dipole antennas. We may distinct the dielectric layer (ε_r = 4.2) necessary to isolate the copper lines, the silicon substrate (ε_r = 11.7) and finally the backside metallization of integrated circuits. The antennas are designed to operate at frequencies around 30 GHz and are characterized by a length of 1.98 mm, a width of 10 µm and a spacing of 20 µm between the two branches. The distance between face to face antennas is 2.5 mm.

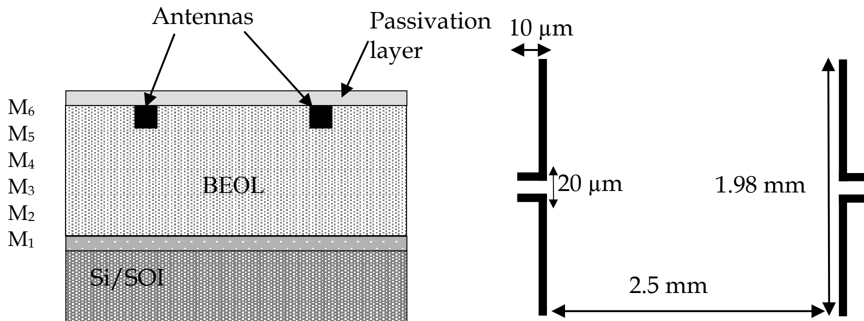

Fig. 14. Schematic view of antennas

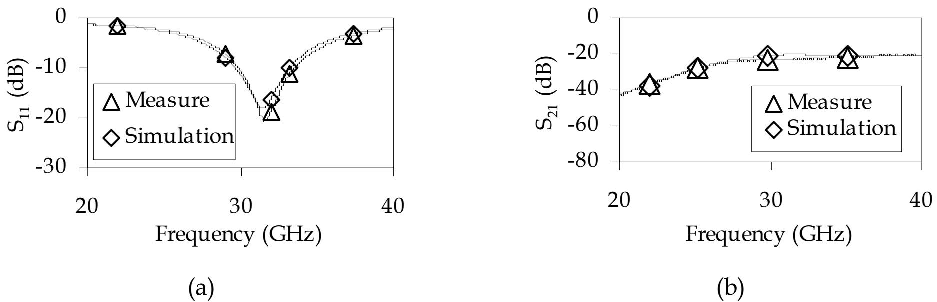

Fig. 15. Comparison between measure and simulation of S_{11} (a) and S_{21} (b) for a silicon bulk substrate of thickness 725 µm and resistitvity of 20 Ohm.cm.

Understanding the propagation of electromagnetic waves generated by such an antenna pair requires the comprehension of the propagation paths. When electromagnetic waves are travelling through one medium, phase velocity estimation can show through which medium the wave is travelling. However the case of on-chip antennas is quite different, as there are more than one medium involved in the waves propagation (air, dielectric, silicon) and

consequently multiple propagation paths. Actually there is no electromagnetic model describing with precision the propagation characteristics of waves generated by on-chip antennas. Consequently the modeling and simulation were done using a 3D electromagnetic solver with finite element method. The used model is based on the Greens functions resolution and it seems to be acceptable for any value of the substrate permittivity and thickness. It suggests that the surface wave number generated by the dipoles in a given frequency is a function of the substrate permittivity and thickness as the maximum energy involve in this transmission propagates inside the substrate. Figure 15 presents a comparison between simulation and measurement. A good agreement is observed for correct simulation conditions and for measurement with set up as discussed later.
The possible transmission of energy between two antennas disposed in the same plane is obtained by the wave propagation into the silicon substrate. Then, the substrate is important in the proposed configuration.
As the back end of line is about 6 µm thick, the most important is the silicon of which thickness can vary according to technological facilities from 1 mm to few hundred micrometers, if the substrate is thinned. The propagation path can be in a first approach considered as dielectric medium with ground shield on the bottom face. In this system the propagation of TE and TM modes is possible.
The cut-off frequency of these modes depends on the properties of the substrate: thickness and dielectric constant. These cut-off frequencies can be evaluate using the following equations (Pozar, 1998):

$$f_{cm} = \frac{m \cdot c}{2 \cdot h \cdot \sqrt{\varepsilon_r - 1}} \quad m = 0,1,2 \ \text{for}\ TM_m \ \text{waves} \tag{1}$$

$$f_{cm} = \frac{(2 \cdot m - 1) \cdot c}{4 \cdot h \cdot \sqrt{\varepsilon_r - 1}} \quad m = 1,2 \ \text{for}\ TE_m \ \text{waves} \tag{2}$$

From previous equations, for every propagation structure, there is always one mode that propagates, the TM_0. This mode is prevailing with a zero cut-off frequency.
In Table 4, the propagation modes cut-off frequencies are reported as function of the silicon substrate thickness. For the thickness of 975 µm, the TM_1, TE_1 and TE_2 occurs at different frequencies in the frequency band of the analysis. Consequently, the emitted energy by the excited antenna will be distributed on these modes with the increase of frequency. At higher frequency each mode will contribute to the propagation, but the attenuation will not be the same for each of them. The measurement results will give information about the transmitting energy and the effect of the multi-mode propagation at high frequency far from the mono-mode frequency excitation.

Thickness (µm)	f_c-TM_1 (GHz)	f_c-TE_1 (GHz)	f_c-TE_2 (GHz)
375	121	61	182
525	86	43	130
650	70	36	105
975	47	23	70
1300	35	17	52
1625	28	14	41

Table 4. Propagation Modes

For this kind of component the characterization method is of great importance. The resonance frequency and the frequency band change significantly next to a GS or to GSG excitation related to probes. This may be related to many effects like the difference in the excited propagated modes, or the difference in the antenna effective length for the two kinds of probes. This effect is very marked for low thickness substrates like the one used for the results of Figure 16 of which thickness is of 375µm, moreover this effect is dependent on the frequency of excitation and consequently on the wavelength of generated waves as compared to thickness.

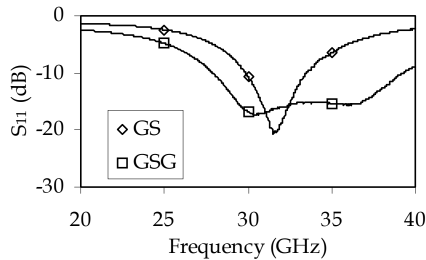

Fig. 16. Influence of probe type on reflection coefficient

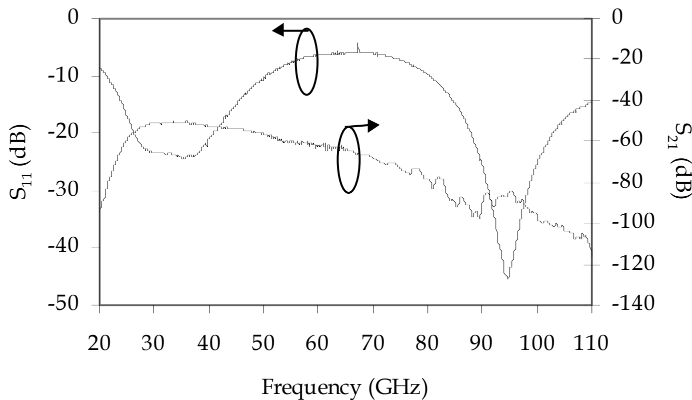

Fig. 17. Reflection and transmission coefficients of a pair of antennas up to 110 GHz

The previous antennas were also tested up to 110 GHz in order to verify their behavior at higher frequencies and the possible use of interconnects in millimeter range.
Figure 17 shows the reflection coefficient S_{11}. The first resonance of the antenna occurs at 31 GHz. The antenna was designed to operate around this frequency. The second resonance occurs at 95 GHz. This corresponds to a three half-wavelength resonance, as it can be predict by antenna theory. From this observation and taking into account the value of the reflection coefficient, it is possible to generate electromagnetic waves at 95 GHz with these antennas. This sharp resonance indicates a good matching with the 50 Ω source at this frequency, but this is not sufficient to ensure a good transmission.
A transmission gain of –25 dB is achieved in the band 30 to 45 GHz and the band pass at –3 dB is of 28 dB from 25 GHz to 50 GHz. For the second promising band around the second

resonance of 95 GHz, the transmission gain is -45 dB. This value is relatively low and therefore the transmission is possible but not so efficient as in the 25 GHz to 50 GHz range. If we compare this result with the propagation mode analysis, we can conclude that the multi-mode propagation frequency is not as good as a mono-mode transmission. The consequence is that, if it is possible to propagates waves at sub-millimeters frequencies, the efficiency can be improve by designing antennas in accordance with substrate thickness and frequency.
To conclude for intrachip interconnect, the best result was obtained at 30 GHz for antennas on high resistivity SOI substrates. The transmission gain was -15 dB and in comparison for low resisitivity silicon bulk substrate, without ground shield under the antennas, the maximum transmission gain was at -30 dB. Moreover this kind of interconnect are not different from usual ones in term of coupling (Triantafyllou et al. 2005; Rashid et al 2003).

4.2. Communications antennas for mm-waves

The increasing of wireless network needs demands the use of the broadband multimedia components to satisfy this performance. A new era, of future commercial communication devices in mm-wave range based on the 60 GHz unlicensed frequency band offers worldwide wideband operation (Nesic et al., 2001).
In particular, for dense local communications, the 60 GHz band for wireless personal area network (WPAN) applications (Figure 18) is of special interest for short-range communications, due to the RF attenuation of the atmospheric oxygen by 16dB/km, in a bandwidth of approximately 7GHz, centered around 60 GHz. Due to the spectrum availability (5-7 GHz) a variety of the short range high data rate applications may be targeted, in the scope from analog wideband transmission, up to digital GBit/s system solutions.

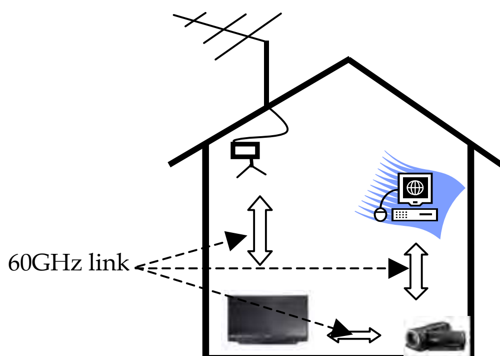

Fig. 18. Possible in-door home application scenario for both analog and digital application.

However, the interference due to attenuation of the atmospheric oxygen at 60GHz is very high link density (16dB/km) then the link distance is limited to 2 km at this frequency. A 60 GHz signal can only be intercepted in the tiny wedge and will only interfere with another 60 GHz link in that wedge (Guo et al., 2008).
To overcome the effects of atmospheric absorption and maintain reliability, radio links in millimeter wave region must use highly focused, or higher-gain, antennas in order to focus

as much as possible of the transmitted signal onto the receiving antenna. As RF frequency increases, signal wavelength becomes shorter, making it possible for smaller antennas to produce the required gain (Volakis, 2007).
In this frequency range and for that kind of transmission, antenna will not be integrated on silicon, but will be integrated by System on Chip (SOC) or System in Package (SIP) process. Some examples of millimeter waves antennas which offer the needed performances are presented: the patch antenna (Figure 19), the patch slot antenna (Figure 20), the Yagi antenna (Figure 21), the dipole (Figure 22). S-parameter are obtained by simulation with CST Microwave Studio. The resonance frequency of each antenna can be adjusted and the band width is lied to the type and geometry of the antenna. To obtain high gain an array can be build with these typical antennas (Volakis, 2007; Huang & Edwards 2006). These antennas can be realized by photolithographic process, with a roger 4003 substrate of ε_r=3.38, h=0.305mm, tanδ=0.0027 and with a 17µm metallization layer. Table 5 shows measured antenna gains for 64 and 256 antenna elements.

Type	Size (8x8)	Gain (dBi)
Patch antenna	11mmx11mmx0.61mm	24.87
Slot Patch Antenna	11mmx11mmx0.61mm	24.08
Yagi Antenna	11mmx6mmx11mm	26.54

Table 5. Gain of the different arrays antennas.

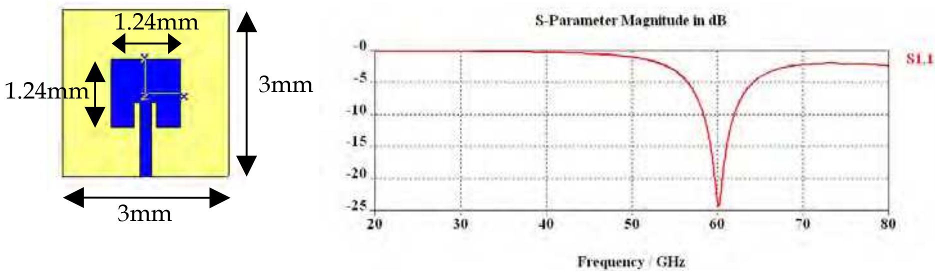

Fig. 19. Patch antenna millimeter wave and his S_{11}

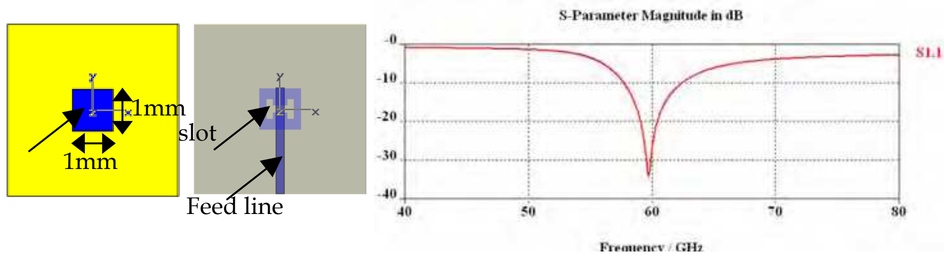

Fig. 20. Patch slot antenna millimeter wave and his S_{11}

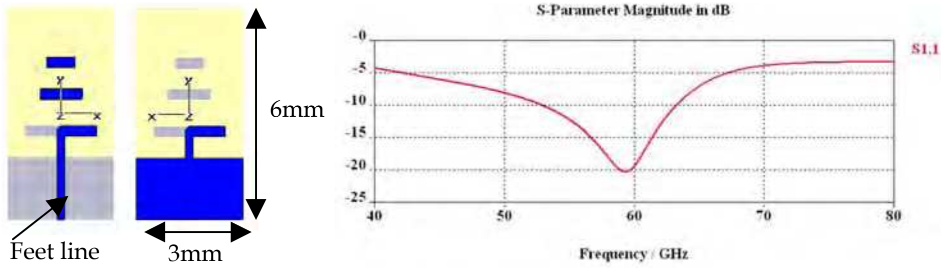

Fig. 21. Patch slot antenna millimeter wave and his S_{11}

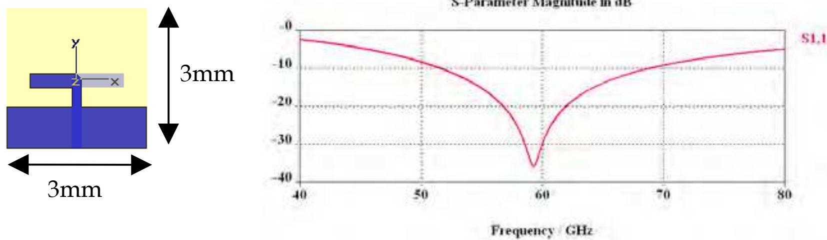

Fig. 22. Dipole antenna millimeter wave and his S_{11}

5. Impedance matching in RF domain

Microwave impedance matching is used to maximize the power transmission between two devices. This function is classically implemented in integrated front-end RF applications with antennas, power amplifiers (Figure 23), mixers or in noise figure systems (Abrie, 1985).

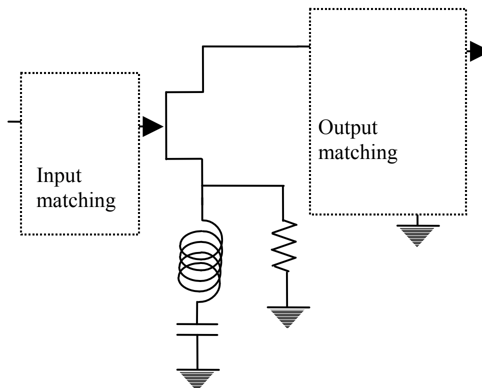

Fig. 23. Typical stand-alone MMIC amplifier with matching networks

The principal characteristics of matching networks that have to be carefully designed are the insertion losses, the reflection coefficient, the frequency band, the noise figure and the power consumption. The topology of the matching network has a great importance for the

overall behaviour and performances of the function. As it is shown, one can distinguish between lumped elements structures (Figure 24) or distributed elements ones (Figure 25).

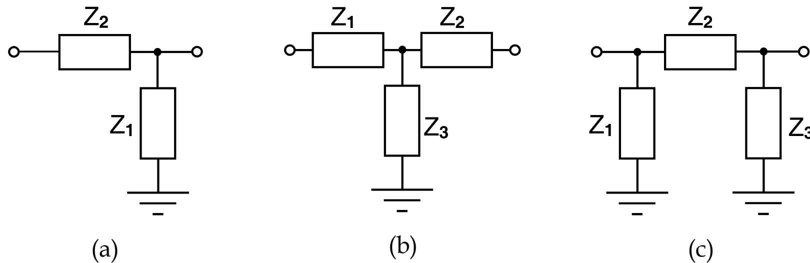

Fig. 24. Lumped topologies of matching networks, (a) two components, (b) T structure, (c) Π structure

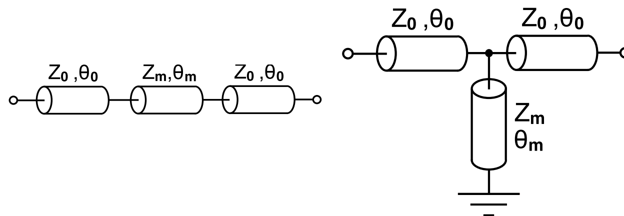

Fig. 25. Distributed topologies of matching networks with characteristic impedance Z and electric length θ

The design of the function is strictly equivalent in hybrid or integrated circuit (IC) technology but the size of the circuit is noticeably different since it is typically 1 cm^2 for the first technology and 1 mm^2 for the second one. Furthermore, the reachable operating frequencies are higher in IC technology than in hybrid one (typically 25 GHz against 2,5 GHz) but, on the contrary, the insertion losses are typically better in hybrid technology (0,2 dB against 3,5 dB). This last problem is due to the IC substrate RF behaviour and to low quality factors of IC transmission lines.
One of the main advantages of the IC technology for industrial matching networks is its very high reliability rate. Nevertheless, it has to be said that IC structures suffer from non-linearity behaviour at high power, even if some PIN diodes or transistors structures claim to operate up to 40 dBm. In the literature, very few data are reported on noise behaviour of IC matching networks although it shall not be a good point for that kind of structure.
Of course, due to the recent development of multiband and multistandard communications, some tuneable matching networks were realized and the flexibility of IC technology and the control of diodes or transistors brings some advantages in that frame (Sinsky & Westgate, 1997). In fact, the integrated circuit (IC) technology drastically reduces dimension of lumped components so of the devices, the order of magnitude becoming the millimetre. For a classical CMOS IC, such impedance tuning device is quite large but it is usual in RF front-end applications. The tunability is obtained as in hybrid technology, with the ability of switching transistors. For RF distributed components, typical IC substrates, like SOI or float-zone Si substrates are not convenient since the losses are too strong, with sometimes

insertion loss near 10dB. The quality factor of lines is poor because of conductors and dielectric losses. In (McIntosh et al, 1999; De Lima et al, 2000) devices were found from 1GHz to 20GHz. Higher frequency devices are difficult to design because of the dielectrics and conductors losses. Nevertheless, the main advantage of this technology is that the fabrication process is standard, and research prototype can be easily transferred to industry. Recently (Hoarau et al, 2008), have designed an integrated Π structure with a CMOS AMS 0.35µm technology of varactors and spiral inductors (Figure 26). Simulated results obtained with ADS show that only a quarter of the smith chart is covered on a 1 GHz band around the center frequency of 2 GHz. L structures could also be used to reduce the total number of components and the losses.

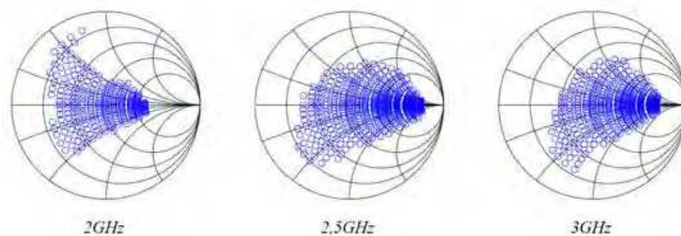

Fig. 26. Smith chart of simulated results of a CMOS AMS 0.35µm device for 3 frequencies

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