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Liquid Phase Oxidation on InGaP and Its Applications

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1. Introduction

High-electron-mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) have attracted many attentions in high speed and power applications due to the superior transport properties. As compared to AlGaAs pseudomorphic HEMTs (PHEMTs), InGaP-related devices have advantages, such as higher band gaps, higher valence-band discontinuity [1], negligible deep-complex (DX) centers [2], excellent etching selectivity between InGaP and GaAs, good thermal stabilities [3-5], higher Schottky barrier heights [3], and so on. Particularly, the use of an undoped InGaP insulator takes the advantages of its low DX centers and low reactivity with oxygen [6-10], which may still suffer from the high gate leakage issue. In order to inhibit the gate leakage issue, increase the power handling capabilities, and improve the breakdown voltages, a metal-oxide-semiconductor (MOS) structure has been widely investigated. However, it is still lacks a reliable native oxide film growing on InGaP, and very few papers have reported on InGaP/InGaAs MOS-PHEMTs. In addition, the MOS-PHEMT not only has the advantages of the MOS structure (e.g., lower leakage current and higher breakdown voltage) but also has the high-density, high-mobility 2DEG channel.

Over the past years, a study on the liquid phase oxidation (LPO) of InGaP near room temperature has been done [11-14]. The application of surface passivation to improve the InGaP/GaAs HBTs' performance has also been first demonstrated [13]. The InGaP/GaAs HBTs with surface passivation by LPO exhibit significant improvement in current gain at low collector current regimes due to the reduction of surface recombination current, as compared to those without surface passivation. Moreover, a larger breakdown voltage and a lower base recombination current are also obtained. In this chapter, the oxide film composition and some issues are addressed. Then a thin InGaP native oxide film prepared by the LPO as the gate dielectric for InGaP/InGaAs MOS-PHEMTs application are discussed, and the comparisons between devices with and without LPO passivation on the InGaP/GaAs HBTs are also reviewed.

2. Characterization of the oxide film

The root mean square (rms) value of surface roughness for the $In_{0.49}Ga_{0.51}P$ sample is estimated to be 1.1 nm before oxidation (i.e., as received) by AFM measurement, and can be

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improved to 0.95 nm after oxidation (i.e., as grown), as shown in Fig. 1. Fig. 2 shows the SIMS depth profiles before and after liquid phase oxidation on $In_{0.49}Ga_{0.51}P$. Although LPO on InGaP material has a much slower oxidation rate which is less than 10 nm/h, as comparing to that of the GaAs material, however, it is still feasible to grow a thin oxide film without pH control [15, 16]. The oxidation rate becomes significantly saturated when the oxidation time is longer than an hour, which is measured using a Veeco Instrument DEKTAK and confirmed by SEM.

The XPS depth profiles of the LPO-grown oxide for $In_{0.49}Ga_{0.51}P$ are shown in Fig. 3(a). Fig. 3(b)-(d) show the XPS surface spectra of the Ga-3d, In-3d, and P-2p core levels, respectively. The binding energies for all spectra are calibrated with the reference (as-received) signal. The as-received sample was dipped into a solution of $HF:H_2O$ = 1:200 for 30 s before measurement. From Fig. 3(c)-(d), in comparison with the previous paper [17], the spectrum is rather similar to that of $InPO_4$. This is also confirmed by the values of the O-1s peak energy and energy separations between the main core levels (i.e., Ga-3d, In-3d, and P-2p) in the oxide phases [18]. This clearly suggests that the oxide film is mostly composed of $InPO_4$-like and Ga oxide. In addition, the oxide film may appear to be etched back in the growth solution after 2 h of oxidation. The thermal stability of the oxide layer is also important in

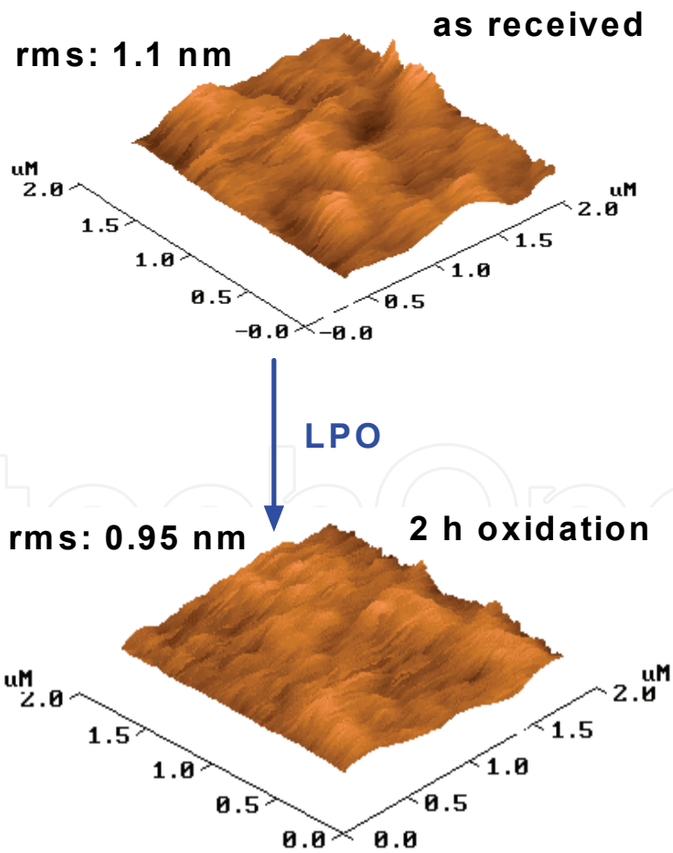
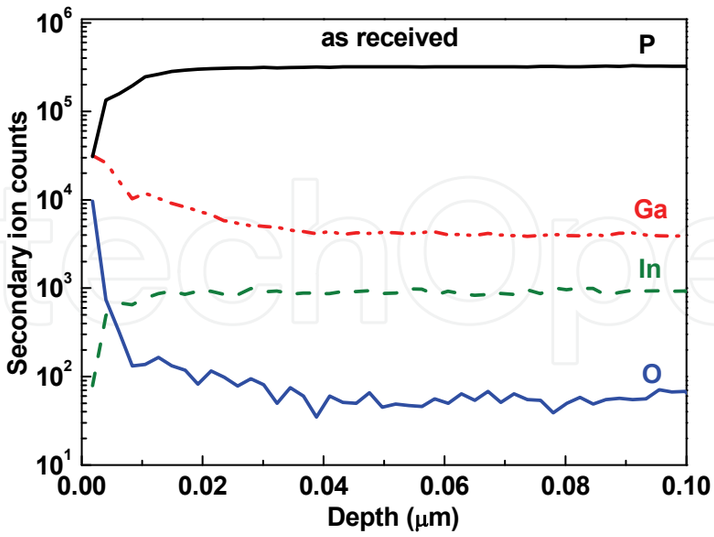


Fig. 1. AFM images of the $In_{0.49}Ga_{0.51}P$ sample before (i.e., as received) and after (i.e., as grown) liquid phase oxidation.



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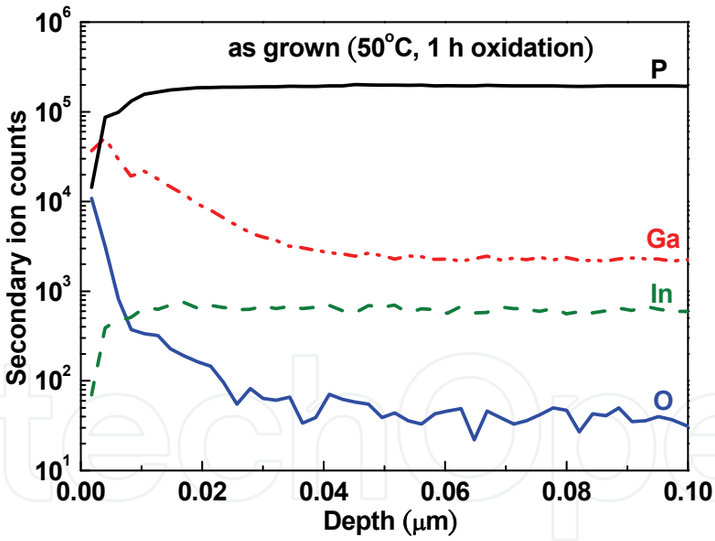
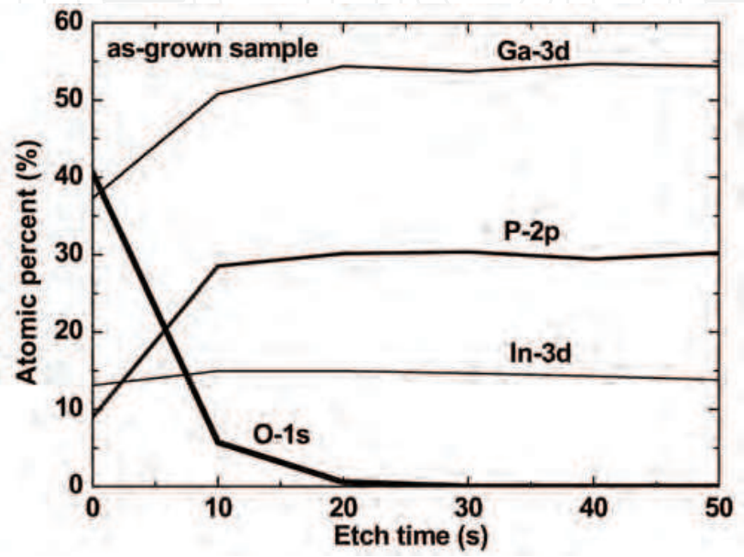


(b)

Fig. 2. SIMS depth profiles of the $In_{0.49}Ga_{0.51}P$ sample before (i.e., as received) and after (i.e., as grown) liquid phase oxidation.

device fabrications because high-temperature processes are usually required. Again, XPS is utilized to also important in device fabrications because high-temperature processes are usually required. Again, XPS is utilized to analyze the surface chemistry of the oxide films, as shown in Fig. 3. After 2 h of oxidation, the RTA processes were performed in a furnace

with N_2 flowing at 300-700 °C for 1 min [13]; however, a peak of $InPO_4$-like is still observed. $InPO_4$ (bandgap energy = 4.5 eV) is chemically stable and has rather good dielectric properties [19]. As a result, the $InPO_4$ probably acts as a capping layer for the entire oxide film to enhance the thermal stability. However, the experimental results show that high-temperature treatments (700 °C) will change the properties of Ga_2O_3, since the XPS energy peak of Ga_2O_3 shifts to a lower binding energy, and the binding energy is inferred to form the GaO_x or Ga_2O_x.



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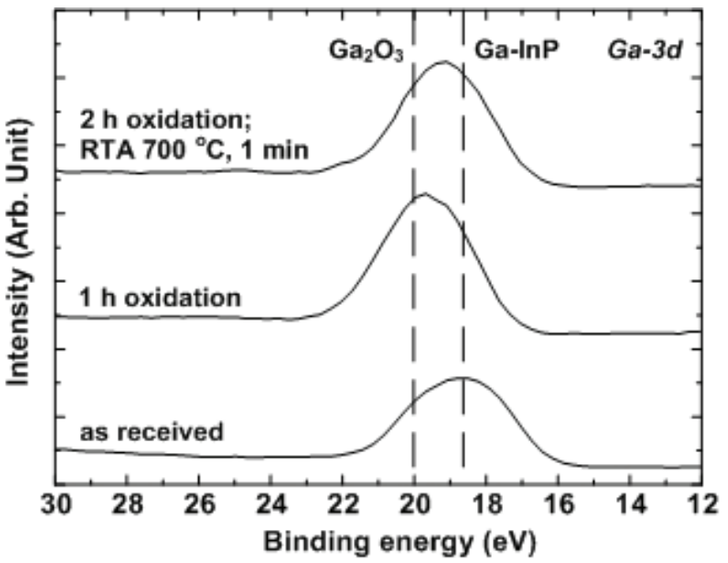

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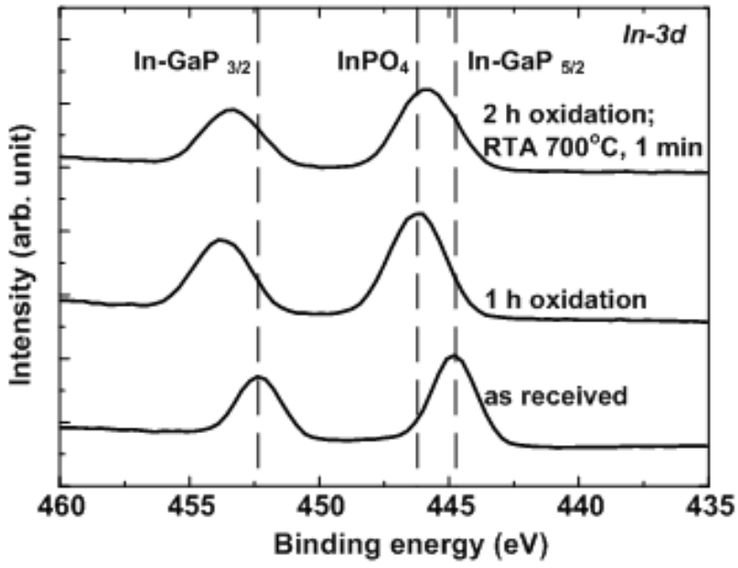

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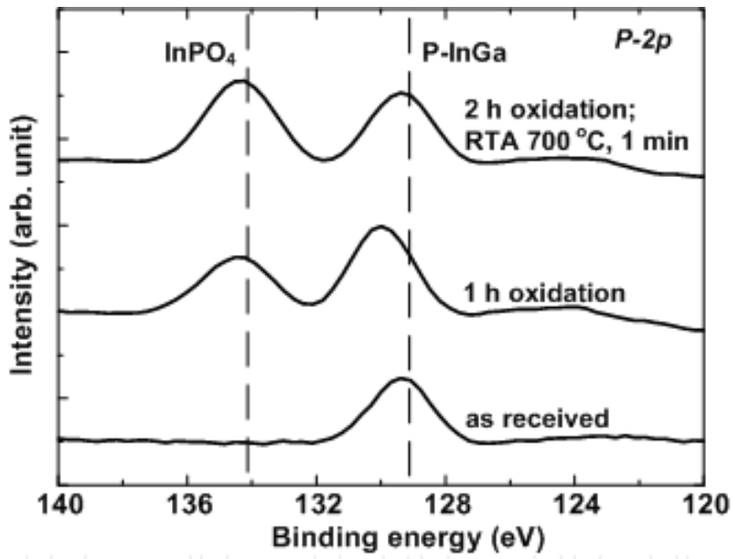


(d)

Fig. 3. (a) The XPS depth profiles of the as-grown oxide film on $In_{0.49}Ga_{0.51}P$.
The (b)-(d) show the XPS surface spectra for the Ga-3d, In-3d, and P-2p core levels, respectively.

3. InGaP/InGaAs MOS-PHEMT

3.1 Experimental

Figure 4 schematically shows the PHEMT structure grown by the metallorganic chemical vapor deposition (MOCVD) on a semi-insulating GaAs substrate. Hall measurement indicates that the electron mobility is 4000 $cm^2/V \cdot s$, and the electron sheet density is 2.2×10^{12} cm^{-2} at room temperature [11]. The device isolation was accomplished by mesa wet

etching down to the buffer layer. The ohmic contacts of the Au/Ge/Ni metal were deposited by evaporation and then were patterned by lift-off processes, followed by RTA. The depth of gate recess is 110 nm for reference PHEMT and 100 nm for MOS-PHEMT. After etching the capping layer and the partial Schottky layer, an LPO growth solution was used to generate the gate oxide for the MOS-PHEMT at 50 ^{o}C for 30 min. Finally, the gate electrode was formed with Au. Moreover, the oxide layer, as illustrated in the figure, also selectively and simultaneously passivated the isolated surface sidewall. The gate dimension is 2×100 μm^2 with a drain-to-source spacing of 5 μm.

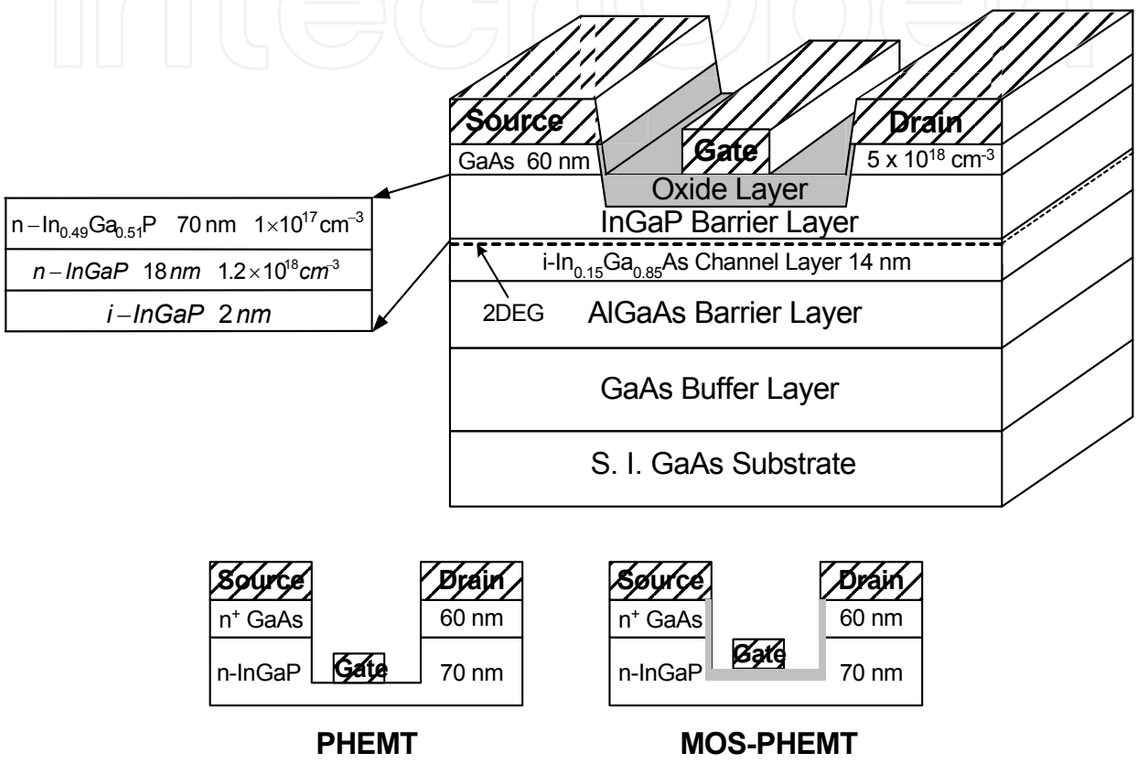
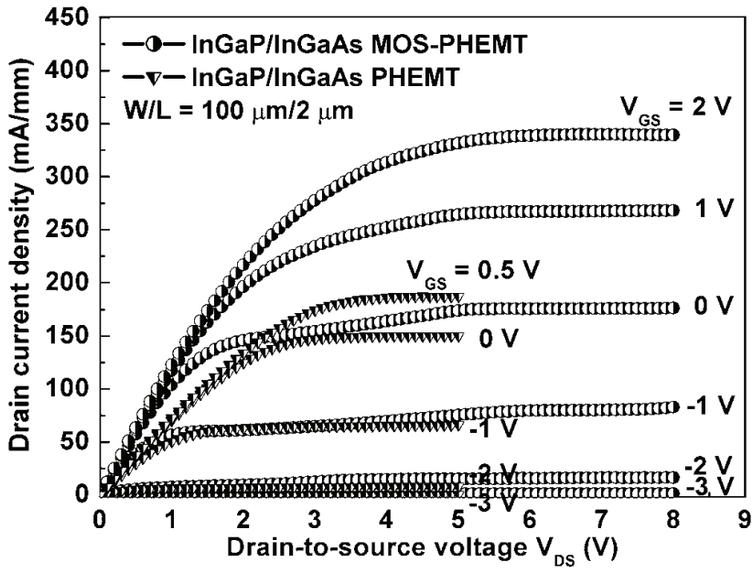


Fig. 4. The schematic drawing of the InGaP/InGaAs MOS-PHEMT.

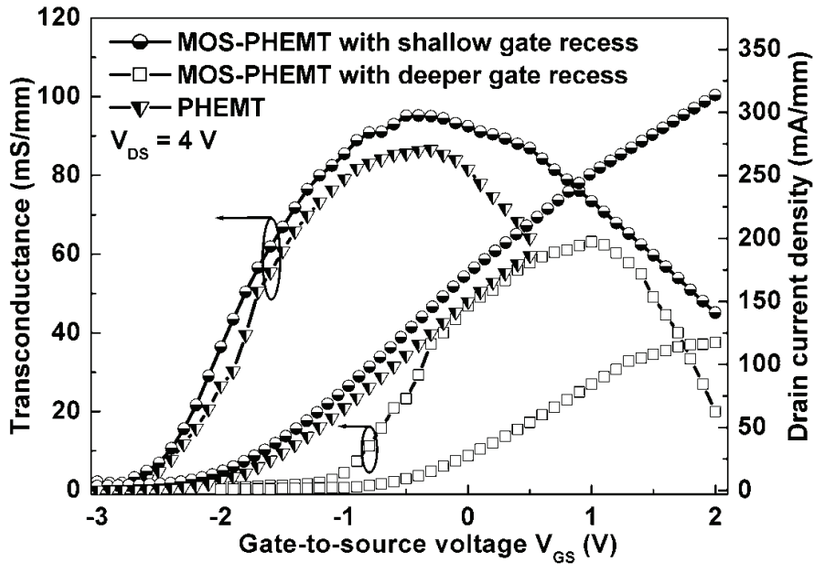
3.2 Results and discussion

Figure 5(a) compares the measured I-V characteristics of the MOS-PHEMT with those of the reference PHEMT fabricated under identical conditions. Clearly, good pinch-off and saturation current characteristics are obtained. Due to the higher energy barriers between the metal gate and the Schottky layer, the MOS-PHEMT can be operated at higher gate-to-source voltage (V_{GS}) and drain-to-source voltage (V_{DS}) than those of the conventional Schottky gate PHEMT, which can enhance the current driving capability. Fig. 5(b) compares the transconductance g_m and the drain current density I_D as a function of V_{GS} at V_{DS} = 4 V of the MOS-PHEMTs with those of the reference PHEMT. For MOS-PHEMT, the 1.8 V-wide gate voltage swing (defined by 10% reduction from the maximum g_m) is higher than that of the PHEMT. The threshold voltage V_{th} of MOS-PHEMT shifts to the left, which is similar to the result of the one with oxide deposited on the Schottky layer [20, 21]. However, the separation region between the oxide-InGaP interface and the InGaAs channel for MOS-

PHEMT is still larger than that of the reference PHEMT in this study, so the drain current density of the PHEMT is smaller than that of the MOS-PHEMT at the same bias V_{GS} due to the decrease of the carrier concentration within the InGaAs 2DEG channel.



(a)



(b)

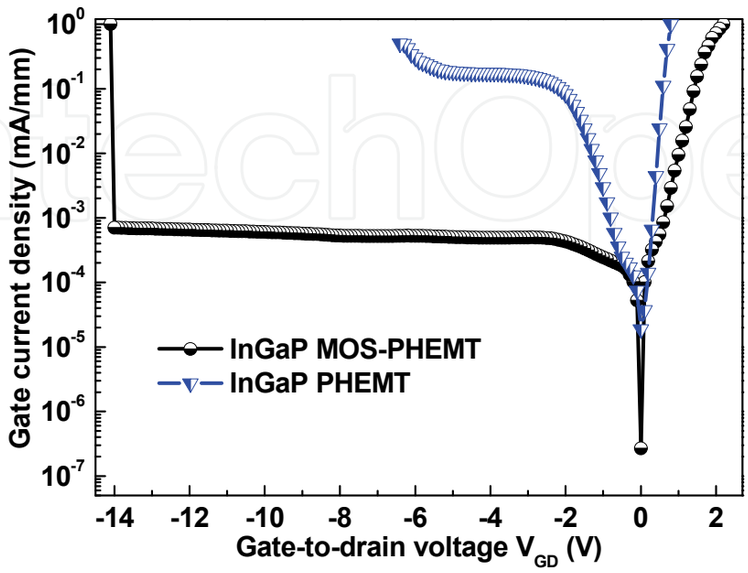
Fig. 5. (a) Measured I-V characteristics of MOS-PHEMT and PHEMT. (b) The transconductance and the drain current density versus V_{GS} at V_{DS} = 4 V for the MOS-PHEMT and the reference PHEMT.

In addition, if the depth of gate recess is etched to be 120 nm, the V_{th} becomes more positive, -0.5 V, for MOS-PHEMT with the identical processing conditions including initial pH value (5.0), temperature (50 ^{o}C), and oxidation time (30 min). For V_{th} shifts to the right, the separation between the oxide-InGaP layer interface and the InGaAs channel layer is decreased due to the consumption of the InGaP during the processes of gate recess and the unique properties of the LPO with the reaction of InGaP, leading to the increase of the total effect of the gate bias on the control of V_{th}. However, a decrease in the maximum g_m, 63 mS/mm, accompanies the degradation in the saturation current, 84 mA/mm at V_{GS} = 1 V. The result is also confirmed by a longer oxidation time, i.e., a thicker oxide layer. This drawback can be overcome by suitable device structures, such as inserting a Si-planar doping layer under the InGaAs channel to increase the carrier density.

The oxide film provides an improvement in the breakdown voltage in terms of the gate leakage current of the MOS structure, supported by the typical gate-to-drain I-V characteristics, as shown in Fig. 6(a). For InGaP MOS-PHEMT, the turn-on voltage, 2.2 V, is obviously higher than that of InGaP PHEMT, 0.8 V, and the corresponding reverse gate-to-drain breakdown voltages, BV_{GD}, are -14.1 V and -6.5 V, respectively. The turn-on voltage and the BV_{GD} are defined as the voltage at which the gate current reaches 1 mA/mm. The gate leakage current can be suppressed at least by more than two orders of magnitude with an oxide film at V_{GD} = -4 V. The smaller gate leakage current of MOS-PHEMT is due to the MOS structure and the elimination of sidewall leakage paths that are directly passivated during the oxidation, which is consistent with the result of Fig. 5. In addition, the gate leakage current observed in MOS-PHEMT comes from a gate leakage path at the edge of the mesa [22] that is not present in the MOS capacitor, which may contribute to the Schottky-like I-V characteristics for forward biases. Fig. 6(b) shows the gate current density as a function of reverse V_{GS} at different V_{DS}. Due to the high electric field existing in the gate-to-drain region, hot electron phenomena occur in the narrow band-gap InGaAs channel. Electrons can obtain higher energy to generate electron-hole pairs through the enhanced impact ionization, resulting in easy injection of the holes into the gate terminal [23]. However, in InGaP-related devices, it is more difficult for the holes generated by the impact ionization to overcome the valence band discontinuity and to reach the gate [4], so the bell shaped behavior of the impact ionization does not appear in Fig. 6. Moreover, the gate current density of MOS-PHEMT is significantly improved, which is less than 0.5 μA/mm, as compared to that of PHEMT. In other words, the electrons and holes generated by the impact ionization are decreased to further reduce the drain and gate currents owing to the oxide layer with a high barrier height.

In order to have a better insight into the transient behavior of the studied devices, the gate pulse measurements were performed using a Tektronix 370A curve tracer [24]. V_{GS} was pulsed from the V_{th} to 0 V with a pulsewidth of 80 μs, while V_{DS} was swept from 0 to 4 V. The comparisons between the static and pulsed I-V characteristics for PHEMT and MOS-PHEMT are shown in Fig. 7. The drain current of PHEMT decreased by 9.8%, while the MOS-PHEMT decreased by only 0.63%. To the best of our knowledge, if the pulsewidth is too short, electrons captured by the traps do not have enough time to be fully emitted. However, if the pulsewidth is long enough, all the trapped electrons are de-trapped and will contribute to the drain current. We believe that the differences between dc and pulsed I-V become evident by applying shorter voltage pulses to the gate such as less than 10-μs pulses for PHEMT and MOS-PHEMT. Therefore, it is clear that the oxide passivation on the

Schottky layer can minimize the effect of surface traps, which is consistent with the lower gate leakage current in Fig. 6.



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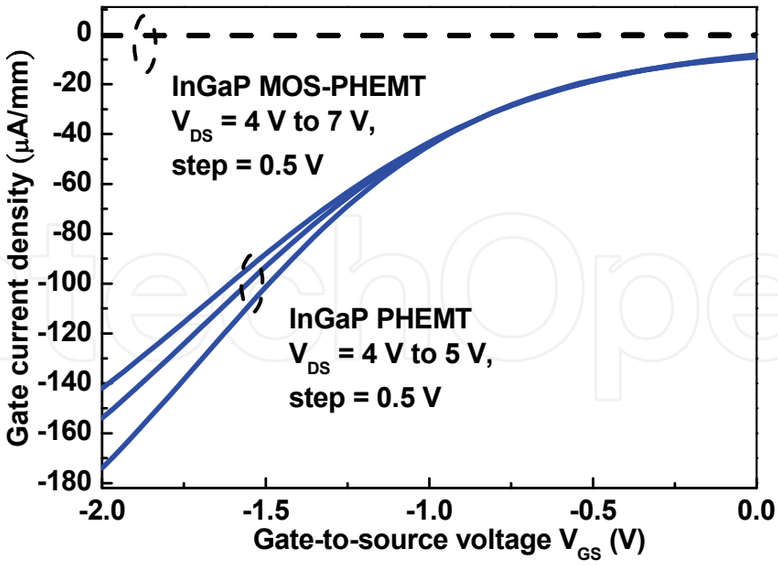
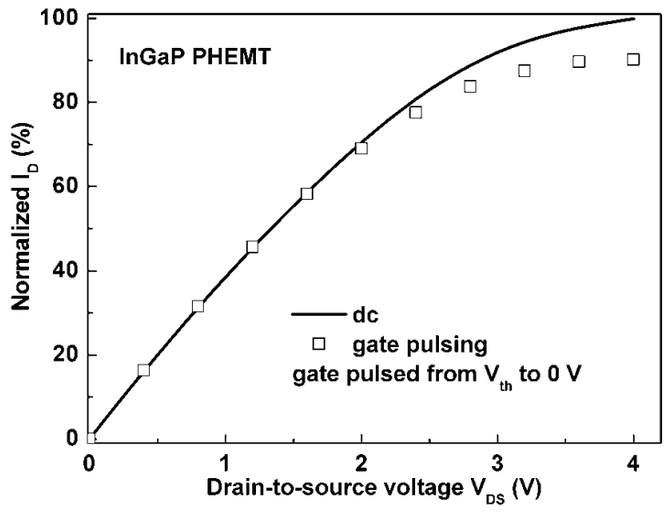


(b)

Fig. 6. (a) The typical I_G-V_{GD} characteristics of PHEMT with and without an oxide film. (b) The gate current density versus reverse V_{GS} at different V_{DS}.



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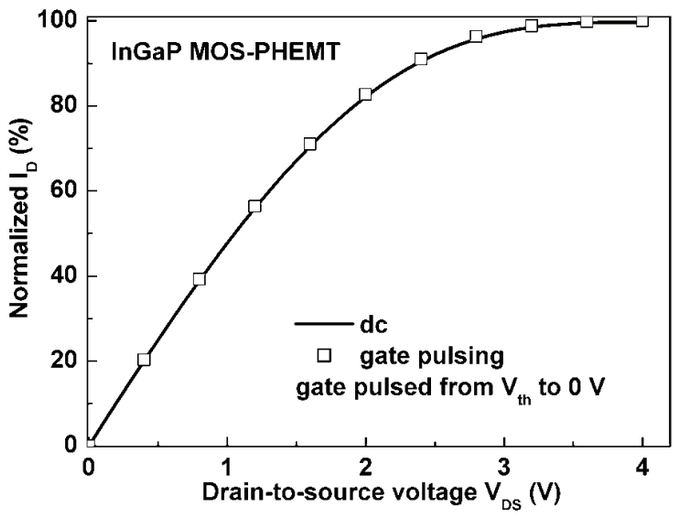


(b)

Fig. 7. Gate pulse measurements for (a) reference PHEMT and (b) MOS-PHEMT with V_{GS} pulsed from V_{th} to 0 V with a pulsewidth of 80 μs, while V_{DS} was swept from 0 to 4 V.

4. InGaP/GaAs HBT with LPO passivation

4.1 Experimental

The structure used for HBT is given in Table 1. The epilayers were grown by a low-pressure MOCVD system on an (100)-oriented semi-insulating (S.I.) GaAs substrate. For InGaP/GaAs HBTs, device fabrication began with emitter definition. The emitter cap layer was removed and stopped at the InGaP active layer. After removing the InGaP layer, a growth solution

was used to form the base oxide (passivation) on the exposed extrinsic surface of base and the base contact was then deposited. Finally, the mesa of base was defined and etched to sub-collector before the collector contact deposition. H_3PO_4-based etchant was used for GaAs and InGaP. The Au/Ge and Au/Be metals were deposited by evaporation and patterned by lift-off processing to form emitter, base and collector regions, respectively.

Layer	Material	Thickness (nm)	Dopant (cm^{-3})
Cap	InGaAs	45	1×10^{19}
Graded	InGaAs	45	1×10^{19}
Sub-emitter	GaAs	130	5×10^{18}
Emitter	InGaP	40	3×10^{17}
Base	GaAs	100	4×10^{19}
Collector	GaAs	750	1×10^{16}
Etching-stop	InGaP	20	5×10^{18}
Sub-collector	GaAs	600	5×10^{18}
S.I. GaAs substrate			

Table 1. The epitaxial structure of InGaP/GaAs HBT.

4.2 Results and discussion

Figure 8 shows the common-emitter I-V characteristics of the HBT with and without surface passivation by LPO. Clearly, the dc current gain (β) of HBTs with passivation is improved (increased) 15% when comparing to HBTs without passivation. The higher β with surface passivation is due to the reduction of the surface recombination current in the exposed extrinsic base regions by LPO method. The common-emitter I-V characteristics of the devices with and without surface passivation at low collector current regimes are shown

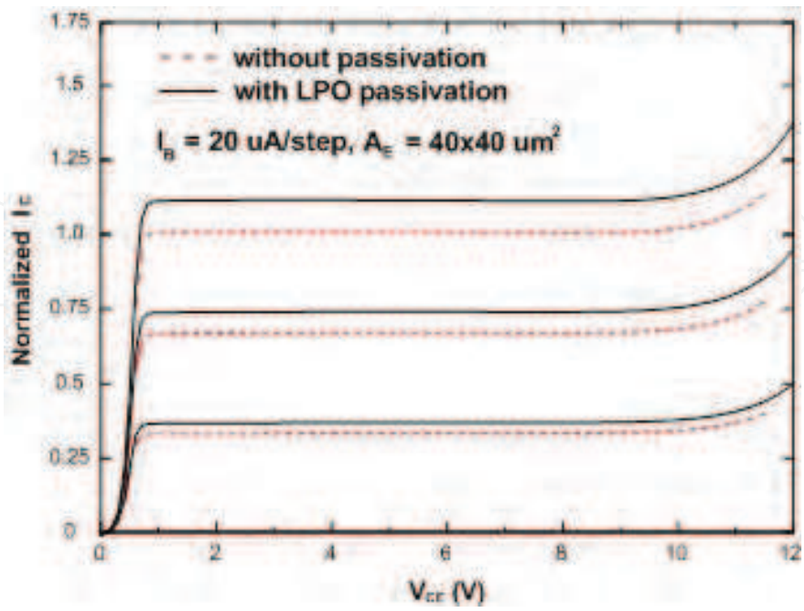
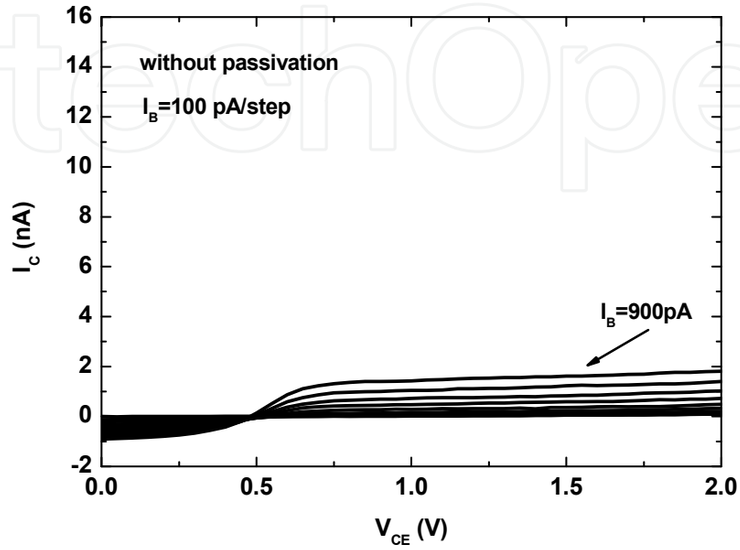


Fig. 8. Common-emitter I-V characteristics of the HBTs with and without LPO passivation.

in Fig. 9. The devices with surface passivation have higher common-emitter β than those devices without passivation, due to the reduction of the surface combination velocity by using an oxide layer on the base surface. In addition, the β values with and without passivation are 13.3 and 2 at I_B = 900 pA, respectively. The maximum increase of 7 fold in the current gain at collector current down to nA level.



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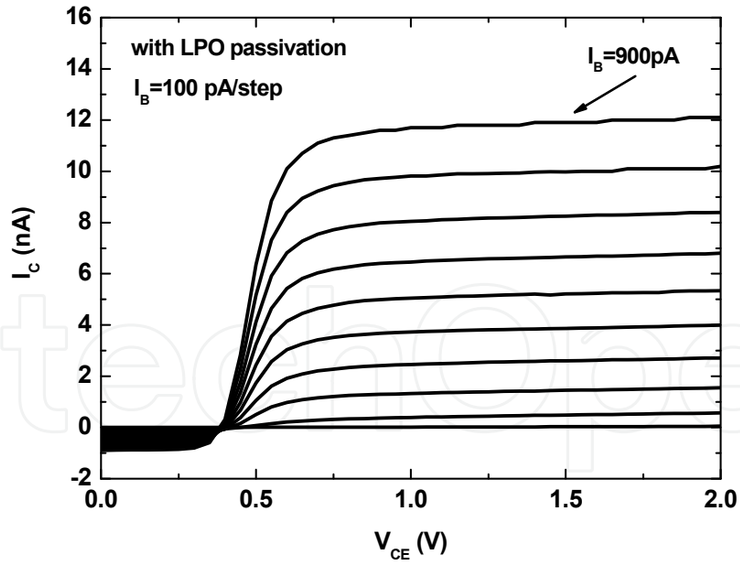

(b)

Fig. 9. Common-emitter I-V characteristics of the HBTs (a) without and (b) with LPO passivation at low collector current regimes.

Figure 10 illustrates the measured Gummel plots of the devices with and without LPO passivation. The collector currents are almost identical without being affected by the passivation treatment. However, a decrease of the base leakage current at low collector

current levels is obviously observed after oxidation. Moreover, it is found that the recombination current at the extrinsic base region and the base-emitter perimeter are competed against one another, resulting in current reduction at lower base-emitter bias V_{BE} = 0.4 V. The increasing β is owing to the reduction of the surface recombination current. It can also be indicated that the device with pasivation exhibits higher β than that without passivation at lower V_{BE} bias. The comparison of β versus the collector current is shown in Fig. 11. The collector-base bias is maintained at 0 V. Clearly, the device with LPO passivation shows wider collector regimes from 10^{-10} A to 0.1 A. And the maximum shift of

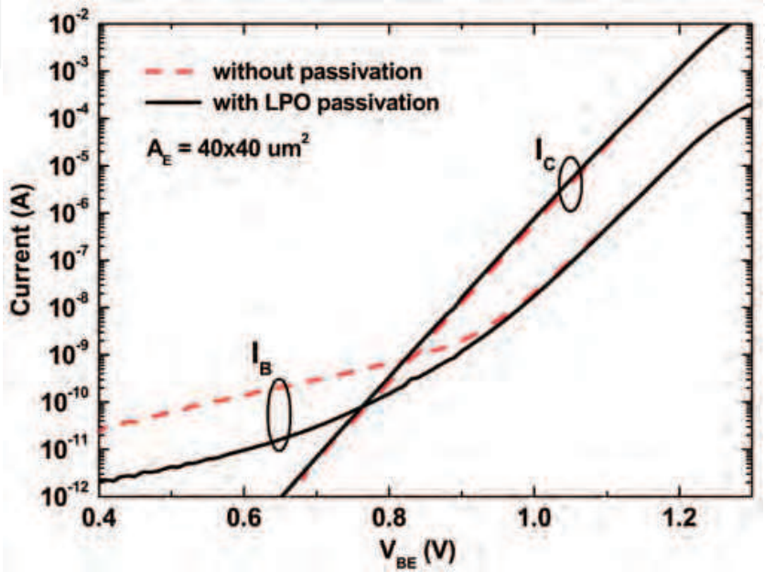

Fig. 10. Typical Gummel plots of InGaP/GaAs HBTs with and without LPO passivation.

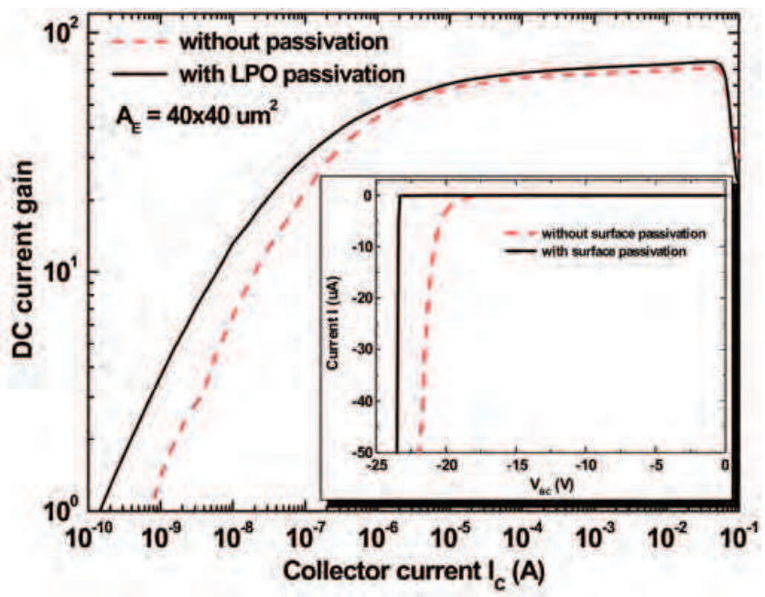

Fig. 11. Comparison of the β against the collector current I_C. The inset shows the base-collector junction breakdown characteristics with and without LPO passivation.

5 fold in the current gain from collector current of 8.1×10^{-10} A to 1.6×10^{-10} A can be achieved. This is attributed to the surface state density are suppressed, i.e., the surface recombination current is effectively reduced. The inset shows the base-collector junction current against bias voltage for the devices with and without passivation. For the device with passivation, the breakdown voltage (23.5 V) is higher than that (21.9 V) without passivation at I = 50 μA. The smaller leakage current is owing to the reduction of the surface recombination by the native oxide passivation in the base region. Above results clearly indicate that the β at low (medium) collector current regimes and the breakdown voltage will be increased. Additionally, the base current is decreased for the devices with passivation when comparing to those without passivation, which will be beneficial to low-power electronics and communication applications.

5. Conclusion

The InGaP/InGaAs/GaAs MOS-PHEMT with the $In_{0.49}Ga_{0.51}P$ oxide as the gate insulator prepared by LPO has been demonstrated. As compared to the counterpart of the conventional InGaP PHEMT, the proposed InGaP MOS-PHEMT can further reduce the gate leakage current at least by two orders of magnitude, increase the breakdown voltage by 200%, and enhance the gate voltage swing. Also, the pulse transient measurement shows much less impact of the surface trap effects for the InGaP MOS-PHEMT. In addition, as compared to the conventional InGaP/GaAs HBTs without surface passivation, the HBTs with LPO passivation possess the characteristics of lower surface recombination currents, higher breakdown voltage and improved higher dc current gain. The HBTs with LPO passivation exhibit 700% improvement in current gain at low collector current regimes by the reduction of surface recombination current, as compared to those without passivation. Therefore, the proposed low-temperature and low-cost LPO can easily be implemented and can provide new opportunities in device applications.

6. Acknowledgements

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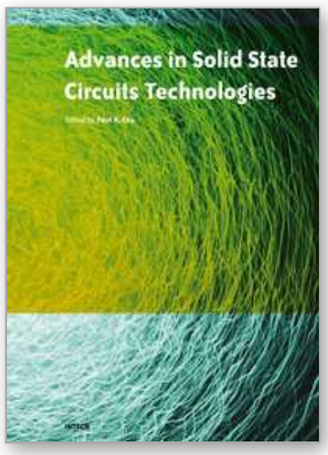

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