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Integrated ASIC System and CMOS-MEMS Thermally Actuated Optoelectronic Switch Array for Communication Network

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1. Introduction

The advancement of communication technology and growth of internet traffic have continuously driven the fast evolution of networks. Compared to the traditional optoelectronic switch, all-optical switch provides high throughput, rich routing functionalities, and excellent flexibility for rapid signal exchange in fiber optical network. Among various all-optical switches, thermal actuated ring switch provides the advantages of high accuracy, easy actuation, and reasonable switching speed. However, when scale up, thermal ring switch may encounter issues related to fabrication error, non-accurate wavelength response, and large terminal numbers in the control circuit.

Planar-lightwave-circuit switch (PLC-SW), employing thermo-optic (TO) effect of silica glass for light switch, is a very promising technique for communication applications because of low insertion loss, high extinction ratio, long-term stability, and high reliability. There have been many matrix switches designed based on the TO effect with low-loss, polarization insensitive operation, and good fabrication repeatability. For example, 8×8 matrix switches were fabricated by using a single Mach-Zehnder (MZ) switching unit and demonstrated well performance in transmission systems, so as an 8×8 matrix switch and a 16×16 matrix switch by the similar MZ switching unit. 32×four-channel client reconfigurable optical add/drop multiplexer on planar lightwave circuit. However, when scaled up, thermal ring switch may encounter issues related to large terminal numbers in the control circuit, fabrication error and non-accurate wavelength response. For example, if conventional driving circuits are employed for a 16×28 or even larger switch array, 448 or more terminals will be required for control. Such a large number of terminals would complicate the module structure and occupy a large area. On the other hand, when a DC-current is applied for balancing wavelength offset from fabrication error, the input power will result in a temperature elevation of the neighboring switches, thus changes the related refractive indexes and therefore deviate wavelengths.

To solve the aforementioned issues, this chapter proposes a ring resonator with silicon nitride as the core layer and silicon dioxide as the cladding layer was designed and fabricated on silicon substrate, a novel architecture of high selection speed three dimensional (3D) data registration for driving large-array optoelectronic packet switches. The 3D driving architecture can successfully reduce the total numbers of control pads into

31 for 448 switches as well as the scanning time up to 67 % reduction with a higher signal rising speed and smaller circuit area. All the sub-circuits, including power control, digital I/O, analog-to-digital converter, power drivers were integrated into a single IC. On the other hand, instead of DC current control, wavelength lock is realized by amplitude and frequency modulated heating pulses for stabilization of temperature and fine-tune of wavelength from fabrication imperfection and environment fluctuation. This planar-lightwave-circuit has been designed, fabricated, and characterized. It is demonstrated not only the functionality in optical packet switches but also the consistency between simulation and experiment results.

In this research, we design the tunable micro ring resonators and propose the employment of an integrated ASIC system CMOS technology control circuit to compensate the fabrication error and tune as well as lock the wavelength in a thermal-actuated ring-type optical switch through a frequency modulation scheme. The use of a standard and commercial CMOS technology for designing micro resonators entails a set of limitations, such as layer thicknesses, and available materials in an inalterable process sequence. From the MEMS design point of view, those restrictions will limit the electrical properties of fabricated micro-resonators. On the other hand, MEMS integration into a CMOS technology presents unique advantages, like reduction of the parasitic capacitance due to the possibility to monolithically integrate the circuitry, in addition to an expected reduction of the overall production costs.

Additional functionalities can also be added in this circuit by tailoring externally the roundtrip loss or coupling constants of the ring. The design concept can be easily scaled up for large array optical switch system without much change in the terminal numbers thanks to the three dimensional hierarchy of control circuit design, which effectively reduces the terminal numbers into the cubic root of the total control unit numbers. The integrated circuit has been designed, simulated, as well as fabricated, and demonstrated a decent performance with Free Spectral Range (FSR) equal to 1.5nm at 1534 nm and very accurate wavelength modulation to 0.3 nm within 0.01 nm fluctuation for thermal actuated ring type optoelectronic switch.

Thermal actuated optoelectronic ring switch provides the advantages of high accuracy, easy actuation, and reasonable switching speed. However, when scale up, thermal ring switch may encounter issues related to fabrication error, non-accurate wavelength response, and large terminal numbers in the control circuit. Planar-lightwave-circuit switch (PLC-SW), employing thermo-optic (TO) effect of silica glass for light switch, is a very promising technique for communication applications because of low insertion loss, high extinction ratio, long-term stability, and high reliability[1-4]. There have been many matrix switches designed based on the TO effect with low-loss, polarization insensitive operation, and good fabrication repeatability. For example, 8×8 matrix switches were fabricated by using a single Mach-Zehnder(MZ) switching unit and demonstrated well performance in transmission systems [5, 6], so as an 8×8 matrix switch [7] and a 16×16 matrix switch [8] by the similar MZ switching unit. 32×four-channel client reconfigurable optical add/drop multiplexer on planar lightwave circuit [9]. However, when scaled up, thermal ring switch may encounter issues related to large terminal numbers in the control circuit, fabrication error and non-accurate wavelength response. For example, if conventional driving circuits are employed for a 16×28 or even larger switch array, 448 or more terminals will be required for control. Such a large number of terminals would complicate the module structure and occupy a large area. On the other hand, when a DC-current is applied for balancing wavelength offset

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To solve the aforementioned issues, this research proposes a ring resonator with silicon nitride as the core layer and silicon dioxide as the cladding layer was designed and fabricated on silicon substrate, a novel architecture of high selection speed three dimensional data registration for driving large-array optical packet switches. The 3D driving architecture can successfully reduce the total numbers of control pads into 31 for 448 switches as well as the scanning time up to 67 % reduction with a higher signal rising speed and smaller circuit area. All the sub-circuits, including power control, digital I/O, analog-to-digital converter, power drivers were integrated into a single IC. On the other hand, instead of DC current control, wavelength lock is realized by amplitude and frequency modulated heating pulses for stabilization of temperature and fine-tune of wavelength from fabrication imperfection and environment fluctuation. This planar-lightwave-circuit has been designed, fabricated, and characterized. It is demonstrated not only the functionality in optical packet switches but also the consistency between simulation and experiment results.

2. Planar-lightwave-circuit design and principle

2.1 Design of wavelength modulation and lock

In this research, PLC filter will usher as a model system for demonstration. A PLC filter is consisted of arrays of micro-rings (MRs) with the ring radii in the order of tens of micrometers, possessing extremely small-area and providing the characteristic of high selectivity. Based on the design of this device, a four-channel PLC filter is depicted with four MRs, as schematically shown in Fig. 1. The operation principle of this device is as the first column of the optical circuit is on each MR drops an incoming signal λx into one of the output channels Ioutx when the MR resonance frequencies matching that of the incoming signal [10-11]. In this research, the design, fabrication, and measurements of a four-channel thermally tuneable MR-based filter PLC controller is presented. Silicon dioxide and silicon nitride were selected as an optical thin film system to compose the micro-rings on top of a silicon substrate. As shown in Fig. 2, the width of straight and ring waveguide was chosen as 2.0 μm. To ensure single mode operation at TE polarization, the height of waveguides was determined to be 0.45 μm by a 3D finite-difference time-domain simulation using RSoft-FullWave(a finite-difference time-domain solver of Poisson's equations)[12-13]. The simulation flow is electro-thermal transport and optics, then according to follow electrostatic potential equation (1) and carrier continuity equations (2), electrons, holes relative derived among temperature, core index, and radius. The effective index method was employed to determine the radius of the ring as 9.965 μm.

1. Poisson's Equation (Electrostatic Potential)

$$\nabla \cdot \varepsilon \nabla \varphi + q(N_D^+ - N_A^- + p - n) = 0 \quad (1)$$

2. Carrier Continuity Equations (Electrons, Holes)

$$\frac{\partial n}{\partial t} + \nabla \bullet j_n + U = 0 \quad \text{And} \quad \frac{\partial p}{\partial t} + \nabla \bullet j_p + U = 0 \quad (2)$$

3. Lattice Heat Equation (Temperature)

$$\frac{\partial}{\partial t}(c_L + \frac{3}{2}(n+p)k)T = \nabla(K_L \nabla T - \overrightarrow{S_n} - \overrightarrow{S_p}) + \overrightarrow{j_n}\overrightarrow{E} + \overrightarrow{j_p}\overrightarrow{E} + R_{dark}E_g \quad (3)$$

4. Photon Rate Equation (Modal Photons)

$$\frac{\partial S_{m,w}}{\partial t} = (G_{m,w} - \frac{1}{\tau_{m,w}})S_{m,w} + R_{m,w}^{spon} \quad (4)$$

5. Derived Helmholtz Equation (Mode Profile)

$$\nabla^2\phi + \varepsilon k_o^2\phi = 0 \quad (5)$$

Where,
n, p: Electron/Hole Density
V: Electrostatic Potential
T: Lattice Temperature
G, R: Optical Gain/Recombination
f: Lasing Frequency
A: Optical Wave Amplitude
S: PhotonNumber
K: Quantum Mechanical Wavefunction
The condition for single mode operation of a Si3N4 optical rib waveguide with a refractive index 2.06 operating at 1.55μm was analyzed using beam propagation method (BPM). The full vectorial BPM was used to analyze the waveguide structure in Fig. 3 for single mode propagation and polarization independence.

Height\width(μm)	0.2-0.4	0.5-0.8	0.9-2.0
0.3	single	multi	multi
0.4	single	single	multi
0.5	single	single	single
0.6	single	single	single
0.7	single	single	single
0.8	single	single	single
0.9	single	single	single

Table 1. Summarizes the waveguide mode.

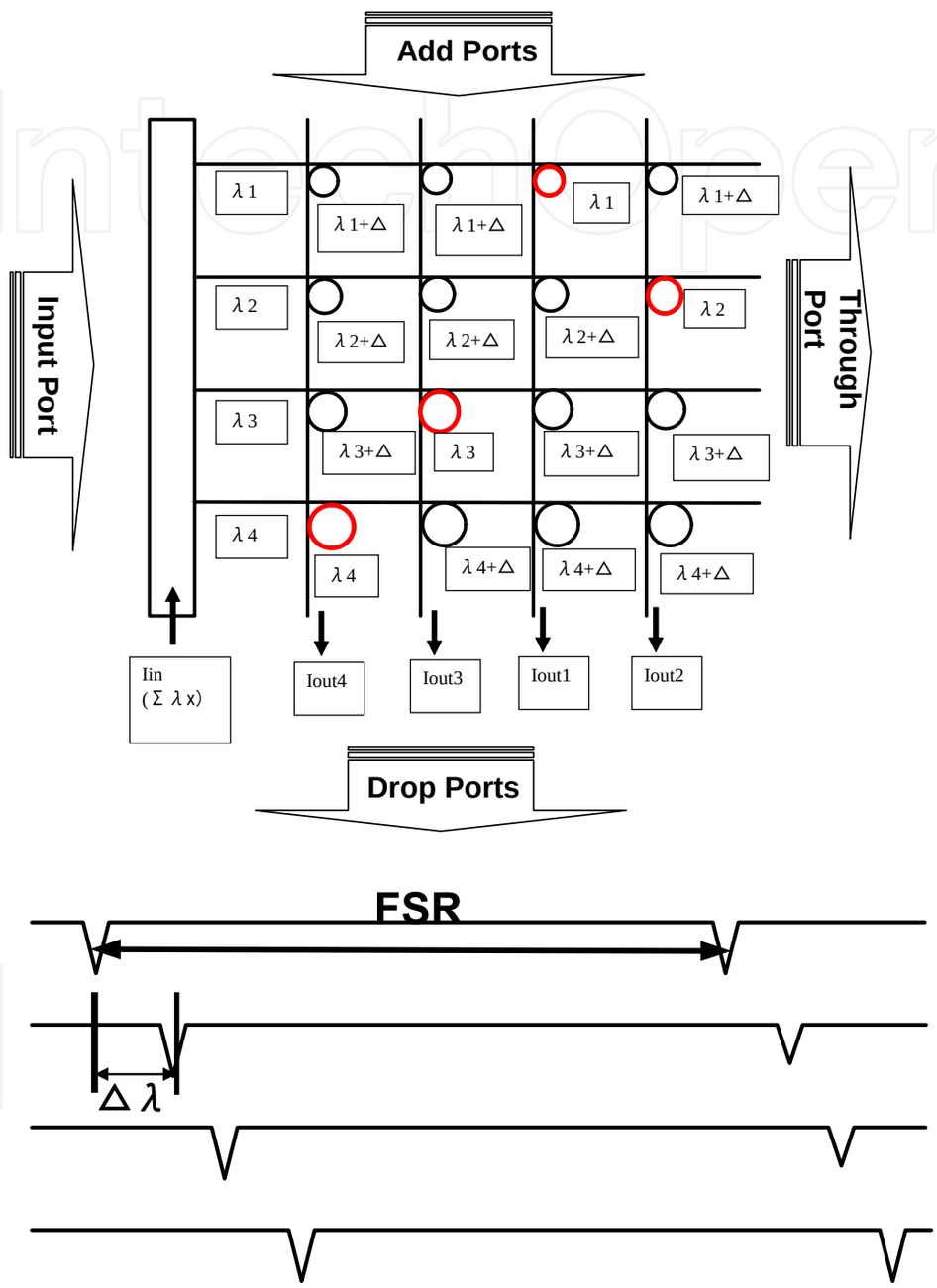

Fig. 1. Schematic of a four-channel PLC.

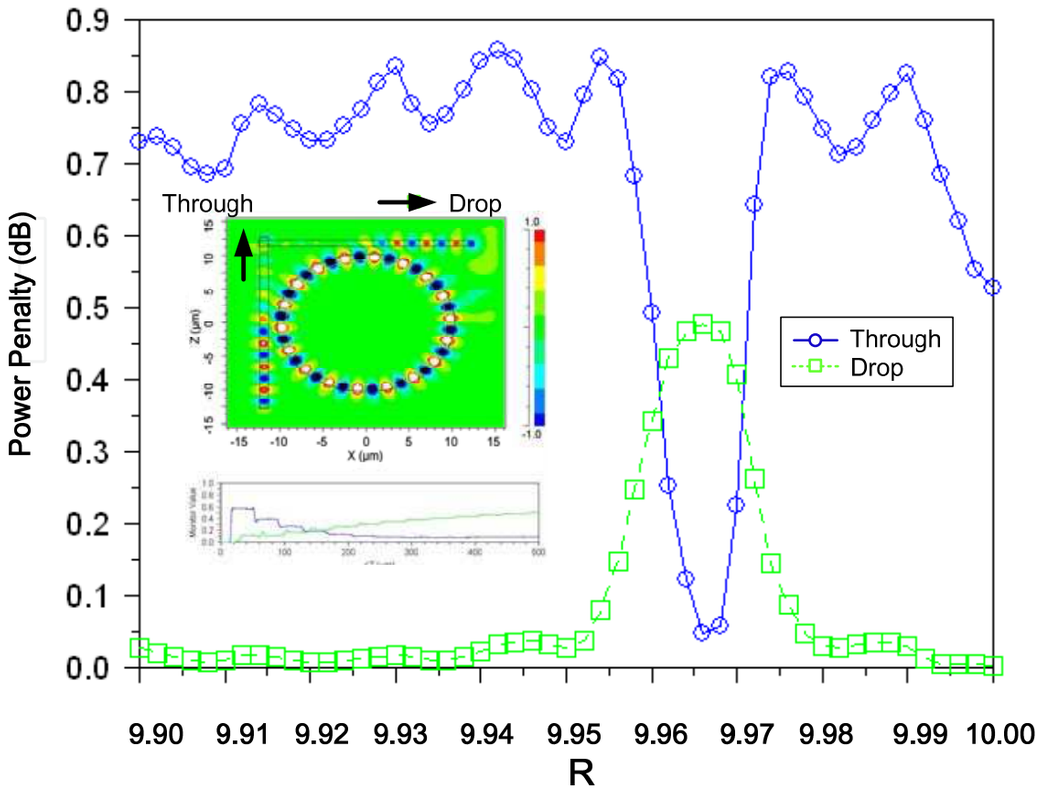

Fig. 2. Transmittance for the radius of micro ring.

According to the BPM calculations, for height = 0.4~0.5μm, width = 0.9~2.0μm enable single mode in the TE polarization. Table 1 summarizes the calculated number of waveguide modes for our studied height and width ratios. Similar single mode output intensity patterns were imaged from other fabricated control waveguide of various height and width. Fig.4(a)、(b) and (c) depicts the imaged mode profiles have only one field maximum near the center for both the horizontal and vertical directions. Insets show the BPM calculated fundamental mode profiles from the same waveguide geometries, depicting similar Gaussian-like mode profiles.

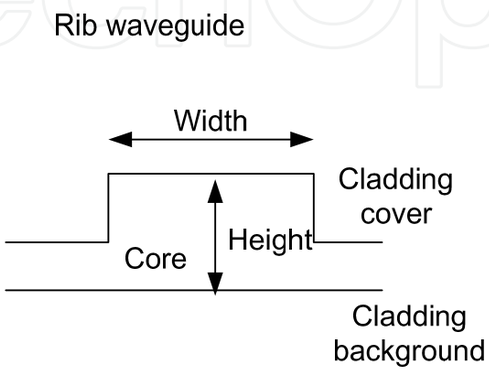

Fig. 3. Schematic cross section of a rib waveguide.

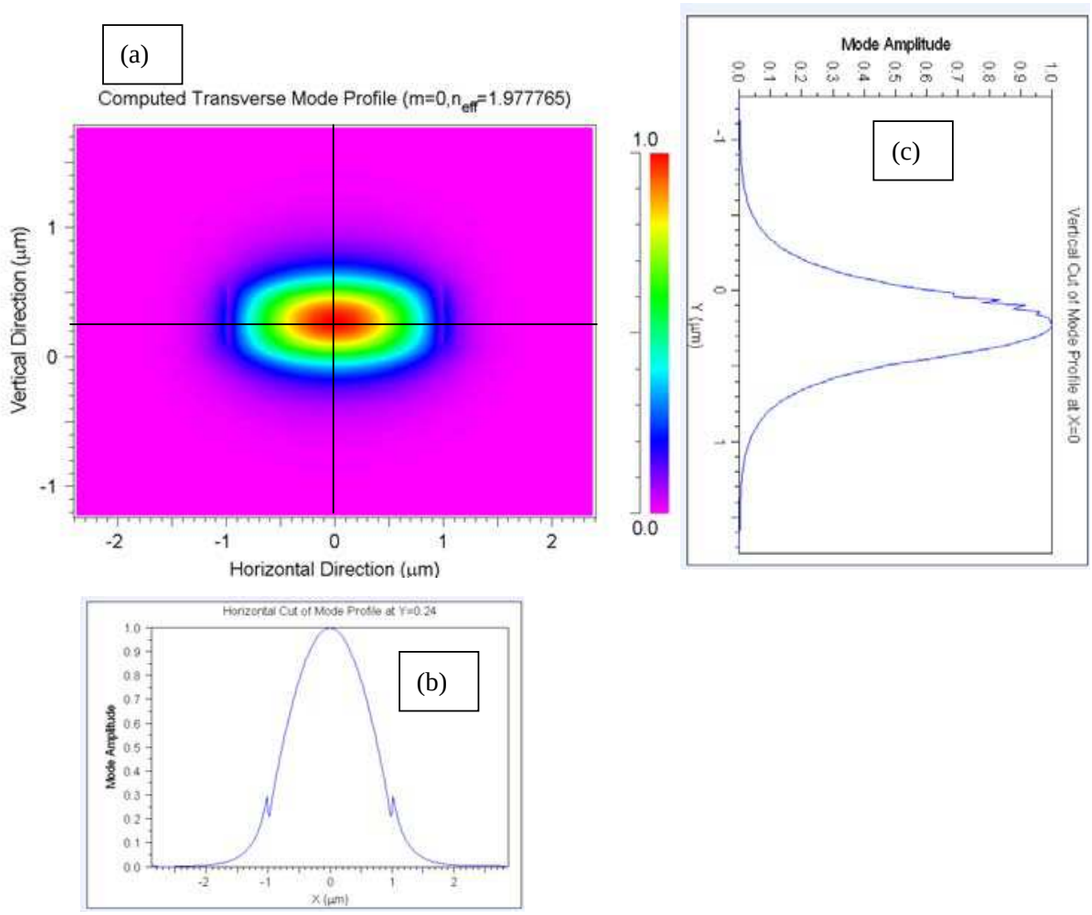

Fig. 4. Simulated fundamental mode profile from BPM-based calculations.

In the process of making the rib waveguide as shown in Table 2, we also examined four different process parameters to see how they affect the final waveguide's dimensions. The first step was to investigate the polarization characteristics of the waveguide due to its geometry. Various waveguide heights ranging from 0.3 to 1.0um and width ranging from 0.9 to 2.0um are considered. While keeping waveguide height constant during the computation, the difference in effective indices of the fundamental TE waveguide modes has been evaluated as the etch depth and waveguide width were varied.

Process number	Process step
1	Thermally grown SiO2 on Si wafer
2	LPCVD deposition of Si3N4 layer
3	Spinning of resist, patterned by photolithography(E-Beam) and structure by RIE
4	Deposition of PECVD SiO2 cladding layer and annealing of layer stack
5	Sputtering a Platinum (Pt) thin film
6	Patterned by photolithography and Pt wet-etch.

Table 2. Process flow for SiO2/Si3N4 coupled microring resonators.

Single mode propagation is an important requirement for optical waveguide devices for use with single-mode fiber; it can reduce the coupling loss. In this research, a technique is used for calculating the field distribution of the Si3N4 rib waveguide. The waveguide was modeled using the three-dimensional full-vectorial beam propagation method (BPM) to calculate the effective refractive indices and modal field profiles for various waveguide widths, heights and etch depths. The scanning electron micrograph (SEM) of Fig. 5 shows such a fabricated rib waveguide.

We experimentally verify the practically single mode nature of our deeply etched rib waveguides by imaging control straight waveguides output intensity patterns. Fig.6 shows the representative imaged waveguide output intensity profile with waveguide of the order of 1550nm.

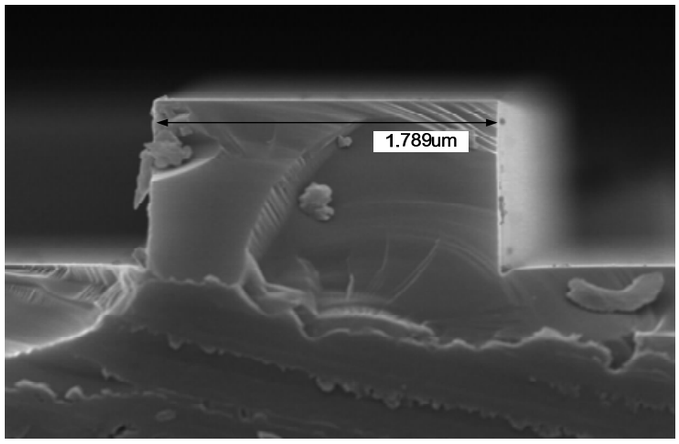

Fig. 5. SEM image of the waveguide cross section.

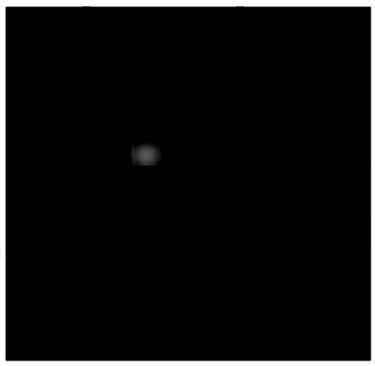

Fig. 6. Imaged waveguide output intensity profile.

In the wavelength modulation, thermal optic effect was employed to shift the resonance wavelength at an amount of $\triangle\lambda$ by the tuning of effective index at different temperatures. This wavelength shift can be used to tune the passband to the desired wavelength. The principle of wavelength modulation is shown in Fig. 1, illustrating that the elevation of temperature on one MR switch shifts the center wavelength by $\triangle\lambda$ but remain the same Free Spectral Range (FSR). The term FSR is borrowed from Fabry Perot interferometry, and describes the maximum spectral range one can arbitrarily resolve without the interference

from the neighbouring signals. On the other hand, a high extinction ratio can be obtained through the filtering effect from the MRs with a steep wavelength response. A relationship between the radius of the ring R, the effective group index n_g, and the FSR is given by equation (6):

$$FSR = \frac{\lambda^2}{2\pi R n_g} \tag{6}$$

where λ is the wavelength [14-15].

In temperature control, frequency modulation was employed instead of voltage level modulation due to the simplicity of implementation by digital signals. Through frequency modulation, the temperature in the thermally tuneable PLC modules can be maintained almost constant and this will result in a more accurate center wavelength for the optical communication channel. It also ensures rapid response of the PLC module as the heater has been modulated on and off in a high frequency (~MHz). As a result, the PLC module at room temperature was able to achieve a very small temperature fluctuation within 0.1°C which can not be achieved by using traditional DC controls.

In order to compensate the fabrication error of the thermal ring switch, a simple and practical phase-trimming technology was employed to avoid the need of electrical biasing. The phase-trimming technique employs a local heating technology by the employment of a thin-film heater embedded under the optical ring in a feedback loop for the fine tune of the optical phase. However, if DC bias is employed in the phase control, the temperature of the neighbouring switch may encounter drift (cross talk) as well as slow response for temperature compensation. To lower down the cross talk effect, provide more accurate temperature control, and speed up thermal response of the optical ring, a frequency modulated heating scheme is employed by dynamic feedback of the frequency of heating pulses.

To achieve the above goal by frequency modulation for accurate temperature control, this study employs a selection algorithm to select a proper waveform pre-stored in the lookup table in an ASIC(Application specific integrated circuits) chip, in which all waveforms have been simulated and optimized for different temperature situations. Each drop and filter channel is assigned a temperature for the desired wavelength shift. The temperature is maintained by a corresponding waveform from the result of the sum of three signals, including data (address), select, and power.

2.2 Design of three dimensional controller

In traditional control circuit design for thermal optical type switch array, each optical ring requires one heater for wavelength adjustment. As a result, when the optical switches scale up into a large array, the numbers of input/output ports will increase enormously. To handle large array of driving circuits for such a heater array, two dimensional (2D) circuit architecture was employed by traditional driving circuits to reduce the IO number from n*n into 2n+1. However, this reduction still can not meet the requirement for high speed signal scanning with low data accessing points when switch numbers greater than 1000.

To achieve this, in this study, a three dimensional data registration scheme to reduce the number of data accessing points as well as scanning lines for large array optical packet switching chip with switch number more than 1000 is proposed. The total numbers of data

accessing points will be $N=3\times\sqrt[3]{Y}+1$, which is 31 for 1000 switches by the 3D novel design, the scanning time is reduced down to 33% (The scanning speed is also increased by 3 times) thanks to the great reduction of lines for 3D scanning, instead of 2D scanning. The property comparison among 1D, 2D, and 3D architectures is listed in Table 3. As the optical switch number increases, a higher order control circuit can effectively reduce the pad number. In addition, the shape and amplitude of the driving signal can be optimized to increase the speed of the response with low driving powers [16].

X :Pads 、Y :Switches	X~Y +1	$X=2\times\sqrt[2]{Y}+1$	$X=3\times\sqrt[3]{Y}+1$ (X : Connection lines , Y :Switches)
Switches	1000	1024	1000
Ring resistors	1000	1024	1000
Interconnect Pad	1001	65	31

Table 3. Performance comparison among 1D, 2D, and 3D driving schemes.

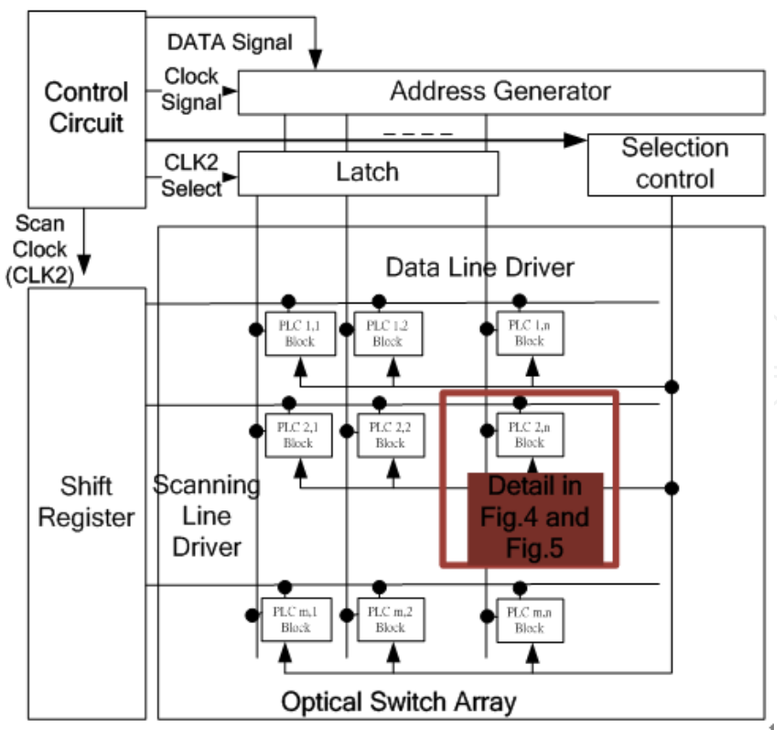

Fig. 7. Block diagram of control algorithm for micro-ring switches.

In the proposed novel 3D design, different from the 2D one, as shown in Fig. 3, the digital driver includes a clock-control circuit, a serial/parallel-conversion circuit, a latch circuit, a level shifter, a D/A converter comprised of a decoder, and an output buffer comprised of an operation amplifier. The D/A converter receive a gray-scale reference voltage from an external source [17-21]. The clock-control circuit receives control signals from an external control circuit. Based on the received control signals, the clock-control circuit attends to control of the latch circuit, the D/A converter [22-24], the output buffer by using a latch-control signal.

The general strategy that we employ is to integrate all relatively small-signal electronic functions into one ASIC to minimize the total number of the components. This strategy demonstrates that both the cost is lowered and the amount of the printed circuit board area is reduced. Based on this concept, a smart 3D multiplexed driver for optical packet switching chip with more than 1000 rings are proposed and the circuit architecture is shown in Fig. 7. Three lines are employed to control the heating of one micro-ring, including voltage, shift register, and data line. The relationship among the waveforms is shown in Fig. 8. Each heater resistor requires a voltage line for the driving current flow and shares the same ground with the other resistors. The resistors are individually addressable to provide unconstraint signal permutations by a serial data stream fed from the controller. The shift register is employed to shift a token bit from one group to another through AND gates to power the switch of a micro-ring group. The selection of a ring is thus a combined selection of the shift register for the group and the data for the specific ring. Such an arrangement allows encoding one data line from the controller to provide data to all of the rings, permitting high-speed printing by shortening the ring selection path and low IC fabrication cost from the greater reduction of circuit component numbers.

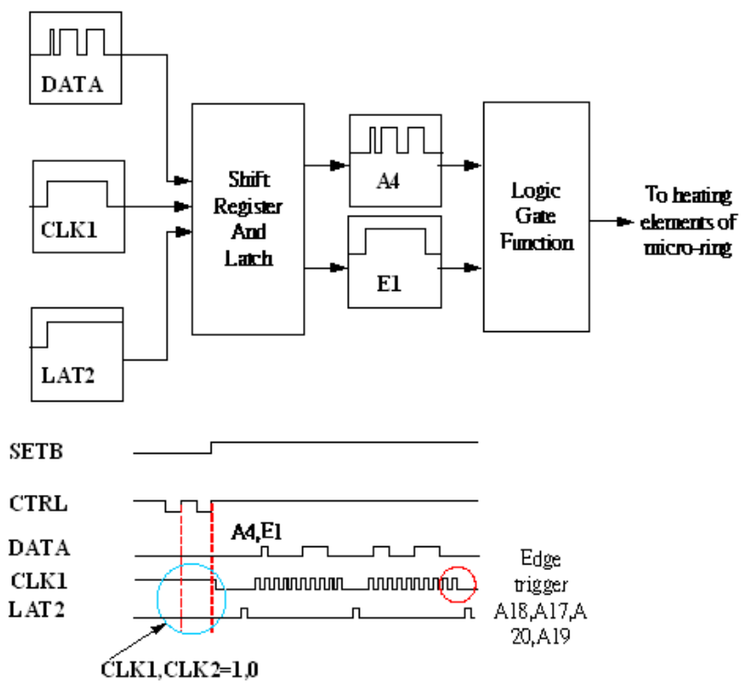

Fig. 8. Example of input waveform for controller from FPGA.

The received optical data information has to be converted into data at an optimal transfer rate (frequency) in order to conform to the ring characteristics. To the end, the clock-control circuit divides the 8-bit optical packet switching signals supplied to the data driver, as shown in Fig. 7, with an aim at lowering the operation frequency. The serial/parallel-conversion circuit converts serial signals of a plurality of channels into parallel signals, and supplies the parallel signals to the latch circuit. The latch circuit temporarily stores the received parallel signals, and supplies them to the level shifter and the D/A converter at predetermined time [25-27]. The level shifter converts a logic level ranging approximately from 3.5 V to 5 V into a ring array voltage level that ranges from 5.5V to 8.5V for various heater resistors as a result of variation processing conditions.

In the signal flow design, optical switches are usually scanned over one by one without jumping on un-activity switches. As a result, for the optical packet switching chip with 448 optical switches, a 1, 2 or 3 dimensional circuit architect will needs 448, 36, and 5 unit times for scanning over all of the switches. Therefore, the scanning time of the 3D multiplexing circuit from the first address line to the 16th, as an example, takes only 5 units of clock time from the simulation result, much faster than that of the 2D configuration with 16 units of clock time. Thus the maximum scanning time for the 3D circuit will be reduced to 30% of that in the 2D case.

To simultaneously write signals into the driving circuit, multiplexing data latches and shift registers are employed by the application of commercial available CMOS ICs. Small numbers of shift registers, control logics, and driving circuits can be electrically connected and integrated with optical packet switching using standard CMOS processes. Fig. 9 shows the driving circuit of the three-dimensional architect. The desired signal for "S" selections and "A" selections can be pre-registered and latched in the circuit for one time writing.

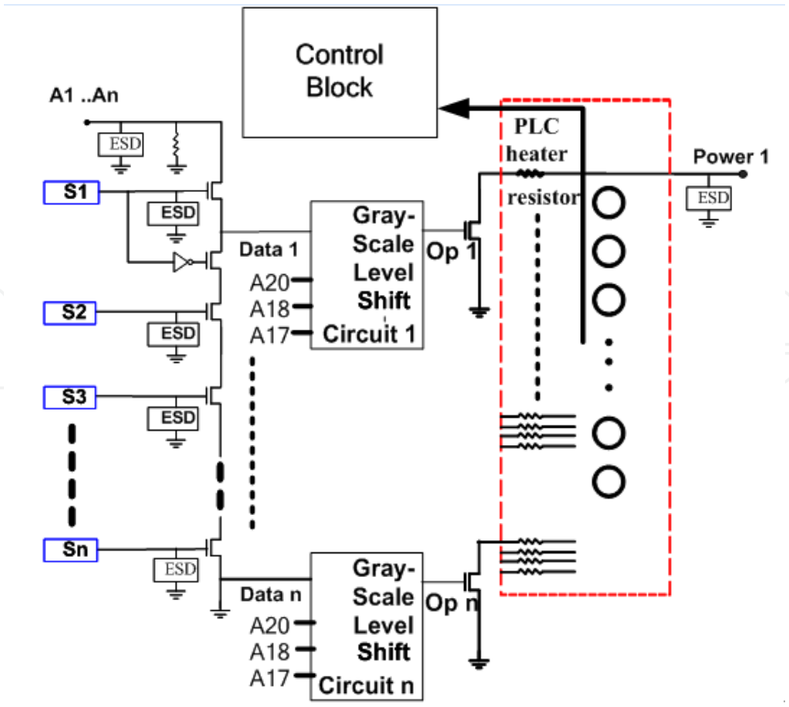

Fig. 9. Architect of three-dimensional driving circuit for micro-ring switches.

The SPICE simulation results on the relationship of input and output signal at 5μs clock time. Fig. 10 demonstrates that not only the switch speed is higher by the level shift device than that of one without level shift circuit, but also the voltage has been enhanced to 5V. An adjustable voltage pulse from 7.98V to 8.02V amplitude modulation is applied to the various heater resistors thanks to the processing condition.
The cooling down of the structure is equally important, though enhancing the speed of the cooling down process might be done by active cooling, but this would require major adaptations to the device and the low cost low power principle would not hold anymore. A much easier way to do this is biasing. In biasing, a DC-current is applied, that will result in a relatively small change in temperature, refractive index and therefore resonance wavelength. To heat the device, the wide pulse width signal or high gray scale level voltage is applied; to cool it down, a narrow pulse width signal or low-level voltage is applied. See Fig. 10 for the simulated behavior of high and low bias driving. The maximum current that can be applied is limited, due to the destruction of the heaters at high powers. The use of a bias will therefore cause a smaller modulation depth, but the modulation will be faster, since the time needed for cooling down is reduced.

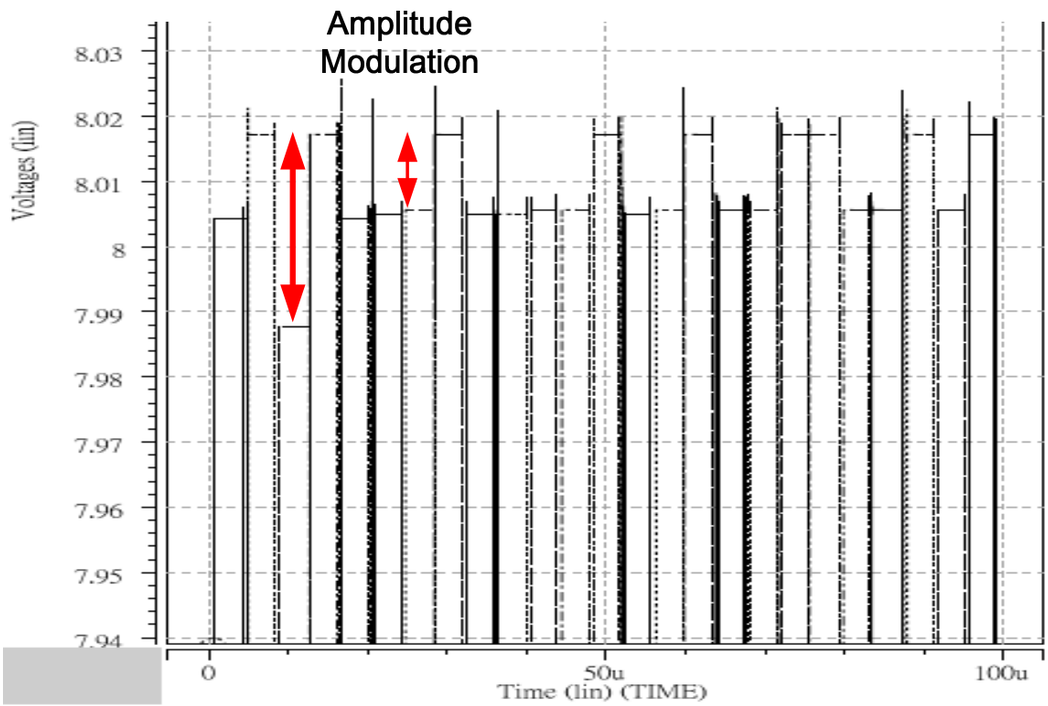

Fig. 10. Transient simulation of the input and output signals of the level shift device.

Power consumption of a narrow pulse width signal or low-level voltage applied for the thermally actuated optical switch array is very small comparing a DC-current applied. The main advancement of this new concept is that the drive signal opening the switch tracks the serial/parallel- conversion circuit, which converts serial signals of a plurality of channels into parallel signals, and supplies the parallel signals to the latch circuit.

If we analyze the total wire power, we calculate that the intermediate interconnection power is the dominant part of the total wire power. The total wire power is scaled down of the three dimensional hierarchy of high gray scale control circuit design, which effectively reduces the terminal numbers into the cubic root of the total control unit numbers.

3. Experimental and results

3.1 Wavelength modulation and lock

By using a Commercial Finite Difference Solver (CFD-RC, USA) for thermo-optical problems, the temperature profile of the MR and the relative changes of refractive indexes can be simulated, as shown in Fig.11(a) and Fig.11(b). Electro-thermal changed temperature by ASIC multiplexing data signal applying to coupled-ring-resonator for adjustment core index. Optimal tunable center wavelength 1511nm conform the shifted core indexes from 2.000 to 2.008. Although the temperature distribution on the ring is about 1˚C, the average temperature of the ring is employed as a reference for the temperature control and the tolerance is within 0.1˚C. To reduce overshooting and obtain rapid set up of ring temperature, heating pulses with amplitude modulation were employed. Through simulation, optimized driving signal can be obtained to maintain stable wavelength in 0.1 ms by accurate temperature modulation [28]. The temperature fluctuation can be controlled within 0.1°C, with a wavelength variation locked in 0.01 nm, as the measured result shown in Fig. 12.

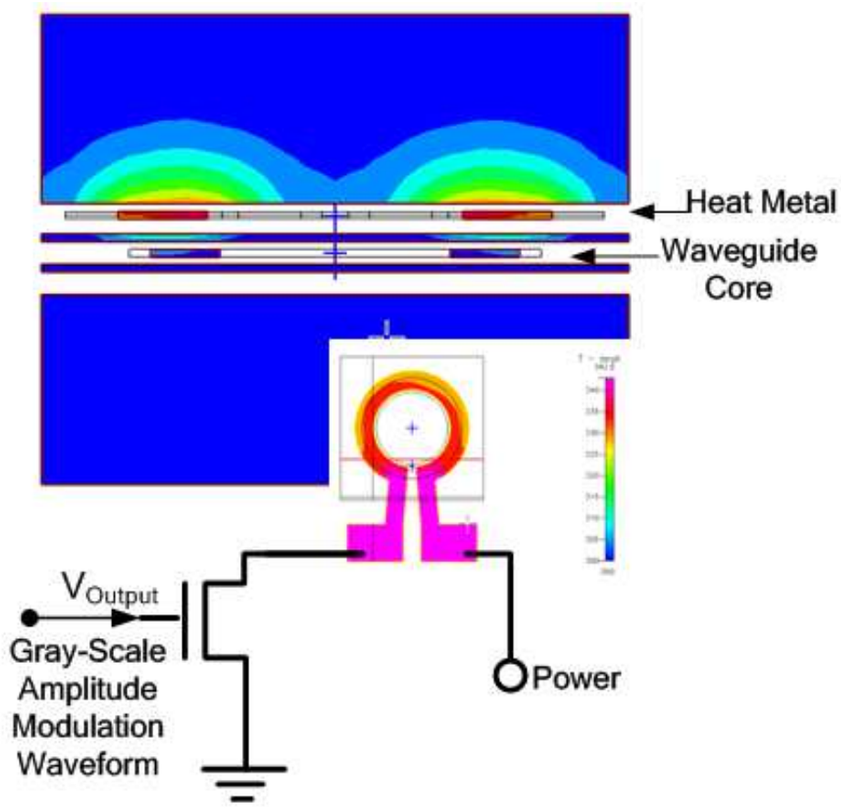

Fig. 11(a). Driving architecture of wavelength lock and simulation profile.

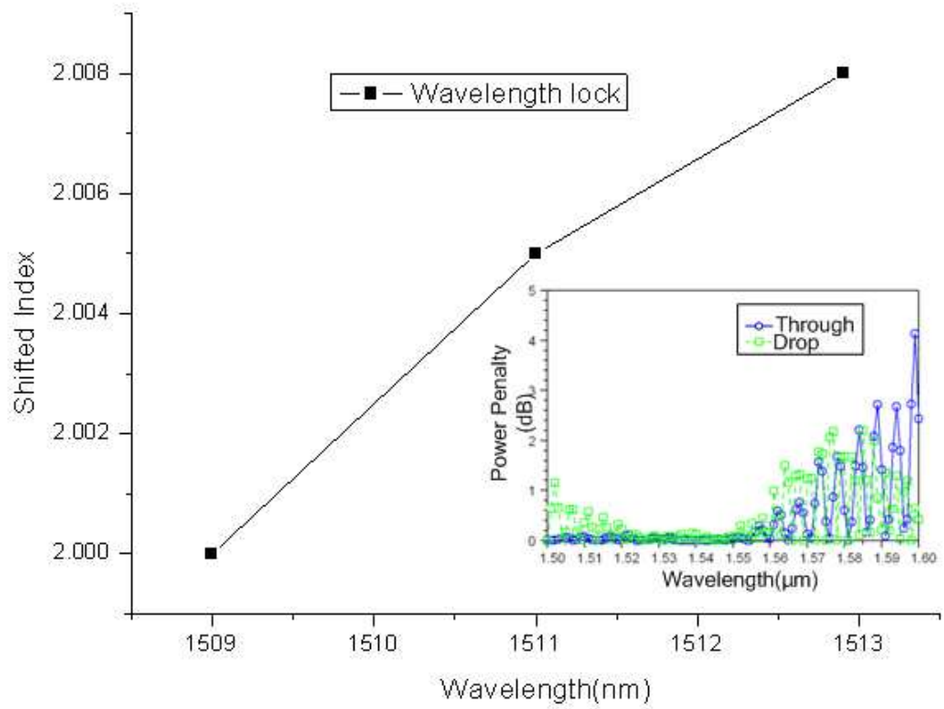

Fig. 11(b). The relative of shifted index and wavelength.

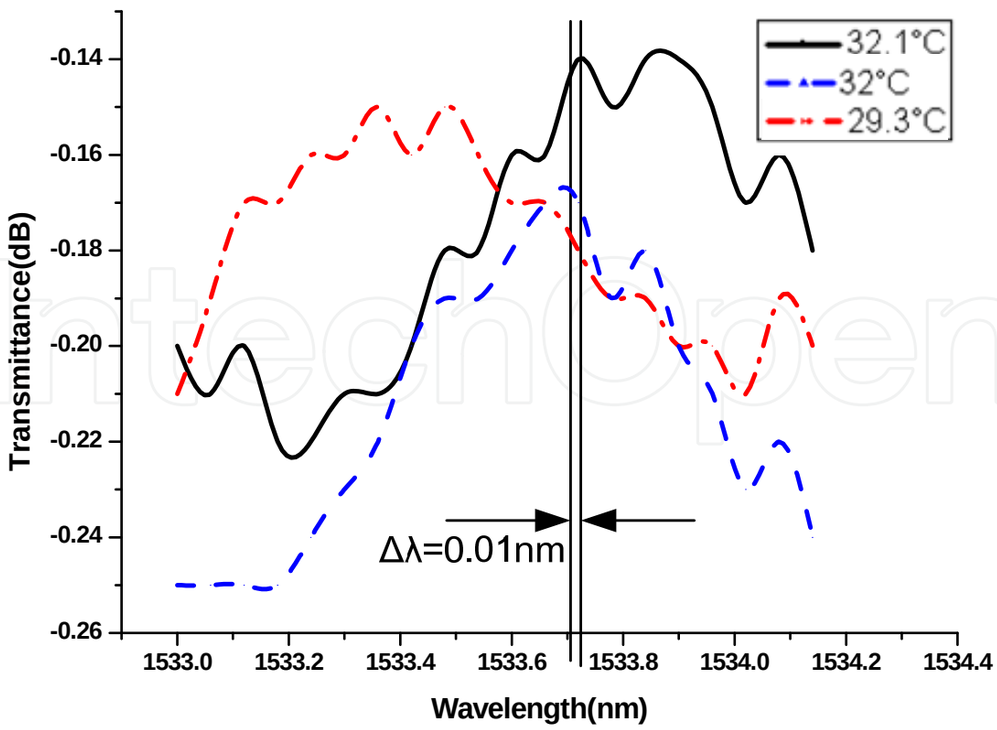

Fig. 12. Wavelength lock.

3.2 Controller and wavelength modulation result

To demonstrate basic functions of the 3D controller, as a result, we were able to reduce the number of electrical terminals to 5 control terminals and 1 power supply terminal. The controller was designed for a 0.35 μm CMOS process with a total circuit area of 2500×2500 μm², which is 80% of the circuit area by 2D configuration for 448 switches.

In the Logic Analysis, the relationship between the ASIC input and output is shown in Fig. 13. The input signals include DATA (signal for selected switch action), CLK1(signal to scan DATA signal), CLK2(signal to latch DATA signal or select), CTRL(signal to select enable type), as well as SETB(the time sequence to set up CTRL or power), and the output signals match the designed ASIC signals very well. Fig. 14. shows the image of a fabricated 16×28 matrix switch controller module. In this module, the chip area of 2.5×2.5 mm and was fabricated by a two-poly four-metal (2P4M) 0.35μm twin-well CMOS technology (TSMC, Taiwan Semiconductor Manufacturing Company Ltd). Each transistor is surrounded by full guard ring for preventing electrostatic shock.

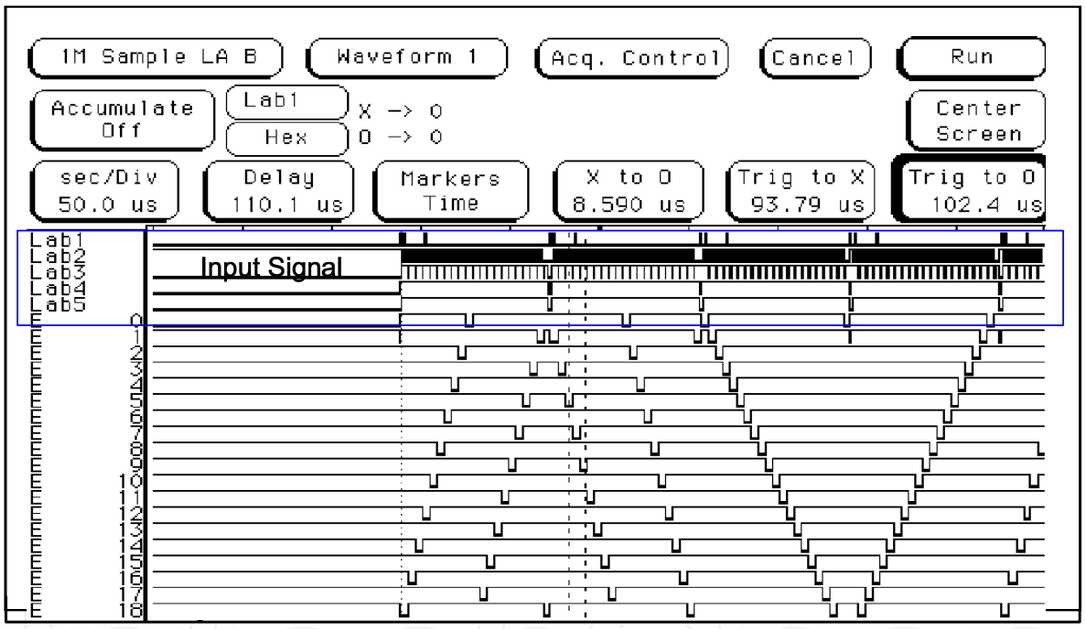

Fig. 13. FPGA verification result.

The testing result of the IC demonstrated the scanning of 448 ring switches takes 60.5 μs for 2D circuit architect while 20.5 μs for the 3D one, representing a time saving of 40 μs or a 67% time reduction. The measurement results of serial output signals for four channels, as shown in Fig. 15, demonstrated a simultaneous operation of four different temperature /wavelength modulations in each channel. By using the optimized driving signals, modulation frequencies up to 10 kHz were measured, resulting in thermal switching speeds in the order of 0.1 ms.

The micro-rings are made with the use of standard clean room fabrication technology. The fabrication of silicon nitride waveguides starts with a six inch diameter polished <100> silicon wafer. First a planar waveguide structure with a SiN(n=2.06@ λ =1550nm) core and SiO2(n=1.452@ λ =1550nm) cladding is formed. Finally the heater layer is deposited by

sputtering a Platinum (Pt) thin film and patterned by photolithography and Pt wet-etch. Some results of temperature coefficient of resistance (TCR) measurements on platinum thin films. The shift in center wavelength of the ring λc is a function of the difference in effective index induced by heating the device that is given by equation (7):

$$\delta\lambda c = \frac{\lambda \Delta Neff}{Neff} \tag{7}$$

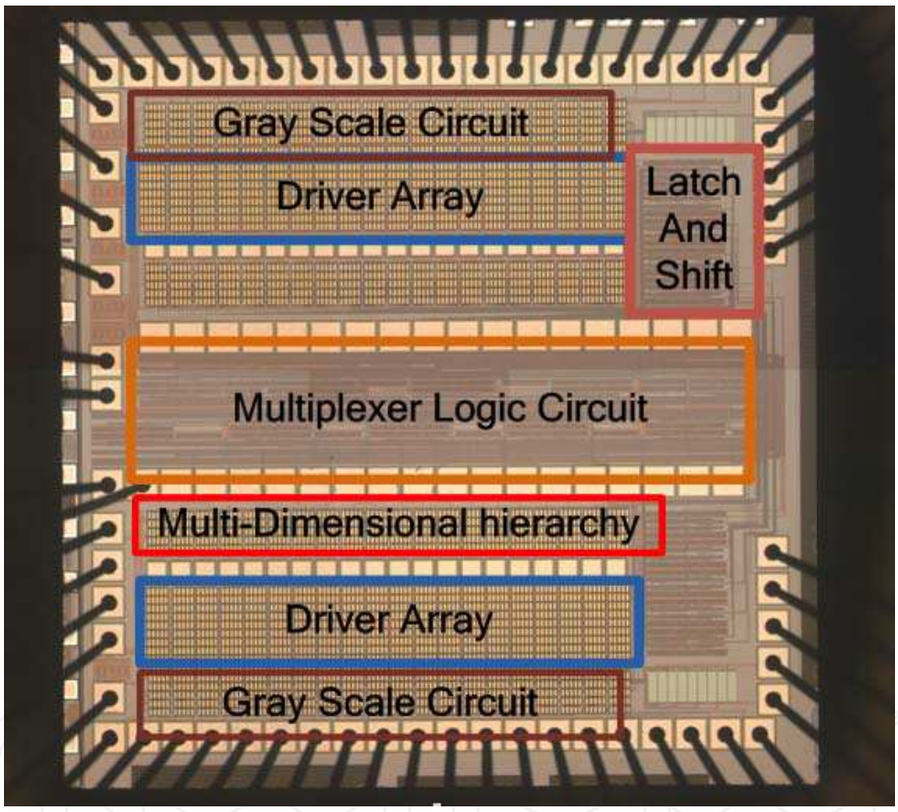

Fig. 14. Photograph of fabricated control IC chip.

In the wavelength modulation, temperature variation induced spectrum shift was measured, and the result is shown in Fig. 16, for the temperature changed from 29°C to 32°C, for which the thermal resonance shift is determined to be 0.1nm/°C. The temperature fluctuation can be controlled within 0.1°C, with a wavelength variation locked in 0.01 nm. The measured values are FSR=1.5nm and center wavelength shift λc=0.3nm at a center wavelength of λ=1532nm.

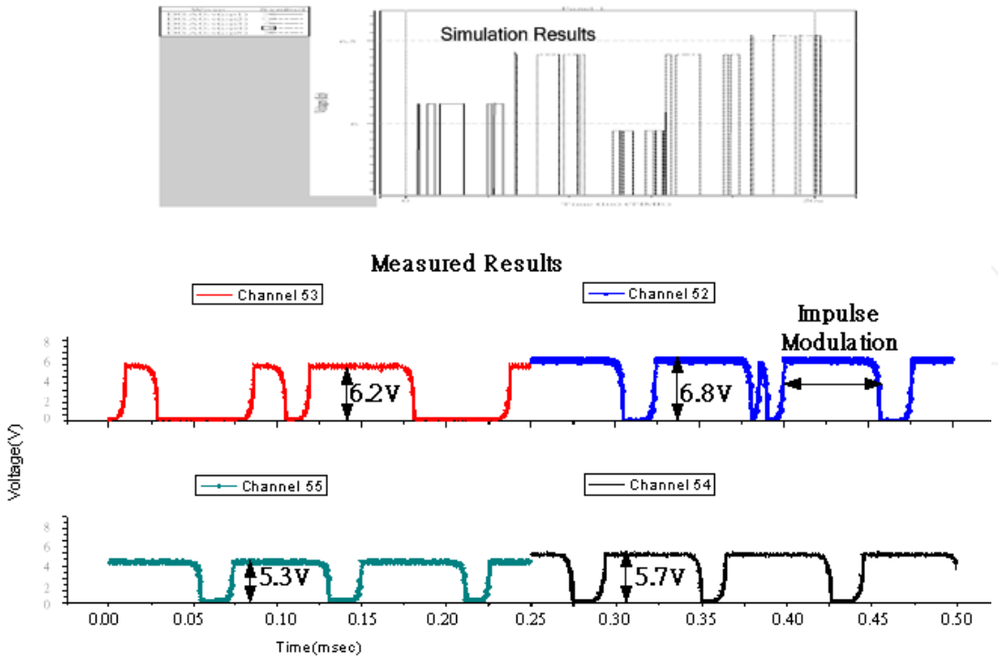

Fig. 15. Measurement result of serial outputs.

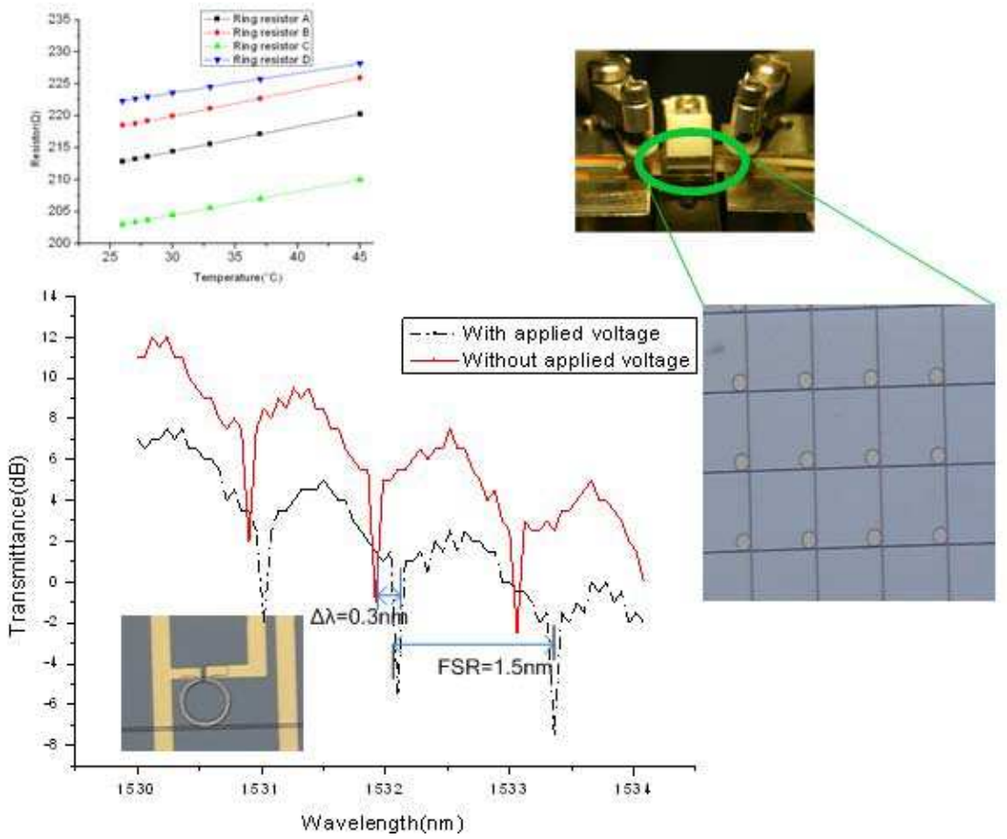

Fig. 16. Wavelength shift of transmission spectrum in coupled-ring-resonator.

4. Conclusion

The next generation of optical networking requires optical switches with complex functionality, small size and low cost. In this research, we have successfully designed and fabricated a silica-based 16×28 PLC-SW controller module in which we incorporated a switch chip based on PLC technology and new driving circuits with a serial-to-parallel signal conversion function. The new driving circuits significantly reduced the number of control terminals, and enabled us to realize a simple module structure suitable for use in a large-scale switch. It has been demonstrated that the scanning of 448 ring switches takes 20.5 μs by the novel 3D architect, representing a 67% time reduction.
On the other hand, thermal-optical effect was employed for wavelength modulation in this optical switch. To reduce overshooting and obtain rapid set up of ring temperature, heating pulses with amplitude modulation were employed. A temperature variation within 0.1°C can be maintained by this design, which can provide a very accurate wavelength modulation to 0.3 nm within 0.01 nm variation.

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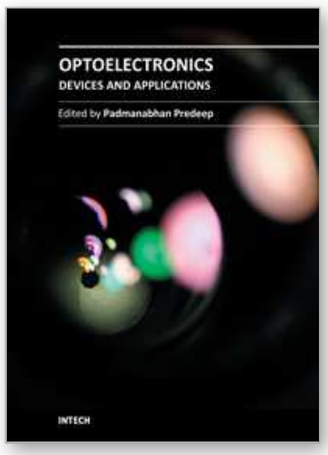

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